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(Final Term Past Paper)

MADE AND SOLVED BY TEAM HADI

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Best of luck!

مہربانی کرکے میری امی جان کے لیے دعا کر دینا اُن کی ۲۰۲۱ میں وافات ہوگی تھی، شکریہ (ہادی)

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CODE:CS302

Question 1: In master-slave flip-flop, master flip-flop will be active in_____of clock whereas slave flip-flop will be active in____of clock.

- Negative edge,positive edge..
- Positive edge, negative edge.
- Positive half, negative half.
- Negative half, positive half..

Question 2: A flash A/D converter uses:

- Counters.
- Flip-flops.
- **Op-amps.**

- An integrator

Question 3: For a gated D-Latch, if EN=1 and D=1 then Q(t+1) = _____

- 0.
- **1**.
- Q(1).
- Invalid.

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Question 4: Which of the following is not the characteristic of a shift register?

- **Serial in parallel in.**
- Serial in parallel out.
- Parallel in/serial out.
- Parallel in parallel out

Question 5: The high density FLASH memory cell is implemented using_____

- **1 floating-gate MOS transistor.**
- 2 floating-gate MOS transistors
- 4 floating-gate MOS transistors.
- 6 floating-gate MOS transistors.

Question 6: When the control line in tri-state buffer is high, the buffer operates like a/an ___gate.

- OR.
- **NOT**
- XOR
- AND

Question 7: The positive edge triggered flip-flop changes its state on___

- Positive half cycle of clock.
- Negative half cycle of clock.
- **Low-to-high transition of clock.**
- High-to-low transition of clock

Question 8: The_____of a ROM is the time it takes for the data to appear at the Data output of the ROM chip after an address is applied at the address input lines.

- Write Time.
- Refresh Time/Recycle Time.
- Read Time.
- **Access Time**

Question 9: The process of converting analog signal to a digital representation (code) is known as____

- Strobing.
- Amplification…. Check it
- Quantization.
- Digitization

Question 10: _____is said to occur when multiple internal variables changes due to change in one input variable.

- **Race condition.**
- Propagation delay.
- Ripple effect.
- Clock skew

Question 11: Which of the following is a symbol of XOR operation in ABEL?

- **$.**
- O.
- #.
- &.

Question 12: If the state diagram of an up/down counter is given, we can find___

- **The next state of a given present state.**
- The previous state of a given present state.
- Both the next and previous states of a given state.

- The state diagram shows only the inputs/outputs of a given states

Question 13: A high level noise margin in a device is determined by the formula___

- **$VNH=V_{OH}(min) - V_{IH}(min)$.**
- VNH=VIH(min) - VOH(min).
- VNH= VOH(max)-VIH(min).
- VNH=VIH(min) - VOH(max).

Question 14: Which of the following signals is applied to the Write Cycle in order to write data to the memory?

- Data signals.
- Address signals….CHECK IT
- Control signals.
- Clear signals

Question 15: A decade counter is reset to its initial state after its value becomes

- 0000.
- 0001.
- 1000.
- 1010

Question 17: A serial in parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains___

- 0000.
- 1111.
- **0111**.
- 1000

Question 18: According to the sampling theorem, the sampling frequency should be___

- Greater than the lowest signal frequency.

- Less than half the lowest signal frequency.
- **Greater than twice the highest signal frequency.**
- Less than half the highest signal frequency

Question 19: The full form of SIPO is____

- **Serial-in Parallel-out.**
- Parallel-in Serial-out.
- Serial-in Serial-out.
- Serial-In Peripheral-Out

Question 20: The_____control line is connected to all memory chips connected together

- Chip.
- Write.
- Read.
- **R/W**

Question 21: PROM stands for___

- Permanent Read Only Memory.
- Portable Read Only Memory.
- **Programmable Read Only Memory.**
- Plugin Read Only Memory

Question 22: The row line in Flash Memory is connected to the_____of each MOS transistor which implements a single bit storage cell.

- Circuit.
- **Control Gate.**
- Cell.
- Terminal

Question 23: The Flip-flop transition table lists all the possible flip-flop input combinations which allow the present state to change to the___state on a clock transition.

- **Next**.
- Previous.
- Current.
- Back

Question 24: The register is a type of____

- Sequential circuit.
- Combinational circuit.
- CPU.
- **Latches**

Question 25: The best state assignment tends to_____

- Maximize the number of state variables that don't change in a group of related states.
- **Minimize the number of state variables that don't change in a group of related states.**
- Minimize the equivalent states.
- Maximize the equivalent states

Question 26: In the Flow-through SRAM, there is (are)_____ Data Output Register(s).

- **No**.
- One.
- Two.
- Three

Question 27: The alternate solution for a multiplexer and a register circuit is_____

- **Parallel in/Serial out shift register.**
- Serial in/Parallel out shift register.
- Parallel in/Parallel out shift register.

- Serial in/Serial Out shift register

Question 28: The hours unit counter circuit is configured as a____counter, counting from 0000 to 1001 when it is enabled by the____counter circuit.

- **Decade, Minutes**
- Down, Seconds
- Up, Hour
- None of the given

Question 29: In an n-bit up-down counter, how many flip-flops are required?

- n/2
- 2n
- **n**
- n^2

Question 30:Keyboard_____is an example of FIFO memory.

- Key
- Port
- **Buffer**
- Driver

Question 31: Next address from the starting address can be obtained by adding_____to the starting address.

- **One**
- Two
- Three
- Four

Question 32: Caveman number system is Base _____ number system

- 2
- **5**
- 10
- 16

Question 33: _____ is used to simplify the circuit that determines the next state.

- State diagram
- Next state table
- State reduction
- **State assignment**

Question 34 : The low to high or high to low transition of the clock is considered to be a(n) _____

- State
- **Edge**
- Trigger
- One-shot

Question 35 :A positive edge-triggered flip-flop changes its state when _____

- **Low-to-high transition of clock**
- High-to-low transition of clock
- Enable input (EN) is set
- Preset input (PRE) is set

Question 36:RCO Stands for _____

- Reconfiguration Counter Output
- Reconfiguration Clock Output
- Ripple Counter Output
- **Ripple Clock Output**

Question 37: The 64-cell array organized as,_____cell array is considered as an 8 byte memory.

- 2x32
- 4x16

- **8x8**
- 16x4

Question 38: How many types of error do Analogue to Digital converters exhibit during their conversion operation?

- 2
- **3**
- 5

Question 39: The decimal number system has,____unique digits.

- 2
- **10**
- 5
- 7

Question 40: In Traffic Signal Controller, When the MANUAL signal is set the____ and_____outputs are set to logic high and low depending upon the input signal FLASHCLK.

- NSRED, EWRED
- NSGRN, EWGRN
- **NSYEL, EWYEL**
- NSWT, EWWT

Question 41: The AND Gate performs a logical function.

- Addition.

- Subtraction.
- **Multiplication**.
- Division

Question 42 : Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state

- Ten
- Eight
- Three
- **Two**

Question 43 :_____ is one of the examples of asynchronous inputs.

- J-K input
- S-R input
- D input
- **Clear Input (CLR)**

Question 44 : _____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

- Race condition
- **Clock Skew**
- Ripple Effect
- None of given options

Question 45: The range of Excess-8 code is from to

- **+7 to -8**
- +8 to -7
- +9 to -8
- -9 to +8

Question 46: Each hexadecimal number digit can be represented by____binary digits. Answer

- **16**
- 2
- 3
- 4


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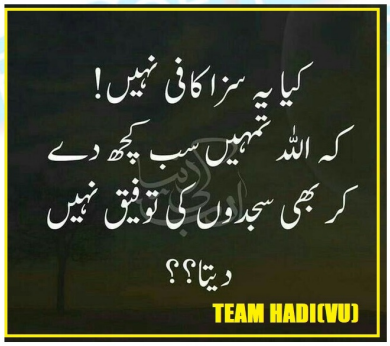
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