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CORRECT ANSWER SOLVED BY HADI
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(Final Term Past Paper)

MADE AND SOLVED BY TEAM HADI

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Best of luck!



Question No : 1 of 52

Marks: 1 (Budgeted Time 1 Min)

Caveman number system is Base _____ number system

Answer (Please select your correct option)

2

5

10

16



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Question No : 2 of 52

Marks: 1 (Budgeted Time 1 Min)

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result



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Answer (Please select your correct option)

1001



0110



correct

1111



1100



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Question No : 3 of 52

Marks: 1 (Budgeted Time 1 Min)

The Gray code is different from the unsigned binary code because _____

Answer (Please select your correct option)

Successive values of Gray code differ by only one bit

correct

Gray Code is positional code

Gray Code does not support negative values

Gray Code ranges from "0" to "9"



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Question No : 4 of 52

Marks: 1 (Budgeted Time 1 Min)

"74ALS" stands for _____



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Answer (Please select your correct option)

- Advanced Low-frequency Schottky TTL
- Advanced Low-dissipation Schottky TTL
- Advanced Low-Power Schottky TTL
- Advanced Low-propagation Schottky TTL

correct

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Question No : 5 of 52

Marks: 1 (Budgeted Time 1 Min)

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

Answer (Please select your correct option)

4

8

12

16



correct



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Question No : 6 of 52

Marks: 1 (Budgeted Time 1 Min)

The cell marked 6 in 4-variable K-Map represent minterm 6 or the maxterm 6 having the following binary value of variables A, B, C and D.



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Answer (Please select your correct option)

A=1, B=1, C=0, D=0

A=0, B=1, C=1, D=0

A=0, B=0, C=1, D=1

A=1, B=0, C=0, D=1



correct

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Question No : 7 of 52

Marks: 1 (Budgeted Time 1 Min)

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

Answer (Please select your correct option)

AND



correct

OR

NOT

XOR



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Question No : 8 of 52

Marks: 1 (Budgeted Time 1 Min)

In a sequential circuit the next state is determined by _____ and _____.



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Answer (Please select your correct option)

- State variable, current state
- Current state, flip-flop output
- Current state and external input
- Input and clock signal applied



correct

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Question No : 9 of 52

Marks: 1 (Budgeted Time 1 Min)

In CMOS 5 Volt series, Input voltage for Logic high signal (V_{IH}) is in the range of _____ volts.



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Answer (Please select your correct option)

3.5 to 5

correct

4.5 to 5

0 to 5

0 to 3.5

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Question No : 10 of 52

Marks: 1 (Budgeted Time 1 Min)

What will be output state when $J = 1$, $K = 0$ and CLR input is active?



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Answer (Please select your correct option)

Q = 1

correct

Q = 0

Retains previous output state

Toggle output

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Question No : 11 of 52

Marks: 1 (Budgeted Time 1 Min)

A feature that distinguishes JK flip-flop from SR flip-flop is _____



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Answer (Please select your correct option)

Toggle condition

correct

Preset input

Type of clock

Clear input

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Question No : 12 of 52

Marks: 1 (Budgeted Time 1 Min)

Which one of the following expressions is an example of Commutative Law for Multiplication?



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Answer (Please select your correct option)

$AB+C = A+BC$

$A(B+C) = B(A+C)$

$AB=BA$

$A+B=B+A$

correct

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Question No : 13 of 52

Marks: 1 (Budgeted Time 1 Min)

The binary values for the standard SOP expression, $ABC\bar{D} + \bar{A}BC\bar{D} + \bar{A}BCD$ are _____



Answer (Please select your correct option)

1110 + 0110 + 0001

correct

1011 + 1111 + 1011

0001 + 1001 + 1110

1010 + 1110 + 0101

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Question No : 14 of 52

Marks: 1 (Budgeted Time 1 Min)

The design and implementation of synchronous counters start from _____



Answer (Please select your correct option)

Truth table

K-map

State table

State diagram

correct

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Question No : 15 of 52

Marks: 1 (Budgeted Time 1 Min)

In a state diagram, the transition from a current state to the next state is determined by _____ and _____



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Answer (Please select your correct option)

Current state, inputs

correct

Current state, outputs

Previous state, inputs

Previous state, outputs

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Question No : 16 of 52

Marks: 1 (Budgeted Time 1 Min)

In _____, the \bar{Q} output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.



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Answer (Please select your correct option)

Moore machine

Mealy machine

Johnson counter

Ring counter

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Question No : 17 of 52

Marks: 1 (Budgeted Time 1 Min)

The sequence of states that are implemented by a n-bit Johnson counter is _____



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Answer (Please select your correct option)

$n+2$ (n plus 2)

$2n$ (n multiplied by 2)

correct

2^n (2 raise to power n)

n^2 (n raise to power 2)

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Question No : 18 of 52

Marks: 1 (Budgeted Time 1 Min)

Flip flops are also called _____

Answer (Please select your correct option)

Bi-stable dualvibrators

Bi-stable transformer

Bi-stable multivibrators

Bi-stable singlevibrators

correct



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Question No : 19 of 52

Marks: 1 (Budgeted Time 1 Min)

For a gated D-Latch, if $EN=1$ and $D=1$ then $Q(t+1) =$ _____



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Answer (Please select your correct option)

0



1



correct

$Q(t)$



Invalid



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Question No : 20 of 52

Marks: 1 (Budgeted Time 1 Min)

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____



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Answer (Please select your correct option)

- Doesn't have an invalid state
- Sets to clear when both $J = 0$ and $K = 0$
- It does not show transition on change in pulse
- It does not accept asynchronous inputs

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Question No : 21 of 52

Marks: 1 (Budgeted Time 1 Min)

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.



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Answer (Please select your correct option)

Set-up time

Pulse Stability time (PST)

Hold time

Pulse Interval time

correct

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Question No : 22 of 52

Marks: 1 (Budgeted Time 1 Min)

The _____ input overrides the _____ input



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Answer (Please select your correct option)

Asynchronous, synchronous

correct

Synchronous, asynchronous

Preset input (PRE), clear input (CLR)

Clear input (CLR), preset input (PRE)

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Question No : 23 of 52

Marks: 1 (Budgeted Time 1 Min)

The divide-by-60 counter in digital clock is implemented by using two cascading counters:



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Answer (Please select your correct option)

Mod-6, Mod-10

correct

Mod-50, Mod-10

Mod-10, Mod-50

Mod-50, Mod-6

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The hours counter is implemented using _____.

Answer (Please select your correct option)

- Mod-10 and Mod-2 counters
- A single decade counter and a flip-flop
- Only a single Mod-12 counter is required
- Mod-10 and Mod-6 counters

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Question No : 25 of 52

Marks: 1 (Budgeted Time 1 Min)

State Machine is a generic name given to _____



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Answer (Please select your correct option)

Sequential circuits

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Combinational circuits

Flip-flops

Counters

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Question No : 26 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is used to simplify the circuit that determines the next state.



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Answer (Please select your correct option)

State diagram

Next state table

State reduction

State assignment

correct

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The alternate solution for a demultiplexer-register combination circuit is _____

Answer (Please select your correct option)

Parallel in / Serial out shift register

Serial in / Parallel out shift register

Parallel in / Parallel out shift register

Serial in / Serial Out shift register

correct



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Question No : 28 of 52

Marks: 1 (Budgeted Time 1 Min)

In the following statement
Z PIN 20 ISTYPE 'reg.invert';
The keyword "reg.invert" indicates _____



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Answer (Please select your correct option)

- An inverted register input
- An inverted register input at pin 20
- Active-high Registered Mode output
- Active-low Registered Mode output

correct

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Question No : 29 of 52

Marks: 1 (Budgeted Time 1 Min)

A GAL is essentially a _____.

Answer (Please select your correct option)

- Non-reprogrammable PAL
- PAL that is programmed only by the manufacturer
- Reprogrammable PAL
- Reprogrammable PAL

correct



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Question No : 30 of 52

Marks: 1 (Budgeted Time 1 Min)

Which is not characteristic of a shift register?



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Answer (Please select your correct option)

Serial in/parallel in

correct

Serial in/parallel out

Parallel in/serial out

Parallel in/parallel out

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Question No : 31 of 52

Marks: 1 (Budgeted Time 1 Min)

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

Answer (Please select your correct option)

1100

0011

0000

1111

correct



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Question No : 32 of 52

Marks: 1 (Budgeted Time 1 Min)

A Nibble consists of ____ bits



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Answer (Please select your correct option)

2



4



8



16



correct

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Question No : 33 of 52

Marks: 1 (Budgeted Time 1 Min)

The address, from which the data is read, is provided by _____



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Answer (Please select your correct option)

Depends on circuitry

None of given options

RAM

Microprocessor

correct

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Question No : 34 of 52

Marks: 1 (Budgeted Time 1 Min)

FIFO is an acronym for _____



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Answer (Please select your correct option)

First In, First Out

correct

Fly in, Fly Out

Fast in, Fast Out

None of given options

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In order to synchronize two devices that consume and produce data at different rates, we can use _____



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Answer (Please select your correct option)

- Read Only Memory
- First In First Out Memory
- Flash Memory
- Fast Page Access Mode Memory

correct

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Question No : 36 of 52

Marks: 1 (Budgeted Time 1 Min)

If the FIFO Memory output is already filled with data then _____



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Answer (Please select your correct option)

- It is locked; no data is allowed to enter
- It is not locked; the new data overwrites the previous data.
- Previous data is swapped out of memory and new data enters
- None of given options

correct

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Question No : 37 of 52

Marks: 1 (Budgeted Time 1 Min)

The voltage gain of the Inverting Amplifier is given by the relation _____



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Answer (Please select your correct option)

$V_{out} / V_{in} = - R_f / R_i$

correct

$V_{out} / R_f = - V_{in} / R_i$

$R_f / V_{in} = - R_i / V_{out}$

$R_f / V_{in} = R_i / V_{out}$

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Question No : 38 of 52

Marks: 1 (Budgeted Time 1 Min)

The process of converting the analogue signal into a digital representation (code) is known as _____

Answer (Please select your correct option)

- Strobing
- Amplification
- Quantization
- Digitization

correct



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Question No : 39 of 52

Marks: 1 (Budgeted Time 1 Min)

Sampling of an analog signal produces :



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Answer (Please select your correct option)

- A series of impulses those are proportional to the frequency of the signal
- A series of impulses those are proportional to the amplitude of the signal
- Digital codes that represent the analog signal amplitude
- Digital codes that represent the time of each sample

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In a binary-weighted D/A converter, the resistors on the inputs :



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Answer (Please select your correct option)

- Limit the power consumption
- Prevent loading on the source
- Determine the weights of the digital inputs
- Determine the amplitude of the analog signal

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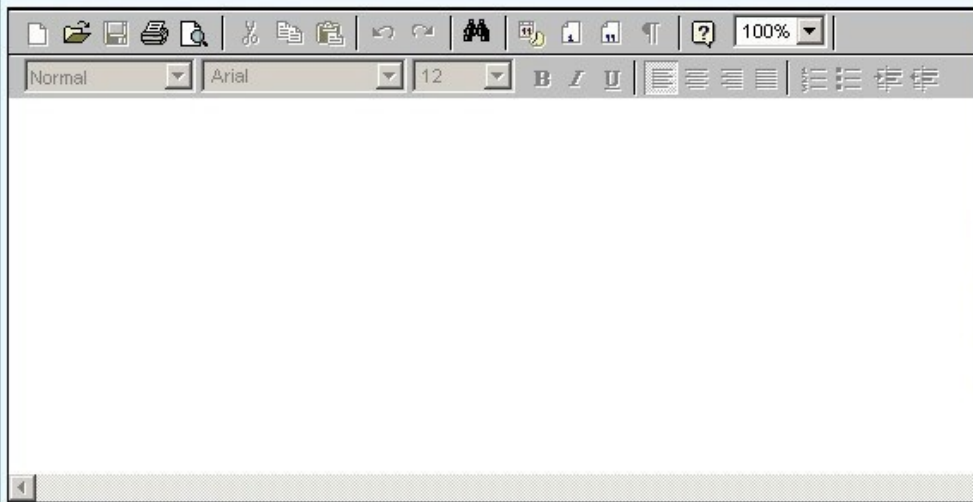
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Question No : 41 of 52

Marks: 2 (Budgeted Time 4 Min)

Write down the ABEL symbols that are used for NOT, AND, OR and XOR operations.

Answer ([Please click here to Add Answer](#))



The image shows a screenshot of a rich text editor interface. The toolbar includes icons for file operations (save, print, copy, paste), text formatting (bold, italic, underline), alignment (left, center, right, justified), and other functions like undo, redo, and help. The font settings are set to 'Normal', 'Arial', and size '12'. The text area below the toolbar is currently empty.



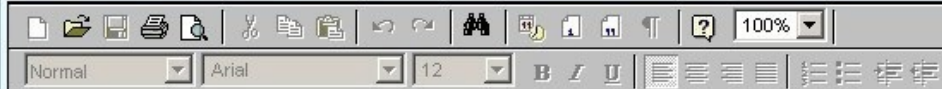
The advertisement features a circular image of two students, a man and a woman, sitting at a desk and working on laptops. The text 'HADI VU PAST PAPER' is written in a large, black, serif font, with 'PAST PAPER' repeated below it. At the bottom, the text 'MADE BY HADI' is written in a large, white, serif font on a black background.

Question No : 42 of 52

Marks: 2 (Budgeted Time 4 Min)

What is meant by state variable?

Answer ([Please click here to Add Answer](#))



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Question No : 43 of 52

Marks: 2 (Budgeted Time 4 Min)

The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. What will be the contents of register after two clock pulses?

Answer ([Please click here to Add Answer](#))



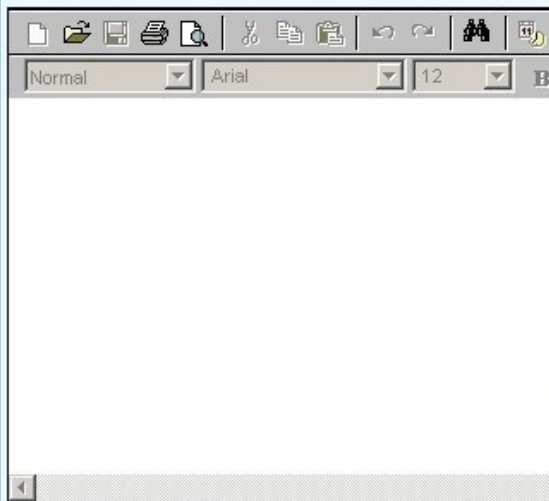
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What is the function of row and column decoders?

Answer ([Please click here to Add Answer](#))



A screenshot of a rich text editor toolbar. It includes icons for file operations (save, print, search), text editing (bold, italic, underline, strikethrough), and alignment. The font settings are set to 'Normal', 'Arial', and size '12'. A 'B' icon is visible on the right side of the toolbar.



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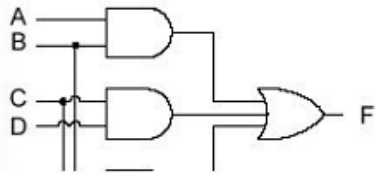
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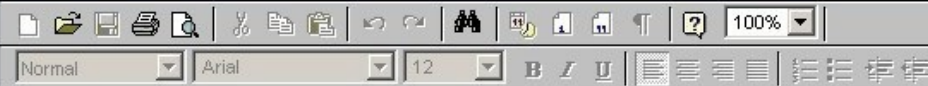
Question No : 45 of 52

Marks: 3 (Budgeted Time 6 Min)

From the circuit diagram given below derive the output expression.



Answer (Please [click here to Add Answer](#))



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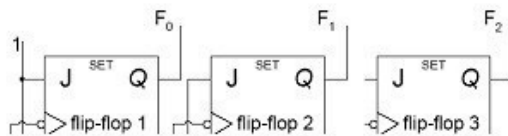
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Question No : 46 of 52

Marks: 3 (Budgeted Time 6 Min)

Following is an incomplete circuit of 3-bit Synchronous Down-counter, in which flip-flop 3 is left unconnected. Connect this 3rd flip-flop with flip-flop 2 in such a way that functionality of 3-bit Synchronous Down-counter is achieved.



Answer (Please [click here](#) to Add Answer)



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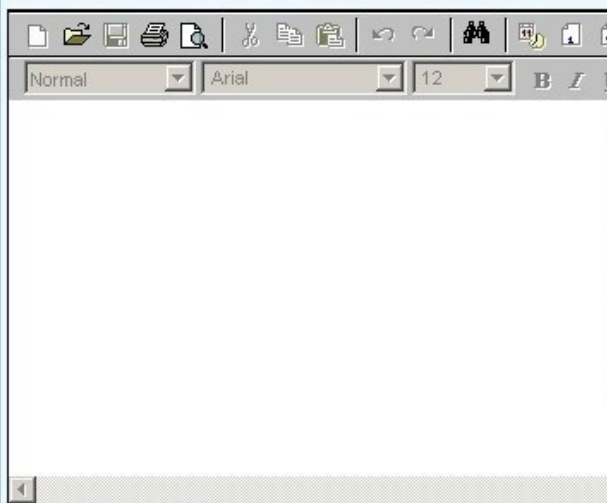
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Question No : 47 of 52

Marks: 3 (Budgeted Time 6 Min)

Suppose a 2 bit up-down counter having states "A, B, C, D". The counter counts upward when $X=1$ and downward when $X=0$. Write down IF-THEN-ELSE statements to show how present states change to next states and previous states.

Answer ([Please click here to Add Answer](#))



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Question No : 48 of 52

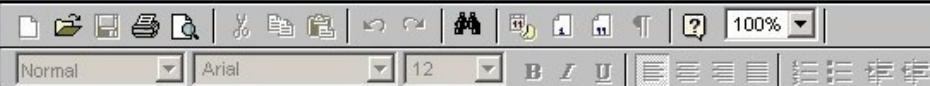
Marks: 3 (Budgeted Time 6 Min)

How DRAMs are different from SRAMs? Write three point of differences.



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Answer (Please [click here](#) to Add Answer)



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Question No : 49 of 52

Marks: 5 (Budgeted Time 10 Min)

Using K- map, minimize the following POS expression:

$$(A+B+C)(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})(\bar{A}+\bar{B}+C)$$

Answer (Please [click here](#) to Add Answer)



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Draw the state diagram of a 3-bit up-down counter. Use an external input X ; when X sets to logic 1, the counter counts downward otherwise counts upward.

Answer ([Please click here to Add Answer](#))



Normal



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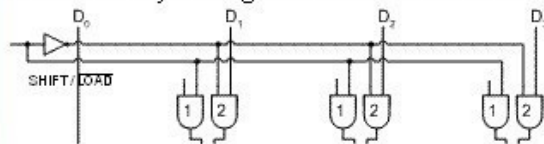
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Question No : 51 of 52

Marks: 5 (Budgeted Time 10 Min)

Given below is an incomplete circuit diagram of parallel in / serial out shift register, in which Q_0 , Q_1 , Q_2 , Q_3 , and Clock input are disconnected. Connect above mentioned connections in such a way that functionality of the given circuit is not affected.



Answer (Please [click here](#) to Add Answer)



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How a registered based LIFO memory is implemented? Draw block diagram of five bytes registered based LIFO memory.

Answer (Please [click here to Add Answer](#))



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