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CORRECT ANSWER SOLVED BY HADI
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(Final Term Past Paper)

MADE AND SOLVED BY TEAM HADI

WARNING: Team HADI is not responsible for any mistake or wrong answer. All students reading and using this document may check and confirm the answers at their own.



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Best of luck!



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Question No : 1 of 52

Marks: 1 (Budgeted Time 1 Min)

Excess-8 code assigns _____ to "-8"

Answer (Please select your correct option)

1110

1100

1000

0000



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Question No : 2 of 52

Marks: 1 (Budgeted Time 1 Min)

The Extended ASCII Code (American Standard Code for Information Interchange) represents _____ unique codes

Answer (Please select your correct option)

256

correct

255

128

127



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Question No : 3 of 52

Marks: 1 (Budgeted Time 1 Min)

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms



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Answer (Please select your correct option)

4

8

12

16

correct

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Question No : 4 of 52

Marks: 1 (Budgeted Time 1 Min)

The active high and active low inputs of 3-to-8 Decoder are as follows:



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Answer (Please select your correct option)

One active-high and the remaining two are active-low.



Two active-high and the remaining one is active-low.

All active high

All active low

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Question No : 5 of 52

Marks: 1 (Budgeted Time 1 Min)

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.



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Answer (Please select your correct option)

- 2-input, 4-bit
- 4-input, 8-bit
- 4-input, 16-bit
- 2-input, 8-bit

correct

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Question No : 6 of 52

Marks: 1 (Budgeted Time 1 Min)

GAL is an acronym for _____.



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Answer (Please select your correct option)

Generic Analysis Logic

Giant Array Logic

General Array Logic

Generic Array Logic

correct

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Question No : 7 of 52

Marks: 1 (Budgeted Time 1 Min)

74HC163 has two enable input pins which are _____ and _____.



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Answer (Please select your correct option)

ENP, ENT

correct

ENI, ENC

ENP, ENC

ENT, ENI

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Question No : 8 of 52

Marks: 1 (Budgeted Time 1 Min)

$A.(B + C) = A.B + A.C$ is an expression of _____



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Answer (Please select your correct option)

Demorgan's Law

Commutative Law

Distributive Law

Associative Law

correct

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Question No : 9 of 52

Marks: 1 (Budgeted Time 1 Min)

An 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

Answer (Please select your correct option)

1

correct

2

4

8



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Question No : 10 of 52

Marks: 1 (Budgeted Time 1 Min)

2's complement of -5 is _____



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Answer (Please select your correct option)

1000

1011

1100

1110

correct

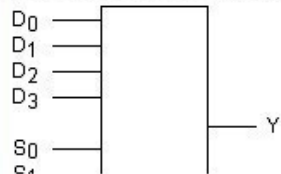
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Question No : 11 of 52

Marks: 1 (Budgeted Time 1 Min)

The device shown here is most likely a _____



Answer (Please select your correct option)

Comparator

Multiplexer

Demultiplexer

Parity generator

correct



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What will be output state when $J = 1$, $K = 0$ and CLR input is active?



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Answer (Please select your correct option)

- Q = 1 **correct**
- Q = 0
- Retains previous output state
- Toggle output

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Question No : 13 of 52

Marks: 1 (Budgeted Time 1 Min)

Which of the following statement is true?

Answer (Please select your correct option)

- Power consumption of TTL is higher than CMOS
- Power consumption of CMOS is higher than TTL
- Both TTL and CMOS have same power consumption
- Power consumption of both CMOS and TTL depends on number of gates in the circuit.

correct



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_____ counters as the name indicates are not triggered simultaneously.



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Answer (Please select your correct option)

Synchronous

Asynchronous

Positive-Edge triggered

Negative-Edge triggered

correct

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_____ is said to occur when multiple internal variables change due to change in one input variable.

Answer (Please select your correct option)

Race condition

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Propagation delay

Ripple effect

Clock skew



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Question No : 16 of 52

Marks: 1 (Budgeted Time 1 Min)

A 5-bit counter has a maximum _____ modulus.



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Answer (Please select your correct option)

10

16

25

32

correct

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Question No : 17 of 52

Marks: 1 (Budgeted Time 1 Min)

The Sequential circuit whose output depends on the current state and the input is known as _____.

Answer (Please select your correct option)

Moore Machine

Mealy Machine

Counter

Flip Flop

correct



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In _____, the \bar{Q} output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.

Answer (Please select your correct option)

Moore machine

Mealy machine

Johnson counter

Ring counter



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The power consumed by a flip-flop is defined by _____

Answer (Please select your correct option)

$P = I_{cc} \times R_{cc}$

$P = V_{cc} \times R_{cc}$

$P = V_{cc} \times I_{cc}$

$P = M_{cc} \times V_{cc}$

correct



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The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _____

Answer (Please select your correct option)

Pulse Stability time (PST)

Set-up time

Hold time

Pulse Interval time

correct



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Question No : 21 of 52

Marks: 1 (Budgeted Time 1 Min)

RCO Stands for _____



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Answer (Please select your correct option)

Reconfiguration Counter Output

Reconfiguration Clock Output

Ripple Counter Output

Ripple Clock Output

correct

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Question No : 22 of 52

Marks: 1 (Budgeted Time 1 Min)

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by using _____

Answer (Please select your correct option)

- T-Flop-Flop
- S-R Flop-Flop
- D-Flop-Flop
- J-K Flop-Flop



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correct

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Question No : 23 of 52

Marks: 1 (Budgeted Time 1 Min)

The Sequential circuit, whose output is determined by the current state only is known as _____.



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Answer (Please select your correct option)

Moore Machine

correct

Mealy Machine

Counter

Flip Flop

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Question No : 24 of 52

Marks: 1 (Budgeted Time 1 Min)

State Machine is a generic name given to _____



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Answer (Please select your correct option)

Sequential circuits

correct

Combinational circuits

Flip-flops

Counters

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Question No : 25 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is used to minimize the possible no. of states of a circuit.



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Answer (Please select your correct option)

State assignment

correct

State reduction

Next state table

State diagram

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Question No : 26 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is used to simplify the circuit that determines the next state.



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Answer (Please select your correct option)

State diagram

Next state table

State reduction

State assignment

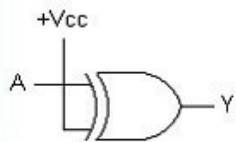
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Question No : 27 of 52

Marks: 1 (Budgeted Time 1 Min)

The output of this circuit is always _____.



Answer (Please select your correct option)

1

0

A

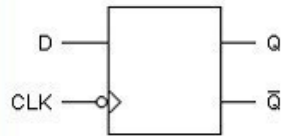
correct

\bar{A}



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Which of the following statement is true regarding above block diagram ?

Answer (Please select your correct option)

- Triggering takes place on the negative-going edge of the CLK pulse
- Triggering takes place on the positive-going edge of the CLK pulse
- Triggering can take place anytime during the LOW level of the CLK waveform
- Triggering can take place anytime during the LOW level of the CLK waveform



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correct

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Question No : 29 of 52

Marks: 1 (Budgeted Time 1 Min)

Which is not characteristic of a shift register?



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Answer (Please select your correct option)

Serial in/parallel in

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Serial in/parallel out

Parallel in/serial out

Parallel in/parallel out

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Question No : 30 of 52

Marks: 1 (Budgeted Time 1 Min)

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

Answer (Please select your correct option)

1100

0011

0000

1111

correct



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Question No : 31 of 52

Marks: 1 (Budgeted Time 1 Min)

A bidirectional 4-bit shift register is storing the nibble 1110. Its RIGHT/LEFT input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.

Answer (Please select your correct option)

1110

0111

1000

1001

correct



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Question No : 32 of 52

Marks: 1 (Budgeted Time 1 Min)

Smallest unit of binary data is a _____



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Answer (Please select your correct option)

Bit

correct

Nibble

Byte

Word

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Question No : 33 of 52

Marks: 1 (Budgeted Time 1 Min)

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines



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Answer (Please select your correct option)

Write Time

Refresh Time

Refresh Time

Access Time

correct

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Question No : 34 of 52

Marks: 1 (Budgeted Time 1 Min)

The high density FLASH memory cell is implemented using _____

Answer (Please select your correct option)

- 1 floating-gate MOS transistor
- 2 floating-gate MOS transistors
- 4 floating-gate MOS transistors
- 6 floating-gate MOS transistors

correct



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Question No : 35 of 52

The total amount of memory that is supported by any digital system depends upon _____

Answer (Please select your correct option)

The size of the address bus of the microprocessor

The organization of memory

The structure of memory

The size of decoding unit



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correct

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Question No : 36 of 52

Marks: 1 (Budgeted Time 1 Min)

The voltage gain of the Inverting Amplifier is given by the relation _____



Answer (Please select your correct option)

$V_{out} / V_{in} = - R_f / R_i$

correct

$V_{out} / R_f = - V_{in} / R_i$

$R_f / V_{in} = - R_i / V_{out}$

$R_f / V_{in} = R_i / V_{out}$

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Question No : 37 of 52

Marks: 1 (Budgeted Time 1 Min)

The process of converting the analogue signal into a digital representation (code) is known as _____



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Answer (Please select your correct option)

Strobing

Amplification

Quantization

Digitization

Correct

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Question No : 38 of 52

Marks: 1 (Budgeted Time 1 Min)

A flash A/D converter uses :

Answer (Please select your correct option)

Counters

Flip-flops

Op-amps

An integrator

correct



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_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.



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Answer (Please select your correct option)

- Resolution
- Accuracy
- Quantization
- Missing Code

correct

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Question No : 40 of 52

Marks: 1 (Budgeted Time 1 Min)

In a binary-weighted D/A converter, the resistors on the inputs :

Answer (Please select your correct option)

- Limit the power consumption
- Prevent loading on the source
- Determine the weights of the digital inputs
- Determine the amplitude of the analog signal



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correct

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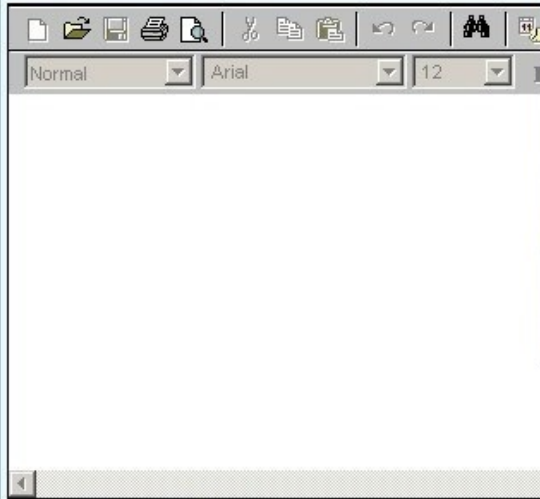
Question No : 41 of 52

Marks: 2 (Budgeted Time 4 Min)

Identify the following quantities as analog and digital.

- a) Pressure in a bicycle tire
- b) Number of students in a class
- c) Speed of a car
- d) Temperature

Answer ([Please click here to Add Answer](#))



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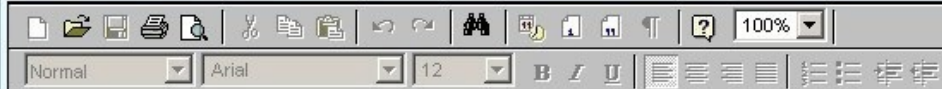
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Question No : 42 of 52

Marks: 2 (Budgeted Time 4 Min)

What is strobing method?

Answer (Please [click here](#) to Add Answer)



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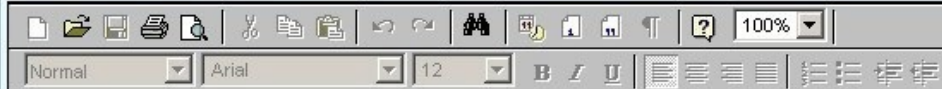
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Question No : 43 of 52

Marks: 2 (Budgeted Time 4 Min)

Write down any two applications of shift registers.

Answer (Please [click here](#) to Add Answer)



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Question No : 44 of 52

Marks: 2 (Budgeted Time 4 Min)

How many address bits are required for a 2048-bit memory organized as a 256 x 8 memory?

Answer ([Please click here to Add Answer](#))



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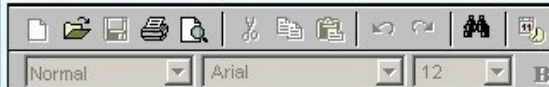
Question No : 45 of 52

Marks: 3 (Budgeted Time 6 Min)

Express each decimal number in binary as an 8-bit sign-magnitude number:

- (a) +29
- (b) -85

Answer ([Please click here to Add Answer](#))



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Question No : 46 of 52

Marks: 3 (Budgeted Time 6 Min)

How can we calculate the frequency of an unknown signal?

Answer ([Please click here to Add Answer](#))



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Question No : 47 of 52

Marks: 3 (Budgeted Time 6 Min)

Suppose a 2 bit up-down counter having states "A, B, C, D". The counter counts upward when $X=1$ and downward when $X=0$. Write down IF-THEN-ELSE statements to show how present states change to next states and previous states.

Answer (Please [click here](#) to Add Answer)



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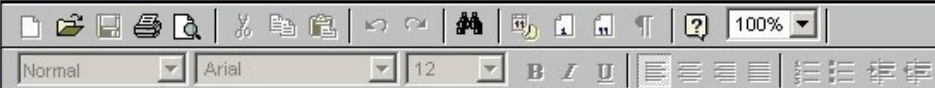
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Question No : 48 of 52

Marks: 3 (Budgeted Time 6 Min)

Answer (Please [click here](#) to Add Answer)



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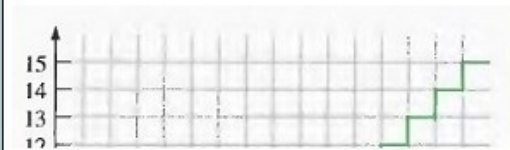
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Question No : 48 of 52

Marks: 3 (Budgeted Time 6 Min)

A 4-bit flash A/D converter is tested for faults. The resulting reconstructed analog output is shown below. Identify the problem and the most probable reason due to which this fault is occurred.



Answer (Please [click here to Add Answer](#))



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VU
PAST
PAPER

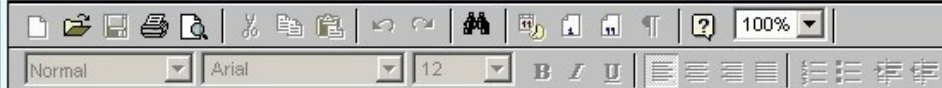
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Convert the following caveman numbers into decimal numbers, perform all the steps.

- a) $\Omega \uparrow \Sigma$
- b) $\uparrow \Delta \Delta \Sigma$

Answer ([Please click here to Add Answer](#))



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You are given the Next-state table of a moor machine, using this information draw the state diagram of the machine.

| Present State | | | Next State | | |
|----------------|----------------|----------------|----------------|----------------|----------------|
| Q ₂ | Q ₁ | Q ₀ | Q ₂ | Q ₁ | Q ₀ |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |

Answer ([Please click here to Add Answer](#))



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Question No : 51 of 52

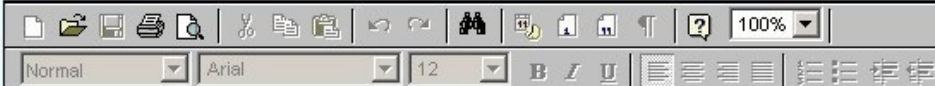
Marks: 5 (Budgeted Time 10 Min)

Make block diagram of Rotate Left Operation of a shift register and explain its working.



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Answer (Please [click here](#) to Add Answer)



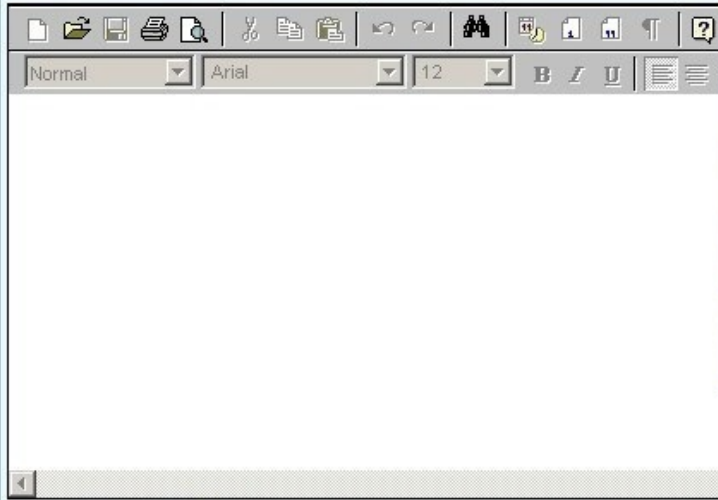
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Question No : 52 of 52

Analog to Digital converters exhibit different types of errors during their conversion operation. Explain at least two.

Answer ([Please click here to Add Answer](#))



A screenshot of a rich text editor interface. The top part shows a toolbar with various icons for text formatting and editing. Below the toolbar, there are dropdown menus for 'Normal' (text style), 'Arial' (font), and '12' (font size). To the right of these are buttons for bold (B), italic (I), and underline (U). Below the toolbar is a large, empty white text area.



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