CS302- Digital Logic & Design
Final Term Solved Subjective
Prepared by JUNAID MALIK

AL-JUNAID TECH INSTITUTE

www.vulmshelp.com

AL-JUNAID TECH INSTITUTE
0304-1659294
www.vulmshelp.com

VU LMS HELP
vulmshelp.com

Language Courses Training Available

I'm providing paid courses in different languages within 3 Months,Certificate will be awarded after completion.

- HTML
- CSS
- JAVASCRIPT
- BOOTSTRAPS
- JQUERY
- PHP MYSQL
- NODES.JS
- REACT JS

LMS Handling Services

LMS Activities Paid Task

Assignments 95% Results

Quizes 95% Results

GDB 95% Results

For CS619 Project Feel Free To Contact With Me

Ph# 0304-1659294
Email: junaidfazal08@gmail.com

AL-JUNAID TECH INSTITUTE

Question No.1

In the highest frequency component in an analog signal is 20 KHz, what is the minimum sample frequency (Marks 2)

Answer:-

In the highest frequency component in an analog signal is 20 KHz, and minimum sample frequency is 40 KHz.

Question No.2

Write down the ABEL symbols that are used for NOT, AND, OR and XOR operations. (Marks 2)

Answer:- Page 201

Logic Operation	ABEL Symbol
NOT	!
AND	&
OR	#
XOR	$

Question No.3

Differentiate between Moore machine and Mealy machine. (Marks 2)

Answer:- Page 318

The Sequential circuit whose output depends on the current state and the input is known as Mealy Machine.

Sequential circuit whose output is determined by the current state only is known as Moore Machine.

Question No.4

How many bytes will be there in 16K x 8 memory? (Marks 2)

Answer:- Page 395

A 16 K x 8 memory, stores 16K bytes or 16 x 1024 = 16384 bytes or 131072 bits.

Question No.5

How many address bits are required for a 2048-bit memory organized as a 256 x 8 memory? (Marks 3)

Question No.6

Explain Rotate Right Operation of shift register with the help of Diagram. (Marks 3)

Answer:- Page 354

0304-1659294
www.vulmshelp.com

The serial output of the register is connected to the serial input of the register. By applying clock pulses data is shifted right. The data shifted out of the serial out pin at the right hand side is re-circulated back into the shift register input at the left hand side. Thus the data is rotated right within the register.

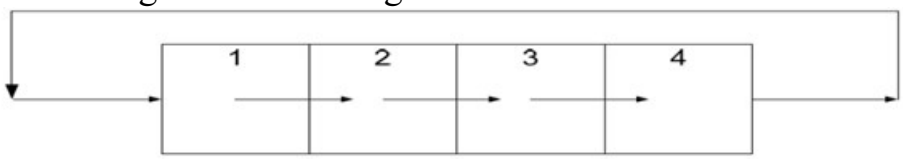


Figure 34.14 Rotate Right Operation

Question No.7

Difference between State Assignment and State Reduction process. (Marks 3)

Answer:- (Page 332 & 335)

1. In state Reduction A state diagram show the sequence of current and next states through which the state machine sequences while in State Assignment Each state in a sequential circuit is identified by a unique combination of binary bits.
2. In state Reduction the transition from a current state to the next state is determined by current state and the inputs while in State Assignment the states can be selected to allow minimum bit changes when changing from one state to the other.
3. State Assignment results in simpler combinational circuits that determine the next state while Reduction in the number of state results in fewer flip-flops and a simpler circuit.

Question No.8

Explain Full-Adder Sum and Carry out Boolean Expression. (Marks 3)

Answer:- (Page 135)

Full-Adder Sum & Carry Out Boolean Expressions

The Sum and Carry Out expressions of the Full-Adder can be determined from the function table. The Full-Adder Sum and Carry Out outputs are defined by the expressions

$$Sum = ABC + ABC + ABC + ABC$$
$$Sum = A(BC + BC) + A(BC + BC)$$
$$Sum = A(B \oplus C) + A(B \oplus C)$$
$$Sum = A \oplus B \oplus C$$

$$CarryOut = ABC + ABC + ABC + ABC$$
$$CarryOut = C(AB + AB) + AB(C + C)$$
$$CarryOut = C(A \oplus B) + AB$$

Question No.9

Explain Latches in your own words.(Marks 5)

Answer:- (Page 218)

A latch is a temporary storage device that has two stable states. A latch output can change from one state to the other by applying appropriate inputs. A latch normally has two inputs, the binary input combinations at the latch input allows the latch to change its state. A latch has two outputs Q and its complement Q(bar). The latch is said to be in logic high state when Q=1 and Q(bar)=0 and it is in the logic low state when Q=0 and Q(bar)=1. When the latch is set to a certain state it retains its state unless the inputs are changed to set the latch to a new state. Thus a latch is a memory element which is able to retain the information stored in it.

Question No.10

Differentiate between synchronous and asynchronous memory. (Marks 5)

Answer:- (Page 406)

In the Asynchronous memory the various input signals are asynchronous and are not tied to the clock, whereas in the Synchronous memory all the inputs are synchronized with respect to the clock and are latched into their various registers on an active clock pulse edge.

Question No.11

Draw state diagram of Moore machine.
(Marks 5) **Answer:- (Page 338)**

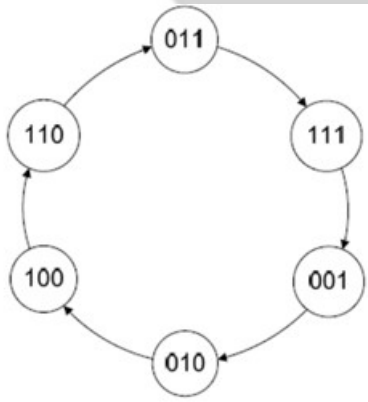


Figure 33.1 State diagram of a Moore Machine

AL-JUNAID TECH INSTITUTE

Question No:12 (Marks: 2)

Write down at least two applications of a shiftregister.

Answer:- (Page 356)

The two applications of the shift registers are

1. Serial to Parallel converter
2. Keyboard encoder

Question No:13 (Marks: 2)

Explain memory expansion process.

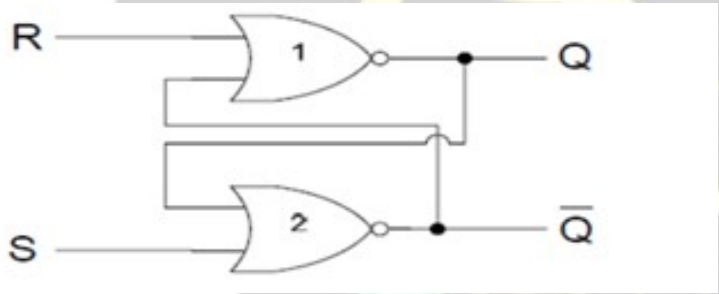
Answer:- (Page 430)

Computer and Digital systems have the capability to allow RAM memory to be expanded as the needed arises by inserting extra memory in dedicated memory sockets on the computer motherboard.

Question No:14 (Marks: 2)

Draw the NOR based S-R Latch

Answer:- (Page 220)



Question No:15 (Marks: 3)

Explain Rotate Left Right Operation with the help of diagram.

Answer:- (Page 354)

AL-JUNAID TECH INSTITUTE
0304-1659294
www.vulmshelp.com

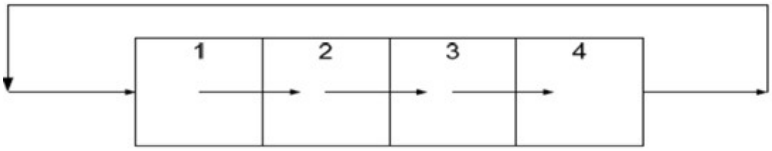


Figure 34.14 Rotate Right Operation

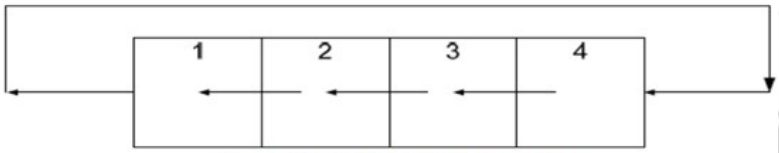
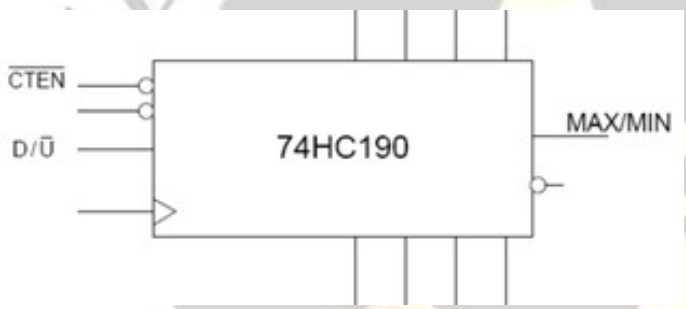


Figure 34.15 Rotate Left Operation

Question No:16 (Marks: 3)

You are given the block diagram of 74HC190 integrated circuit up/down counter, explain the function of labeled inputs/outputs.



Answer:-(Page 295)

1. Active-low CTEN counter enable input
2. D/U the count down/up input. When the input is set to logic 1, the counter counts down and when the input is set to logic 0, the counter counts up
3. The MAX/MIN output that is set to high when the terminal count 1001 is reached when counting up or when the terminal count 0000 is reached when counting down. The MAX/MIN output is logic high for one complete cycle when a terminal count is reached.

Question No:17 (Marks: 5)

Explain Memory Select or Enable Signals

Answer:- (Page 397)

In a computer system there are more than one memory chips to store program information. At any particular instant a read or write operation is carried out on a single addressable location. The unique location can only be accessed in one of the several memory chips, thus a single memory chip has to be selected before a read or write operation can be carried out. All

memory chips have a chip enable or chip select signal which has to be activated before the memory can be accessed.

Question No:18 (Marks: 5)

Explain the implementation of First In First Out (FIFO) Memory by using RAM.

Answer:- (Page 427)

Shift register based FIFO memory is used in digital systems designed for specific applications where small sized buffers are used to allow transfer of data between two devices operating at different data rates. Such digital systems either have no RAM or very small RAM for storing variables. Computers implement FIFO memory by reserving a part of their RAM memory for use as buffers. The Keyboard buffer for example is implemented by reserving a part of the RAM. When RAM is used as FIFO memory, two registers are used to point to the FIFO Buffer Out and Buffer In respectively. The two registers hold the addresses of the locations of the Buffer Out and Buffer In respectively, which are updated as new data is written into the buffer and previous data is read out from the FIFO buffer. Implementation of the FIFO buffer in RAM is usually takes the form of a circular buffer.

Question No:19 (Marks: 5)

Explain application of demultiplexer

Answer:- (Page 178)

Demultiplexer is used to connect a single source to multiple destinations. One use of the Demultiplexer is at the output of the ALU circuit. The output of the ALU has to be stored in one of the multiple registers or storage units. The Data input of the Demultiplexer is connected to the output of the ALU. Each output of the Demultiplexer is connected to each of the multiple registers. By selecting the appropriate output data from the ALU is routed to the appropriate register for storage.

The second use of the Demultiplexer is the reconstruction of Parallel Data from the incoming serial data stream. Serial data arrives at the Data input of the Demultiplexer at fixed time intervals. A counter attached to the Select inputs of the Demultiplexer routes the incoming serial bits to successive outputs where each bit is stored. When all the bits have been stored, data can be read out in parallel.

Question No: 20 (Marks: 2)

Explain the erase operation in context of Flash Memory.

Answer:- (Page 421)

During the erase operation charge is removed from the memory cell. A sufficiently large positive voltage is applied at the source with respect to the control gate. The voltage applied across the control gate and source is opposite to the voltage applied during programming. If charges are present on the gate, the positive voltage supply at the source attracts the electrons depleting the gate. A FLASH memory is erased prior to programming.

Question No.21

How can a serial in/parallel out register be used as a serial in/serial out register?

Question No.22

Explain the next-state table with the help of a table for any sequential circuit?

Answer:- (Page 306)

Once the state diagram of the sequential circuit is defined, a Next-State Table is derived which lists each present state and the corresponding next state. The next state is the state to which the sequential circuit switches when a clock transition occurs.

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Question No.23

What is meant by Non-Monotonicity of Digital to Analog converter?

Answer:- (Page 460)

if the D/A converter outputs a lower voltage than its preceding output voltage the converter is said to exhibit non-monotonic behavior.

Question No.24

Write down at least two functions of a register.

Answer:- (Page 306)

0304-1659294 www.vumshelp.com

Technically, a register performs two basic functions. It stores data and it moves or shifts data. The shifting of data involves shifting of bits from one flip-flop to the other within the register or moving data in and out of the register. The shift operation of the binary data is carried out by applying clock signals. Several different kinds of shift operations can be identified.

Question No.25

You are given the Next-state table of a Moore machine, using this information draw the state diagram of the machine.

Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	1	1	1	1	1
1	1	1	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	1	0
1	1	0	0	1	1

Answer:-(Page 338)

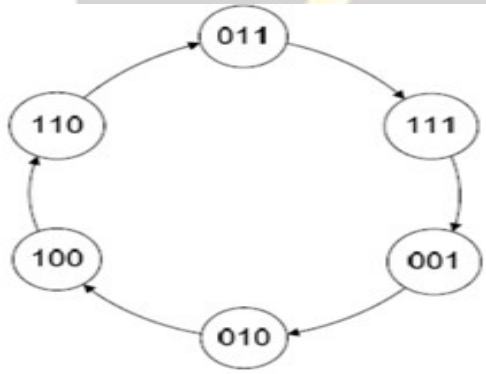


Figure 33.1 State diagram of a Moore Machine

Question No.26

Define the term "Variable" in context of Boolean algebra.

Answer:- (Page 71)

A variable is a symbol usually an uppercase letter used to represent a logical quantity.

A variable can have a 0 or 1 value.

Question No.27

A general sequential circuit consists of a combinational circuit and memory elements. How this Memory element is implemented.

Answer:- (Page 318)

A general Sequential circuit consists of a combinational circuit and a memory element. The memory element is made of a set of n flip-flops all connected to a a common clock. The n flip flops store 2n states. The flip-flops change their current state to the next state on each clock transition. The next state is determined by the current state and the external input. The output of the State Machine is determined by the current state and external input. The inputs to the memory which allow the memory to change its state on a clock transition are known as excitation inputs or excitation variables.

Question No.28

what is meant by Monotonicity of Digital to Analog converter?

Answer:- (Page 460)

The output of the D/A converter should give an increasing analogue voltage output when the binary input is varied between its minimum and maximum values.

Question No.29

Explain Programmable Logic Devices?

Answer:-(Page 179)

Programmable Logic Devices are used in many applications to replace the Logic gates and MSI chips. PLDs save circuit space and reduce and save the cost of components in a Digital Circuit. PLDS consists of Arrays of AND gates and OR gates that can be programmed to perform specific functions.

0304-1659294
www.vulmshelp.com

Question No.30

How many clock pulses are required to enter a byte of data serially into an 8-bit shift register? 2 **Answer:-**

8 clock pulses are required to enter a byte of data serially into an 8- bit shift register

Question No.31

How can calculate the frequency of an unknown signal?

Answer:-(Page 301)

The frequency of the unknown signal can be calculated by counting the number of clock pulses of the unknown signal and dividing the count number by the time interval in which the clock pulses are counted,

Question No.32

Write the drawbacks of 16-bit ALU without look-Ahead carry circuit?

Question No.33

How many address bit are required for a 2048-bit memory organized as a 256*8 memory?

Question No.34

Differentiates between Memory capacity and Memory Density?

Answer:- (Page 395)

Each memory array has a maximum capacity to store information in the form of bits. Memory density on the other hand specifies the number of bits stored per unit area. More the number of bits stored in a unit area more dense the memory, that is, more bits are stored in less space.

Question No.35

Explain Memory Select or Enable signal?

Answer:- (Page 397)

In a computer system there are more than one memory chips to store program information. At any particular instant a read or write operation is carried out on a single addressable location. The unique location can only be accessed in one of the several memory chips, thus a single memory chip has to be selected before a read or write operation can be carried out. All memory chips have a chip enable or chip select signal which has to be activated before the memory can be accessed.

Question No.36

Explain state Assignment Process.

Answer:-(Page 335)

Each state in a sequential circuit is identified by a unique combination of binary bits. Unless the output of the sequential is directly taken form the flip-flop outputs such as counters, the states can be selected to allow minimum bit changes when changing from one state to the other. Keeping the bits changes to minimum when changing from one state to the next, results in simpler combinational circuits that determine the next state.

Question No: 37 (Marks: 2)

Some of the counters (e.g. 74HC163) are called pre-set counters. why?

Answer:-

74HC163) are called pre-set counters because A counter set in advance to stop or produce output once a specific count has been reached.

Question No: 38 (Marks: 2)

How many bytes will be there in 32 K x 8 memory?

Answer:- (Page 395)

A 32 K x 4 memory stores 32K nibbles or 32 x 1024 = 32768 nibbles

Question No: 39 (Marks: 3)

Differentiate between truth table and next-state table.

Question No.40

Two state assignments are given in the table below. Identify which state assignment is best and why?

States	State assignment 1	State assignment 2
A	00	00
B	01	01
C	11	10
D	10	11

Question No.41

Convert the hexadecimal number 7AB1 into binary numbers. Write down all the steps. **Answer:- (Page 27)**

Replacing each Hexadecimal digit by its 4-bit binary equivalent

7= 0111, A= 1010, B=1011, 1= 0001 So, 7AB1 = 0111101010110001

Question No.42

Explain grouping of cells in k-map. **Answer:- (Page 90)**

Groups are formed on the basis of 1s (Minterms) or 0s (maxterms). A group is selected to have maximum number of cells of Minterms or Maxterms, keeping in view that the size of the group should be a power of 2. The idea is to form minimal number of largest groups that uniquely cover all the cells, thereby ensuring that all minterms or maxterms are included.

Question No.43

Provide some of guidelines for selection of state assignment. 3

Answer:-

- Choose an initial coded state into which the state machine (sequential circuit) can easily be forced to reset (000 or 111)
- Minimize the State Variables that change on each transition
- Maximize the number of state variables that don't change in a group of related states
- If there are unused states, then choose the best state variable combinations to achieve the first three goals.

Question No.44

Discuss at least one difference in Johnson and ring Counter

Answer:-(Page 355)

The Ring Counter is similar to the Johnson counter, except that the Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

Question No.45

Three types of error while converting Analogue signal into digital

Answer:

1. Missing Code
2. Incorrect Code
3. Offset Error

Question No.46

Explain memory read operation with help of example 5

Answer:- (page 397)

Memory Read operation is carried out by first selecting the memory chip by activating the Memory Select signal. The Read signal is asserted to configure the memory circuitry for reading data from the memory. An address (100) is applied on the Address Lines. The internal address decoder of the memory decodes the address and selects one unique row from which data is read. Figure 39.4.

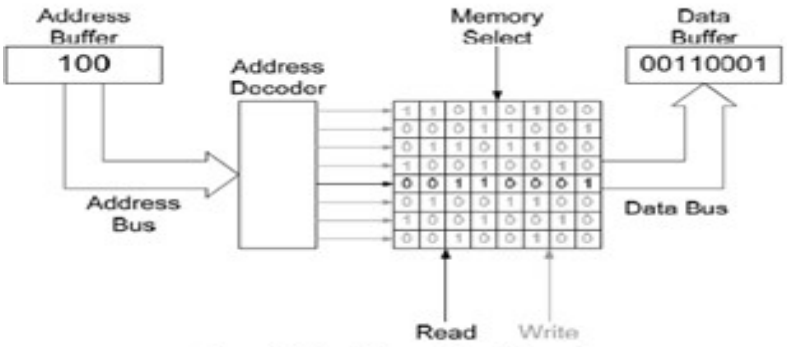


Figure 39.4 Memory Read Operation

The address of the location in the memory from which data is to be read is supplied by the microprocessor. The microprocessor stores the address in its address buffer. The data read from the memory is stored in a data buffer inside the microprocessor. In the diagram shown, a microprocessor places an address 100 on its external address bus connected to the address lines of the memory. The internal address decoder of the memory decodes the address 100 and activates a row select line which selects the row location 4. The data (00110001) at the location is read from the memory and placed on the data bus where it is latched by the microprocessor and stored in its data buffer.

Question No.47

Explain flesh analogue to digital converter. marks 5

Answer:- (Page 447)

The Flash A/D converter is based on a resistor potential divider, where multiple resistors of identical value form a voltage divider. A reference voltage is applied at one end of the potential divider which divides the voltage equally across all the resistors. The input analogue voltage is applied at the non-inverting inputs of a set of Op-Amp based comparators. The inverting input of each comparator is connected to the resistive voltage divider which provides reference voltages for all the comparators. If the input voltage is larger than the reference voltage the output of the comparator is logic high otherwise it is logic low. The outputs of all the comparators are connected to the input of a priority encoder which converts the comparator outputs to a binary coded equivalent value.

Question No.48

Briefly explain address multiplexing in DRAM. marks5

Answer:- (Page 410)

DRAM chips use address multiplexing to reduce the number of address lines by half. The address required to select a memory location is split into row and column addresses. To access a DRAM location for reading or writing of information the row address is first applied at the

address lines. The row address is latched by the Row Address Latch of the DRAM memory chip. The column address is applied next at the same address lines. The column address is latched by the Column Address Latch. Two signals RAS and CAS are used as strobe signals to control the Row Address and Column Address latches respectively. The external address lines are multiplexed as the same set of address lines are used to apply the row address and the column address at different time instances. The outputs of the Row Address Latch and the Column Address Latch are connected to the Row and Column Decoders which select a single row and column line selecting the storage cell to be accessed.

Question No.49

Explain READ Write signal used for memory. Marks 3

Answer:- (Page 396)

Read/Write signals are required to configure the memory for read and write operation. Memory chips have a single Read/Write signal. When the signal is set to high it allows data to be read from the memory. When the signal is set to low data is written into the memory. Some memory chips have two separate Read and Write signals. The read and write signals are separately asserted to control the Read and Write operation.

Question No.50

What is difference between PROM and ROM. Marks 3

Answer:-

The difference between a PROM and a ROM (**r**ead-**o**nly **m**emory) is that a PROM is manufactured as blank memory, whereas a ROM is programmed during the manufacturing process. To write data onto a PROM chip, you need a special device called a PROM programmer or PROM burner. The process of programming a PROM is sometimes called burning the PROM.

0304-1659294
www.vulmshelp.com

Question No.51

Making decade counter by cascading two 74HC163. 05

Question No.52

Explain don‟s care condition.

Answer:- (Page 96)

Function Tables represent the function by listing all the possible inputs and marking the corresponding outputs with 1s and 0s. Thus a circuit having four inputs can be described by a 4-variable function table having 16 possible input combinations. For each of the 16 possible

input conditions the corresponding output bits are marked as 1s and 0s depending upon the minterms or maxterms. It is however, possible that out of the 16 possible input combinations, three input combinations never occur. Since these three input combinations never occur so should their corresponding outputs be marked as 0s or 1s? Since these inputs never care therefore we don't need to worry about the output of these input states. They are considered to be don't care conditions.

Question No: 53 (Marks: 5)

Performance characteristics of D/A converters are determined by five parameters. Name them.

Answer:- (Page 460)

Performances characteristics of D/A converters are determined by five parameters are:
1. Resolution 2. Linearity 3. Monotonicity 4. Setting time 5. Accuracy

Question No.54

Give advantages of Counters are available in integrated circuits? (Marks 2)

Question No.55

Successive approximation counter have a fixed consecutive time Is tarha ka qs tha (Marks 2)

Question No.56

How many states in 8-bit Johnson counter? (Marks 2)

Answer:-(Page 354)

The sequence of states that are implemented by a n-bit Johnson counter are 2n So, 8 bit Johnson counter has 2*8 = 16 states

Question No.57

Diff b/w truth table and next state table
(Marks 3)

Question No.58

How hexadecimal number is converted into binary number give one example? (Marks 3)

Answer:-(Page 28)

Converting from Hexadecimal back to binary is also very simple. Each digit of the Hexadecimal number is replaced by an equivalent binary string of 4-bits. FD13 Hexadecimal Number 1111 1101 0001 0011 Replacing each Hexadecimal digit by its 4-bit binary equivalent

0304-1659294
www.vulmshelp.com

Programmable Logic Devices are based on a programmable AND-OR gate array which are programmed to implement any function in the SOP form. The output of the AND-OR gate array can be directly used as a combinational circuit output. Provision is there to connect the output of the AND-OR gate array to a D-flip-flop for Sequential circuit operation. An FPGA is a more flexible device than PLDs as instead of a single AND-OR gate array, an FPGA device contains multiple logic blocks that can be individually programmed to perform different functions. Each Logic Block is connected to other blocks through row and column interconnects that can be programmed to connect any Logic block to another.

Question No: 59 (Marks: 5)

Differentiate between synchronous and asynchronous RAM.

Answer:- (Page 406)

Synchronous RAM is very similar to the Asynchronous RAM, in terms of the memory array, the address decoders, read/write and enable inputs. In the Asynchronous memory the various input signals are asynchronous and are not tied to the clock, whereas in the Synchronous memory all the inputs are synchronized with respect to the clock and are latched into their various registers on an active clock pulse edge.

Question No: 60 (Marks: 2)

Draw the Truth-Table of NOR based S-R Latch

Answer:- (Page 222)

Input		Output
S	R	Qt+1
0	0	Q_t
0	1	0
1	0	1
1	1	invalid

Table 22.3 Truth-Table of NOR based S-R Latch

0304-1659294
www.vulmshelp.com

Question No: 61 (Marks: 2)

Two state assignments are given in the table below. Identify which state assignment is best and why?

States	State Assignment 1	State Assignment 1
A	00	00

B	01	01
C	11	10
D	10	11

Question No: 62 (Marks: 3)

Given the following statement used in PLD programming:
Y PIN 23 ISTYPE „com";
Explain what does this statement mean?

Answer:- (Page 360)

The statement describes Y available at output pins 23. The Y variable is a 'Combinational' output available directly from the AND-OR gate array output. The active-low or active-high output of the Registered Mode can also be specified in the declaration statement

Question No: 63 (Marks: 3)

Explain dynamic RAM in your own words.

Answer:-

Dynamic random-access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1. Since capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory.

Question No.64 (Mark s: 2)

Define quantization process.

Answer:- (Page 444)

The process of converting the analogue signal into a digital representation (code) is known as quantization

Question No.65 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer and 2-to-4 Binary Decoder?

Answer:- (Page 178)

The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit figure 16.10. Assuming the select inputs I1 and I0 are set to 1 and 0 respectively. The O2 output is set to 1 if the Data input is 1 or it is set to 0 if the Data input is 0.

Question No.67 (Marks: 2)

Suppose a 2 bit up-counter, having states "A, B, C, D". Write down GOTO statements to show how present states change to next states.

Question No.68 (Marks: 3)

Name three Operations that can be performed on FLASH Memory

Answer:- (Page 420)

FLASH Memory operations are classified into

- Programming Operation
- Read Operation
- Erase Operation

AL-JUNAID TECH INSTITUTE
0304-1659294
www.vulmshelp.com