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## CS 302 GRAND QUIZ

Sr No.	MCQS QUESTION	ANSWER
1.	The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.	Faster
2.	In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.	NAND, NAND
3.	Why demultiplexer is called a data distributor?	Single input to Single Output
4.	_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.	Combinational Input
5.	The n flip-flops store _____ states.	$2^n$
6.	The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.	NAND
7.	The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacents 1s are detected in the input, the output is set to high.	1
8.	As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.	Top
9.	In memory write cycle, the time for which the WE signal remains active is known as the _____.	Write pulse

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		width
10.	You have to choose suitable option when your timer will reset by considering this given code: TRSTATE.CLK = clk; TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);	NSY2 or EWY2
11.	Two signals _____ and _____ provide the timing inputs to the State Machine.	PTIME and QTIME
12.	PALs tend to execute _____ logic.	SOP
13.	Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration TWD?	WE
14.	Memory is arranged in _____.	two-dimensional manner
15.	The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.	High
16.	Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.	8 AND

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17.	The maximum value, represented by a single hexadecimal digit is _____.	"F"
18.	The _____ input overrides the _____ input.	Asynchronous, synchronous
19.	A SOP expression can be implemented by an _____ combination of gates.	AND-OR
20.	The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.	AND
21.	The Transition table is very similar to the _____ table.	State
22.	The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.	Truth Table
23.	A 3-variable karnaugh map has	eight cells
24.	If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.	Same
25.	Adding two octal numbers "36" and "71" result in _____.	127

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26.	Consider $A=1, B=0, C=1$ . A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.	One
27.	Subtractors also have output to check if 1 has been _____.	Primed
28.	Which of the following Output Equations determines the output of the State Machine?	$MAX = Q_0Q_1EN$
29.	When the transmission line is idle in an asynchronous transmission	It is set to logic high
30.	UVERPROM is stands for	Ultra-Violet
31.	The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.	4
32.	Select the mode of programming in which GAL16V8 can be programmed:	All of the given
33.	The $CONSTATE.CLK = \text{Clock}$ is used to indicate that the _____ state variables change on a clock transition.	CONSTATE
34.	The domain of the expression $AB'CD + AB' + C'D + B$ is	A, B, C and D

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35.	The ROM used by a computer is relatively _____ as it stores few bytes of code used to Boot the Computer system on power up.	Small
36.	_____ Counters as the name indicates are not triggered simultaneously.	Synchronous
37.	The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.	Three
38.	The output of a NAND gate is _____ when all the inputs are one.	Zero
39.	For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.	1
40.	A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.	True
41.	Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.	Shift Registers
42.	The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.	XOR, NAND
43.	A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:	1111

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44.	Which of the following is a volatile memory?	DRAM
45.	The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.	REQ1
46.	The AND Gate performs a logical _____ function.	Division
47.	Implementation of Latch is required almost _____ transistor.	Six
48.	Which one flip-flop has an invalid output state?	SR
49.	Divide-by-32 counter can be achieved by using	Flip-Flop and DIV 32
50.	The terminal count of a 4-bit binary counter in the UP mode is _____.	1100
51.	In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.	True
52.	The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.	Four
53.	Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.	RAM

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54.	An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.	Q output of all flip-flops to clock input of next flip-flops
55.	In DRAM read cycle R /W signal is activated to read data which is made available on the _____ data line.	D(OUT)
56.	Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.	256
57.	8-bit parallel data can be converted into serial data by using _____ multiplexer.	8-to-1
58.	If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.	1001
59.	Canonical form is a unique way of representing _____.	SOP
60.	A NOR based S-R latch is implemented using _____ gates instead of _____ gates.	NOR, NAND
61.	Cin is part of _____ Adder.	Full
62.	Flash memory Operation are classified into _____ different operation.	Two

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63.	GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.	row, column
64.	In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.	7.8 microsec
65.	In the keyboard encoder, how many times per second does the ring counter scan the key board?	650 scans/second
66.	Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.	Negative-OR, Negative-AND
67.	If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.	1
68.	The 64-cell array organized as 8 x 8 cell array is considered	as an 8 byte memory
69.	The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.	Synchronous
70.	PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.	PLDs

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71.	For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.	None of the given
72.	A multiplexer with a register circuit converts	Parallel data to serial
73.	The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.	Four
74.	Which of the following Output Equations determines the output of the State Machine?	MAX = Q0Q1EN
75.	8-bit parallel data can be converted into serial data by using _____ multiplexer.	8-to-1
76.	You have to choose suitable option when your timer will reset by considering this given code: TRSTATE.CLK = clk; TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);	NSY2 or EWY2
77.	UVERPROM is stands for	Ultra-Violet
78.	In memory write cycle, the time for which the WE signal remains active is known as the _____.	Write pulse width

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79.	PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.	PLDs
80.	The Transition table is very similar to the _____ table.	State
81.	Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.	Negative-OR, Negative-AND
82.	The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.	CONSTATE
83.	Adding two octal numbers "36" and "71" result in	127
84.	Divide-by-32 counter can be achieved by using	Flip-Flop and DIV 32
85.	A multiplexer with a register circuit converts	Parallel data to serial
86.	_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.	Combinational Input
87.	Memory is arranged in _____.	two- dimensional

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		manner
88.	Implementation of Latch is required almost _____ transistor.	Six
89.	In DRAM read cycle R /W signal is activated to read data which is made available on the _____ data line.	D(OUT)
90.	Why demultiplexer is called a data distributor?	Single input to Single Output
91.	The maximum value, represented by a single hexadecimal digit is _____.	"F"
92.	Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.	RAM
93.	The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.	REQ1
94.	In a sequential circuit the next state is determined by _____ and _____	Current state and external input
95.	The divide-by-60 counter in digital clock is implemented by using two cascading counters:	Mod-6, Mod-10

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96.	The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop	Hold time
97.	74HC163 has two enable input pins which are _____ and _____	ENP, ENT
98.	_____ is said to occur when multiple internal variables change due to change in one input variable	Race condition
99.	The _____ input overrides the _____ input.	Asynchronous, synchronous
100.	A decade counter is _____.	Mod-10 counter
101.	In asynchronous transmission when the transmission line is idle, _____	It is set to logic high
102.	A Nibble consists of _____ bits.	4

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103.	Excess-8 code assigns _____ to "-8"	0000
104.	The voltage gain of the Inverting Amplifier is given by the relation _____	$V_{out} / V_{in} = -R_f / R_i$
105.	LUT is acronym for _____	Look Up Table
106.	The three fundamental gates are _____	NOT, OR, AND
107.	The total amount of memory that is supported by any digital system depends upon _____	The size of the address bus of the microprocessor
108.	Stack is an acronym for _____	LIFO memory
109.	Addition of two octal numbers "36" and "71" results in _____	127
110.	_____ is invalid number of cells	J-K input

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	in a single group formed by the adjacent cells in K-map_____ is one of the examples of synchronous inputs.	
111.	_____ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.	Clock Skew
112.	A GAL is essentially a _____.	Reprogrammable PAL
113.	_____, all the columns in the same row are either read or written.	FAST Mode Page Access
114.	In order to synchronize two devices that consume and produce data at different rates, we can use _____.	Fist In First Out Memory
115.	A positive edge-triggered flip-flop changes its state when _____.	Low-to-high transition of clock

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116.	A frequency counter _____	Counts no. of clock pulses in 1 second
117.	In a sequential circuit the next state is determined by _____ and _____	Input and clock signal applied
118.	Given the state diagram of an up/down counter, we can find _____	The next state of a given present state
119.	The total amount of memory that is supported by any digital system depends upon _____	The size of the address bus of the microprocessor
120.	The expression $F=A+B+C$ describes the operation of three bits _____ Gate.	OR
121.	The ANSI/IEEE Standard 754 defines a _____ Single-Precision Floating Point format for binary numbers.	32-bit
122.	The basic building block for a logical circuit is _____	A Logical Gate
123.	The output of the expression $F=A.B.C$ will be Logic _____ when $A=1$ , $B=0$ , $C=1$ .	Zero
124.	_____ is invalid number of cells in a single group formed by the adjacent cells in K-map.	12