CS302
QUIZ#4
FINAL TERM
FALL 2024
BY
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FOR LMS HANDLING
CONTACT
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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 10 of 10 (Start time: 09:24:48 PM, 08 January 2025)

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

Select the correct option

- ○ 10 micro seconds
- ◉ 80 micro seconds
- ○ 8 micro seconds
- ○ 80 mili seconds

Question # 9 of 10 (Start time: 09:24:09 PM, 08 January 2025)

Karnaugh map is used in designing

Select the correct option

◉	All of the above
○	a clock
○	an UP/DOWN counter
○	a counter

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Question # 8 of 10 (Start time: 09:23:37 PM, 08 January 2025)

In designing any counter the transition from a current state to the next sate is determined by

Select the correct option

○	Only inputs
○	Only current state
○	current state and outputs
◉	Current state and inputs

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 7 of 10 (Start time: 09:22:50 PM, 08 January 2025)

The _____ inputs can be directly mapped to Karnaugh maps.

Select the correct option

- (●) S-R
- ( ) J-K
- ( ) External
- ( ) Flip-flop

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Question # 6 of 10 (Start time: 09:22:22 PM, 08 January 2025)

Choose the best possible answer of following question:
The D flip-flop is only activated by_____.

Select the correct option

◉	a positive edge trigger
○	a negative edge trigger
○	both positive & negative edge trigger
○	None of the given options

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 5 of 10 (Start time: 09:21:46 PM, 08 January 2025)

Each stage of Master-slave flip-flop works at ____ of the clock signal

Select the correct option

○	Each stage works on complete clock signal
●	One half
○	One fourth
○	One third

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 4 of 10 (Start time: 09:21:11 PM, 08 January 2025)

The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins

Select the correct option

○	2
○	6
◉	4
○	8

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CS302 - Digital Logic Design (Semester Quiz # 04) **Quiz Start Time: 09:18 PM, 08 January 2025**

Question # 3 of 10 (Start time: 09:20:06 PM, 08 January 2025) **Total Marks:** 1

The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)

Select the correct option

○	(2 raise to power n)
○	(n raise to power 2 and then minus 1)
◉	(2 raise to power n and then minus 1)
○	(n raise to power 2)

Click to Save Answer & Move to Next Question

CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 2 of 10 (Start time: 09:19:26 PM, 08 January 2025)

To parallel load a byte of data into a shift register, there must be

Select the correct option

○	eight clock pulse
○	one clock pulse for each 0 in the data
◉	one clock pulse
○	one clock pulse for each 1 in the data

CS302 - Digital Logic Design (Semester Quiz # 04) **Quiz Start Tir**

Question # 1 of 10 (Start time: 09:18:01 PM, 08 January 2025)

_____ is said to occur when multiple internal variables change due to change in one input variable

Select the correct option

- (●) Race condition
- ( ) Clock Skew
- ( ) Hold delay
- ( ) Hold and Wait

Click to Save Answ

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Asynchronous mean that_____

Select the correct option

○	Each flip-flop except the last one is enabled by the output of the preceding flip-flop
○	Each alternative flip-flop after the first one is enabled by the output of the preceding flip-flop
◉	Each flip-flop after the first one is enabled by the output of the preceding flip-flop
○	Each flip-flop is enabled by the output of the preceding flip-flop

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CS302 - Digital Logic Design (Semester Quiz # 04) Qu

Question # 9 of 10 (Start time: 08:23:10 PM, 08 January 2025)

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____

Select the correct option

○	none of given options
○	111
●	110
○	010

Question # 8 of 10 (Start time: 08:21:51 PM, 08 January 2025)

The Test Vector definition defines the test vectors for all the three counter inputs and _____counter output/outputs.

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Select the correct option

- ○ Four
- ◉ One
- ○ Three
- ○ Two

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 7 of 10 (Start time: 07:38:02 PM, 08 January 2025)

Each stage of Master-slave flip-flop works at ____ of the clock signal

Select the correct option

- ○ One fourth
- ○ One third
- ◉ One half
- ○ Each stage works on complete clock signal

Question # 6 of 10 (Start time: 07:36:26 PM, 08 January 2025)

_____ flip-flops are obsolete now.

Select the correct option

- ○ D-Flipflop
- ○ Edge-triggered
- ◉ Master-Slave
- ○ T-Flipflop

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 5 of 10 (Start time: 07:34:45 PM, 08 January 2025)

The glitches due to "Race Condition" can be avoided by using a _____

Select the correct option

○	Pulse triggered flip-flops
○	Negative-Edge triggered flip-flops
◉	Positive-Edge triggered flip-flops
○	Gated flip-flops

CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 4 of 10 (Start time: 07:34:19 PM, 08 January 2025)

The Synchronous counters are also known as Ripple Counters:

Select the correct option

- (●) False
- ( ) True

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 3 of 10 (Start time: 07:33:41 PM, 08 January 2025)

The term hold always means _____.

Select the correct option

○	Q=0, $\bar{Q}$=0
○	Q=0, $\bar{Q}$=1
●	No change
○	Q=1, $\bar{Q}$=0

Question # 2 of 10 (Start time: 07:33:02 PM, 08 January 2025) **Total Marks:** 1

A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

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Select the correct option

- 1100
- 1001
- 0011
- 1011

Click to Save Answer & Move to Next Question

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Question # 1 of 10 (Start time: 07:32:10 PM, 08 January 2025)

According to Moore circuit, the output of synchronous sequential circuit depend/s on _____ of flip flop.

Select the correct option

- (●) Previous State
- ( ) External Inputs
- ( ) Present State
- ( ) Next State

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CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Star

Question # 10 of 10 (Start time: 07:22:06 PM, 08 January 2025)

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to _____.

Select the correct option

○	Reset
◉	Toggle
○	Latch
○	Set

Click to Save A

CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Start Time: 07:16 PM

Question # 9 of 10 (Start time: 07:21:24 PM, 08 January 2025)

A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

Select the correct option

- (●) 1001
- ( ) 0011
- ( ) 1100
- ( ) 1011

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Question # 8 of 10 (Start time: 07:20:50 PM, 08 January 2025)

A divide-by-10 ring counter requires a minimum of

Select the correct option

○	five flip-flops
○	four flip-flops
○	twelve flip-flops
●	ten flip-flops

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 7 of 10 (Start time: 07:20:15 PM, 08 January 2025)

The terminal count of a 4-bit binary counter in the UP mode is_____

Select the correct option

- ○ 0011
- ○ 1100
- ○ 0000
- ◉ 1111

Question # 6 of 10 (Start time: 07:19:38 PM, 08 January 2025)

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

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Select the correct option

- ○ 64 mW
- ○ 10 mW
- ○ 1024 mW
- ◉ 25 mW

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 5 of 10 (Start time: 07:18:57 PM, 08 January 2025)

Karnaugh map is used in designing

Select the correct option

○	a counter
○	a clock
○	an UP/DOWN counter
◉	All of the above

CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 4 of 10 (Start time: 07:17:51 PM, 08 January 2025)

The characteristic equation of D-flip-flop implies that _____.

Select the correct option

○	The next state is independent of inputs
◉	The next state is dependent on present state
○	The next state is independent of present state
○	The next state is dependent on previous state

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Question # 3 of 10 (Start time: 07:17:18 PM, 08 January 2025)

If a circuit suffers "Clock Skew " problem, the output of circuit can't be guarantied.

Select the correct option

○	False
◉	True

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 2 of 10 (Start time: 07:16:45 PM, 08 January 2025)

The terminal count of a 4-bit binary counter in the DOWN mode is_____

Select the correct option

- (●) 0000
- ( ) 0011
- ( ) 1111
- ( ) 1100

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 1 of 10 (Start time: 07:16:21 PM, 08 January 2025)

_____ Counters as the name indicates are not triggered simultaneously

Select the correct option

- ○ Synchronous
- ○ Negative-Edge triggered
- ◉ Asynchronous
- ○ Positive-Edge triggered

Click to

CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Start Time: 04:29 PM

Question # 1 of 10 (Start time: 04:29:08 PM, 08 January 2025)

A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is_____

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Select the correct option

- 1000
- 0001
- 1111
- 1110

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CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 4 of 10 (Start time: 04:31:55 PM, 08 January 2025)

Number of states in an 8-bit Johnson counter sequence are:

Select the correct option

○	8
●	16
○	12
○	14

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Question # 3 of 10 (Start time: 04:31:22 PM, 08 January 2025)

A decade counter is _____

Select the correct option

- ○ Mod-8 counter
- ○ Mod-3 counter
- ◉ Mod-10 counter
- ○ Mod-5 counter

sec(s)

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Quiz Start Time: 04:29 PM, 08 January 2025

Question # 2 of 10 (Start time: 04:30:48 PM, 08 January 2025)

Total Marks: 1

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

Select the correct option

- 64 mW
- 1024 mW
- 10 mW
- 25 mW

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Question # 6 of 10 (Start time: 04:33:28 PM, 08 January 2025)

A stage in the shift register consists of

Select the correct option

○	a byte of storage
○	a latch
○	four bits of storage
●	a flip flop

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Question # 5 of 10 (Start time: 04:32:29 PM, 08 January 2025)

The characteristic equation of D-flip-flop implies that _____.

Select the correct option

- (●) The next state is dependent on present state
- ( ) The next state is independent of inputs
- ( ) The next state is dependent on previous state
- ( ) The next state is independent of present state

CS302 - Digital Logic Design (Semester Quiz # 04)

Question # 8 of 10 (Start time: 04:35:04 PM, 08 January 2025)

The term hold always means _____.

Select the correct option

- (●) No change
- ( ) $Q=1, \bar{Q}=0$
- ( ) $Q=0, \bar{Q}=0$
- ( ) $Q=0, \bar{Q}=1$

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CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Start Time: 04:29 PM, 08 January

Question # 7 of 10 (Start time: 04:34:03 PM, 08 January 2025) Total M

The Test Vector definition defines the test vectors for all the three counter inputs and _____counter output/outputs.

Select the correct option

- One
- Four
- Two
- Three

Click to Save Answer & Move to Next Questi

Question # 10 of 10 (Start time: 04:36:27 PM, 08 January 2025)

RCO stands for _____

Select the correct option

- (●) Reconfiguration Counter Output
- ( ) Reconfiguration Clock Output
- ( ) Ripple Clock Output
- ( ) Ripple Counter Output

Click to

Question # 9 of 10 (Start time: 04:35:47 PM, 08 January 2025)

Two states are said to be equal if they have exactly same_____.

Select the correct option

- ○ None of the given options
- ○ Next state
- ○ Inputs
- ◉ Outputs

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