1. The NOR logic gate is the same as operation of the…….gate with on inverter connected to the output

Ans. NOT

2.the logical sum of two or more logical product terms is called

Ans.SOP

3. The demulitplexer is called

Ans. data distributor

4.1010_0101……..

Ans.0101

5. The active high and active low inputs 3 to 8 decoder are as follows

Ans. one active high and two are remaining active low

6. The 16 input multiplexer the decoder input….and…..enable one out of four multiplexer

Ans. C, D

7. If the number of samples are collected is reduced by the half reconstructed signal will be……..from to original

Ans. different

8. Combinational logic is used to combination circuit where as registered logic base on……circuit

Ans. sequential circuit

9. Binary decorder have……..input and…….output

Ans.n, 2^n

10…….has fastest switching speed and low power requirements

Ans. advanced low power shockttky

11. The multiplexer circuit has …….input (s) and…..output (s)

Ans. multiple, signal

12. Which of the following 4 bit has five function select inputs?

Ans.74XX181

13. How many of enable inputs are active in74XX138 3 to 8 decoder

Ans. three

14. The based devolves with WC supply….vexes

Ans. +5

15. The number1259 may belong to…,….number system

Ans. decimal or hexadecimal system

16. ……..come different configuration they are identified unique number

Ans. Pals

17. NAND gate is formed by connecting

Ans. AND gate and then NOT gate

18. Subtraction also have output check 1 has been

Ans. borrowed

19. The data digit circuit operates with which contribution of value given blow

Ans. +5volts and o volts

20. An Asynchronous down counter implement using (J k flip flop) by connecting

Ans. Q output to all flip flop to clock input to next flip flop

21……..occur when the same clock signal arrive at different at different clock input due to propagation delay

Ans. clock skew

22. For a down counter that counts (111 to 000) if current state is*10* the next state will be……

Ans. 110

23. If S=1and R=0 then for positive edge triggered flip flop

Ans. 1

24 the terminal count of 4 bit binary counter in the UP mode is…….

Ans.1111

25. For a gated D latch If EN =1 and D =1 then Q (t+1) =……

Ans.1

26. A non shot mono stable device contain……

Ans. NOR gate resister,capacitor and NOT gate

27.Why demutiplexer is called data distributor

Ans. the input will be distributed to one of the output

28 74Als' stands for……

Ans. advanced low power Schottky TTL

29.Addition of two decimal digits in BCD can be done through

Ans.BCD adder

30.Which one is true

Ans. powe consumption of TTL is higher from CMOS

31.Both the multiplexer are selected simultaneously when….is not to logic….. In 2 input 8 bit multiplexer

Ans. S LOW

32.The complement of product of variable is equal to the sum of complement of variable is known as

Ans. DeMorgan's second theorem

33.The PLDS are implemented having a general purpose structure based on…….array

Ans. adjacent

34.A slandered interface for programming in system PLD consists

Ans. 4 wire

35.In 8 multiplexer the two output are connected though a gate

Ans. AND

36.The……select input (S) of the 4 input multiplexer are common dual 4 input multiplexer

Ans. two

37. maxterm is the sum of……of the corresponding monetary with its literal complemented

Ans. Terms

38. the below are integrated circuit technologies except

Ans. ETMOS

39. any of the……forms of the karnaugh map can be used to simplify Boolean expression

Ans. two

40. what is the value of output adding of following binary number 1011+1110

Ans.11001

41.the GAL22v10 is popular GAL having…….input and10 input/output

Ans.12

42.a standard SOP has …….term that have all variable in the domain of expression

Ans. Sum

43.which of the following is not correct method of grouping

Ans. on corners

Question1 Karnaugh map is used in designing

Ans. All of the above

Question2 In gate SR latch what is the value of the output of EN=1,S=0 and R=0?

Ans. 1

Question3 An Asynchronous Down-counter is implement (using J-k flip-flop) by connecting

Ans. Q,output of all flip- flops to clock input of next flip-flops

Question4 occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay

Ans. Clock skew

Question 5 The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the

Ans. Set- up time

Question6 A 4- bit UP- DOWN counter is in DOWN mode and in the 1010 state on the next clock pulse to what state does the counter go?

Ans.1011

Question 7 For a down counter that counts from(111 to 000) if current state is”101”the next state will be

Ans.110

Question8 If S=1 and R=0, then for positive edge triggered flip-flops

Q=(t+1)=

Ans.1

Question9 A one- shot mono-stable device contains=

Ans. NOR gate, Resistor, capacitor and NOT Gate

Question10 We have a digital circuit Different parts of circuit operate at different clock frequencies (4MHZ,2MHZ and 1MHZ), but we have a single clock sources of circuit we can get help by using

And. J-k flip-flop

Question11 RCO stands for

Ans. Ripple Clock Output

Question12 A Divide- by 20 counter can be achieved by using

Ans. Flip-Flop and DIV 10

Question13 The terminal count of a 4-bit binary counter in the Up mode is

Ans.1111

Question14 For a gated D-latch if EN-1 and D=1 then Q(t+1)=

Ans.1

Question 1

The Boolean expression A+BC equals

Ans.(A+B)'(A'+C)

Question2

The ABEL symbol for "OR" operation is

And. #

Question3

The domain of the expression AB'CD+AB'+CD+B is

Ans. A,B,C and D

Question4

Boolean Addition operation is performed by a(n).…gate

Ans. OR

Question5

The maximum decimal number that can be represented using the 64-bit unsigned represented is..

Ans.(2^64)+1

Question6

If the numbers of samples that are collected is reduced by half the reconstructed signal will be…form/to the original

Ans. Different

Question7

Is used when the output is connected back to the input of the PAL or if the output pin is used as a

Ans. combinational input/ output

Question8 is a single input gate

Ans. NOT

Question9

Is used when the output is connected back to the input of the PAL or if the output pin is used as an input only

Ans. combinational input/output

Question10

The domain of the expression AB` CD+ AB'+ CD+ B is

Ans. A,B,C and D

Question11

The GAL22V10 is a popular device having inputs and ten inputs/outputs

Ans.12

Question12

Power dissipation of device's remaining constant throughout their operation

Ans.TTL

Question13

The output of any CMOS series logic gate can be at logic high'1' or logic low '0'

Ans.3.3 and 5volt

Question14

Two 2-input ,4-bit multiplexers 74x157 can be connected to implement a…multiplexer.

Ans.2- input,8bit

Question15

The enable input of the decoder when set to 1 disables the decoder and the multiplexers.

Ans. G

Question16

Digital circuits operate with voltage value (s).

Ans.2

Question17

Canonical from is a unique way of representing

Ans. Boolean Expression

Question18

High level Noise margins (VNH) of CMOS 5volt series circuit is

Ans.3.3v

Question19

Consider A=1, B=0,C=1 B and C represent the input of three bit NAND gate, the output of the NAND gate will be.

Ans. No output as input is invalid

Question20

1011+101=

Ans.10011

Question21

When the control line in tri- state buffer is high the buffer operates like a gate

Ans.XOR

Question22

Addition of two BCD digits requires two…parallel adder circuits.

Ans.4- bit

Question23

Maxterm is the sum of the corresponding minterm with its literal complemented.

Ans. word

Question24 (A+B).(A+C)=

Ans. AC+B

Question25

Which of the following is not the correct method of grouping?

Ans. Along adjacent columns

Question26

Suppose we want to transmit the data" 10001101", and an "Even- parity" bit scheme is used to detect errors the parity bit added to this data will be

Ans.0

Question27

The implement the decoder circuit having inputs and outputs. Function tables have to be drawn which represent the output status of each Output line for or combinations of inputs

Ans.1 and 9

Question28

Parts of logic gate identifies the switching

Ans. XX

QuQuestion29

Inputs output

A	B.	R
0	0	0
0	1	1
1	0	1
1	1	0

The function table represent gate

Ans. NOT

Question30

Sum term (max term) is implemented using ….gates

Ans. OR

Inputs		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

this function table represents _____ Gate.

Or gate

The ABEL symbol for “OR” operation is

#

A standard SOP form has _____ terms that have all the variables in the domain of the expression.
Sum

which one of the following is not a valid rule of Boolean algebra?

A = Ā

How many data select lines are required for selecting eight inputs?
3 (correct)

If two adjacent 1s are detected in the input, the output is set to high. inpu t combinations will be
0011(ans)

The 4-variable Karnaugh Map (K-Map) has _____rows and ____colums
4,4, (ans)

The boolean expression A + B' + C is

a sum term(ans)

the boolean expression AB'CD'is

a product term(ans)

Don’t care conditions are marked as _____ in the output column of the function table

X(ans)

An example of SOP expression is
both (a) and (b)(ans)

For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.
1 (ans)

A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.

Select correct option:
2 (Correct)

Multiplexers are also known as _____.
Data Selectors

The OR Gate performs a Boolean _____ function
Addition (Correct)

Sum term (Max term) is implemented using _____ gates
OR (Correct)

The number “1259” may belong to _____ number system.
Binary or Hexadecimal system (Correct)

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result
1111 (Correct)

“1101” in signed representation is equivalent to _____
13 (Correct)

TTL based devices work with a dc supply of ____ Volts
+5 (Correct)

In decimal value “275” the weight of the digit “7” is _____
100 (Not Sure)

The decimal “10” will have an octal equivalent _____
9 (Not Sure)

Caveman number system is Base _____ number system
5 (Correct)

How many bits must each word have in one-to-four line de-multiplexer to be implemented using a memory?

1 bits

The total amount of memory is depends upon _____
The size of the address bus of the microprocessor

_____ can be determined the Instability condition.

logic diagram

If we add an inverter at the output of AND gate, what function is produced?

NAND

Which is also known as coincidence detector?

AND gate

Transition table include _____
squares

For every possible combination of logical states in the inputs, which table shows the logical state of a digital circuit output?
Truth table

Stack is an acronym for _____
LIFO memory

When an Asynchronous sequential circuit changes two or more binary states variables a Condition occurs called _____
Race condition

positive OR gate is also a negative

AND gate

Time delay device is memory element of_____

asynchronous circuits

Boolean algebra is also called

a) arithmetic algebra

b) switching algebra

c) Both A & B

Boolean function must be brought into_____ To perform product of max terms

OR terms

The binary number 10101 is equivalent to the decimal number_____.

21

The domain of expression ABCD + AB + CD + B is—
B only

The Boolean expression A BC D is—
Sum term

The universal gate is_____.
NAND gate

According to boolean algebra absorption law, which of the following is correct?

xy+y=x

A Boolean function may be transformed into
logical diagram

The inverter is _____
NOT gate

The resulting circuit of a NAND gate are connected together is_____

NOT gate

x*y = y*x is the
identity element

Minterms are also called

standard product

OR gate and _____ will form The NOR gate?
NOT gate

The NAND gate is AND gate followed by ……
NOT gate

Max terms are also called_____.
standard sum

In Boolean algebra Multiplicative inverse is
a

By the repeated use of _____Digital circuit can be made
NAND gates

The only function of NOT gate is_____ of the following.

Invert input signal

Boolean algebra is defined as a set of_____.
two values

First operator precedence for evaluating Boolean expressions is

Parenthesis

The output is_____ When an input signal 1 is applied to a NOT gate

0

The bar sign (-) indicates _____ In Boolean algebra?

NOT operation

The value of n is _____when the resolution of an n bit DAC with a maximum input of 5 V is 5 mV.

10

2’s complement of binary number 0101 is _____

1011

An OR gate has 4 inputs. The output is ……. When One input is high and the other three are low.

High

To convert BCD to seven segments _____device is used.

Decoder

Decimal number 10 is equal to binary number _____.

1010

In 2’s complement representation the number 11100101 represents the decimal number _____.

-27

BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are_____.

All

A decade counter skips _____.

binary states 1010 to 1111

_____Number of States A ring counter with 5 flip flops will have?

5

Positive edge-triggered flip-flop changes its state when _____

Low-to-high transition of clock

If S=1 and R=1, for negative edge triggered flip-flop then Q(t+1) = _____

Invalid

Adjacent 1s detector circuit will have active low output for the input

1101

A 5-variable karnaugh map has

Thirty two cells

8-bit parallel data can be converted into serial data by using _____ multiplexer

8-to-1 ok

In asynchronous digital systems all the circuits change their state with respect to a common clock

False

Divide-by-32 counter can be acheived by using

Flip-Flop and DIV 16

The Synchronous counters are also known as Ripple Counters:

False ok

A flip-flop is connected to +5 volts and it draws 5 mA of current during

its operation, the power dissipation of the flip-flop is
25 mW
The 3-to-8 Decoder has active-low outputs and three extra ____ gates connected at the three inputs to reduce the four unit load to a single unit load.

Not

Which of the number is not a representative of hexadecimal system?

“1001” correct

High level Noise Margins (VNH) of CMOS 5 volt series circuits is _____

0.9 V correct

To get the answer “1” in Boolean addition of three variables, _____

One of the variables must be 1 correct

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
8 correct

_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

2 correct

Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____
Zero

The Binary number 1011.101 has an Integer part represented by _____ and a fraction part ____ separated by a decimal point.
1011, 101 correct

1011+101 = _____

10000 correct

Adding two octal numbers “36” and “71” result in ___ _____
127 correct

The first Least Most digit in decimal number system has
Has position 0 and weight equal to 1 not sure

Sum term (Max term) is implemented using _____ gates
OR correct

The OR Gate performs a Boolean _____ function
Addition correct

Adding two octal numbers “36” and “71” result in _____
127 correct

If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____
24582 not sure

NOR Gate can be used to perform the operation of AND, OR and NOT Gate
TRUE correct

The three fundamental gates are _____
NOT, OR, AND correct

A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.
8 correct

The 4-variable K-Map has _____ rows and _____ columns of cells.
4, 4 correct

NAND gate is form by connecting _____
AND Gate and then NOT Gate correct

Which of the following is the octal equivalent of 28 decimal number?

34

The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.

(2^64)-1

In a 4-variable K-map, a 2-variable product term is produced by

a 4-cell group of 1s

For a Standard SOP expression, a ____ is placed in the cell corresponding to the product term present in the expression.

1

The _____ input select/deselects both the decoders simultaneously.

Enable

NAND and _____ gates are known as Universal Gates.

NOR

The declaration section of ABEL generally includes the device declaration, _____declarations and set declarations.

Pin

An SOP expression having a domain of 2 variables will have a truth table having _____combinations of inputs and corresponding output values.

4

In the 32-bit Single Precision Floating formation, the exponent value _____ is reserved to represent 0 exponents.

0

CMOS technology is characterized by low power dissipation with _____ switching speeds.

Slow

The complement of a variable is always

The inverse of the variable

A (B + C) = A.B + A.C is the expression of _____.

Distributive Law

If the number 2025 is represented in floating point, then exponent is _____.

3

Excess-8 code of -6 is _____.

0010

A 3-variable Karnaugh map has

Eight cells

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is _____ to the range of values that are to be represented.

Proportional

Suppose we want to transmit the data “10001101” and an “Even-Parity” bit scheme is used to detect errors, the parity bit added to the data will be_____.

Both “0” and “1” can be used

The carry propagation delay problem in parallel binary adder can be solved by _____.

Using two full adders

Two 2-input, 4-bit mulitplexers 74X157 can be connected to implement a _____ multiplexer.

2-input, 8-bit

The octal equivalent of the following binary number is _____.

117

A’ is written is ABEL as_____.

!A

Which of the following is the hexadecimal equivalent of 28?

1C

High Level Noise Margins (VNH) of CMOS 5 volt series circuits is _____.

0.9 V

Adjacent 1s detector circuit will have active high output for the input.

0011

Modern information techniques are relying more on _____ transmission.

Digital

The _____ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.

Two

How many data select lines are required for selecting eight inputs?

3

Select the mode of programming in which GAL 16V8 cam be programmed.

All of the given option

_____ has the fastest switching speed and low power requirement.

Advanced low power Schottky

The PLA can be programmed to give an output of constant _____ or _____.

0.1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called ___ of the flip-flop.

Hold time

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

Each stage of Master-slave flip-flop works at ___ of the clock signal.

One half

In Master-Slave flip-flop the clock signal is connected to slave flip-flip using ___

NOT

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is ___

1111

___ is said to occur when multiple internal variables change due to change in one input variable

Race condition

The Synchronous counters are also known as Ripple Counters: False

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the ___

Set-up time

The n flip-flops store ___ states.

2^n

When the ___ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of ___

1,2

A positive edge-trigged flip-flop changes its state when ___

Low-to-high transition of clock

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1,2

A positive edge-trigged flip-flop changes its state when ___

Low-to-high transition of clock

A decade counter is ___

Mod-10 counter

The look-ahead carry circuits_____

Reduce propagation delay

If two numbers in BCD representation generate an invalid BCD number then the binary __ is added to the result

0110

Both the multiplexers are selected simultaneously when _____is set to logic _____ in 2-inputs, 8-bit Multiplexer.

G, Low

Function labels required to represent the input/output combinations for each segment in 7-segment display
7

Multiplexers are also known as _____
Data selectors

The PLA can be programmed to give and output of constant_____ or _____
0, 1

Cin is part of _____ Adder.

Full

The look-ahead carry circuits_____

Reduce propagation delay

Which of the following gates has the outputs 1 if and only if at last one input is 1?

OR

A sop expression can be implemented by on ___combination of gates.

AND-OR

The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through ___ ALU units in 16-bit ALU.

Four

Digital circuits operates with_____ voltage value(s)
2

In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles_____
Lower priority outputs

To determine the seven expressions for each of the seven outputs in 7-segment display, seven _____ variable Karnaugh maps are used.
4

The output of a NAND Gate is ____ when all the inputs are one.

Zero

The _____ is the slowest and consumes more power.
Standard TTL

The between expression X-AB+CD represents
Two ANDs ORed together

The expression F-A+B+C describes the operation of three bits___ Gate.
OR

Which one of the following is NOT a valid rule of Boolean Algebra?
A=A'

A 5-Variable Karnaugh map has

Thirty two cells

____ is invalid number of cells in a single group formed by the adjacent cells K-map
12

In 32-bit Single –Precision floating point format representation the range of exponent value is from _____to _____
+127 to -126

____ has the fastest switching speed and low power requirements
Advanced low power schottky

Which of the following is a volatile memory?
DRAM

_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.
Combinational Input

The AND Gate performs a logical _____ function.
Division

The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacent 1s are detected in the input, the output is set to high.

1

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

row, column

Which of the following Output Equations determines the output of the State Machine?
MAX = Q0Q1EN

The maximum value, represented by a single hexadecimal digit is _____.

"F"

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.
1

The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.
High

Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.
Negative-OR, Negative-AND

Two signals _____ and _____ provide the timing inputs to the State Machine.
PTIME and QTIME

The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.
4

PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.
PLDs

The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.
CONSTATE

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.
Shift Registers

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.
Synchronous

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.
None of the given

The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-

Complemented B input to be connected to the Adder input.
XOR, NAND

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.
Four

In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.
NAND, NAND

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.
8 AND

8-bit parallel data can be converted into serial data by using _____ multiplexer.
8-to-1

The _____ input overrides the _____ input.
Asynchronous, synchronous

A SOP expression can be implemented by an _____ combination of gates.
AND-OR

The 64-cell array organized as 8 x 8 cell array is considered
as an 8 byte memory

The terminal count of a 4-bit binary counter in the UP mode is _____.

1100

A 3-variable karnaugh map has
eight cells

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.
Q output of all flip-flops to clock input of next flip-flops

Memory is arranged in _____.
Two-dimensional manner

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.
1001

Subtractors also have output to check if 1 has been _____.
Primed

The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.
Three

A multiplexer with a register circuit converts
Parallel data to serial

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.
True

The n flip-flops store _____ states.
2^n

The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.
four

Why demultiplexer is called a data distributor?
Single input to Single Output

When the transmission line is idle in an asynchronous transmission
It is set to logic high

UVERPROM is stands for
Ultra-Voilet

In memory write cycle, the time for which the WE signal remains active is known as the _____.
Write pulse width

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.
AND

PALs tend to execute _____ logic.
SOP

The ROM used by a computer is relatively _____ as it stores few buyers of code used to Boot the Computer system on power up.
Small

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?
-WE

You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);
NSY2 or EWY2

A NOR based S-R latch is implemented using _____ gates instead of _____ gates.
NOR, NAND

Implementation of Latch is required almost _____ transistor.
Six

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.
7.8 microsec

The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.
NAND

For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.
1

Select the mode of programming in which GAL16V8 can be programmed:
All of the given

Divide-by-32 counter can be achieved by using
Flip-Flop and DIV 32

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.
REQ1

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

One

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:
1111

Adding two octal numbers "36" and "71" result in _____.
127

The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.
Truth Table

The domain of the expression AB'CD + AB' + C'D + B is
A, B, C and D

If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.
Same

In DRAM read cycle R /W^{-} signal is activated to read data which is made available on the _____ data line.
D(OUT)

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.
True

Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.
RAM

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack

_____.
Top

Which one flip-flop has an invalid output state?
SR

The output of a NAND gate is _____ when all the inputs are one.
Zero

The Transition table is very similar to the _____ table.
State

Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.
256

Canonical form is a unique way of representing _____.
SOP

_____ Counters as the name indicates are not triggered simultaneously.
Synchronous

Cin is part of _____ Adder.
Full

Flash memories Operation are classified into _____ different operation.
Two

A Product term is 0 when_____
Any one literal is 0

In 8-inpit multiplexer, the two outputs are connected through a/an___gate.
OR

____ Device dissipate varying amount of power depending upon the frequency of operation.
CMOS

Boolean Addition operation is performed by a(an)___ gate.
OR

A SOP expression can be implemented by an_____ combination of gates.
AND-OR

The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.
(2^64)-1

In 16-bit ALU, The G output is activated if the 4-bi unit generate a Carry ____ irrespective of Carry___.
Out,In

A standard POS from has ____ ters that have all the variables in the domain of the expression.
Sum

In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles_____.
Lower priority inputs

Which of the following is the example of comparater?
XNOR

IN CMOS 5 Volt series, Input voltage of Logic high signal (VIH) with a ranges from ____ to ____ volts.
3,5,5

The Adjacent 1 S Detector accepts 4-bits input. If ____ adjacent 1S are detected in the input, the output is set to high.

4

DE Morgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

Negative-AND, Negative-OR

Adding two octal numbers "36 and 71" result in ____.

127

Any of the _____ forms of the Karnaugh Map can be used to simplify Boolean expressions

Four

Quine-McCluskey and K-Map methods are used for _____ of Boolean expression.

Simplification

The number "1259" may belong to ____ number system.

Decimal or Hexadecimal system

The series of TTL chips are characterized by their____.

Switching Speed only

All ABEL statements must end with_____.

;

In sequential circuit memory elements are connected with____.

Clock

In the 32-bit Single Precision Floating Point format, the exponent value____ is reserved to represent infinity exponents.

255

The _____ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

PLA

The limitation in implementation of parallel binary address is known as_____.

Carry input

The Gray code is different form the unsigned binary code because___.

Successive value of Gray code by only one bit

Removing the NOT gate at the output of the NOR gate result in an____.

OR gate

Portable devices that run on batteries use___ circuit that have low power dissipation.

Integrated

The domain of the expression AB'CD+B is

B only

_____ is a single input gate

OR

To represent in digital value, the number of digit (0s and 1s) that represent a quantity is ____ to the range of values that are to be represented.

Equal

BCD code of 16 is____.

00010001

To determine the seven expressions for each of the seven outputs in 7-segment display, seven____ variable Karnaugh Maps are used.

3

In Odd parity generator circuit which gate is used to detect parity errors?
XOR

A 3-variable Karnaugh map has
Eight cells

The measurable values generally change over a
Continuous range

____ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.
GAL

When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?
1001

How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decorder?
Three

The simplified expression using either of the two K-maps are_____.
Identical

Which of the following expression in the product of sums form?

AB+CD

CMOS technology is characterized by low power dissipation with____ switching speeds.

Slow

GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

True

High level Noise Margins (VNH) of CMOS 5 volt series circuits is_____

0.9 V

The output of the expression F=A+B+C will be Logic _____when A=0, B=1, C=1. the symbol"+" here represents OR Gate

One

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

SET

3.3 v CMOS series is characterized by _____ and_____as compared to the 5 v CMOS series.

Fast switching speeds, very low power dissipation (page61)

The binary value "1010110" is equivalent to decimal _____

86

The _____ Encoder is used as a keypad encoder.

Decimal-to-BCD Priority

How many data select lines are required for selecting eight inputs?

3

The Quad Multiplexer has _____ outputs

4

Demultiplexer has

Single input and multiple outputs.

The expression _____ is an example of Commutative Law for Multiplication.

AB=BA

The look-ahead carry circuits_____

Reduce propagation delay

What is the output expression of segment ‘b’ implementation in BCD to 7-segment decoder?

B’+C’D’+CD

2-input, 8-bit Multiplexer, by setting the S input to logic_____the____ inputs of both the multiplexers are selected.

High, B

The maximum decimal number that can be represented using the 64-bit unsigned representation_____

(2^64)-1

When two or more products terms are assumed by Boolean addition, the result is a ____

SOP

Tri-State Buffer is a ___ gate with a control line that disconnects the

NOT

The 4-bits 2’s complement representation of “7” is _____

1001

_____and _____ are the steps of the Quine-McCluskey.
Find prime implicants and select minimal set of the prime implicants.

The binary number 1011,101 has an Integer part represented by_____ and a fraction part ___ separated by a decimal point.
1011,101

Subtractors also have output to check if 1 has been _____
Borrowed

CMOS technology is characterized by low power dissipation with_____ switching speeds.
Slow

The _____ description is used to simulate the logic circuit and verify its operation.
Test vector

How many outputs can an integrated circuit comparator have?
Three

Which of the following is not the correct method of grouping?
Diagonally

The output of the expression F=A.B.C will be logic _____when A=1,B=0, C=1.

Zero

The _____ gate and ___ gate implementation connected at the B input of the 4-bit Adder is used to allow complemented or Un-Complemented B

input to be connected to the Adder input.
AND, OR

In the 32-bit Single Precision Floating point format, the exponent value _____ is reserved infinity exponent.
99

The Boolean expression (AB'CS') is used
A product term

The product of an XOR gate is zero(0), when _____All the inputs are zero
I and IV only

_____ methods are used to Convert Decimal fractions to Binary.
2

To display the number___ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit
2

A SOP expression is equal to I _____

When one or more product terms in the expression arc equal to 1

The output A B is set to I when the input combinations is
A=01, B=10

Two 2-bit comparator circuits can be connected to form single 4-bit comparator
True

High level Noise Margms (VNH) of CMOS 5 volt series circuits is _____

0.9 V

If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them inflating point representation and then multiplying them, the value of mantissa of result will be _____

24.582 (But not sure)

The output of the expression FA+B+C will be Logic _____represents OR Gate.

10(binary)

If an active-HIGH S-R latch has a O on the S input and a 1 on the R input and then the R input goes too, the latch will be

SET

3.3 y CMOS series is characterized by _____ and _____as compared to the 5 y CMOS sense.

Fast swltchln2 secedes. Very low lower dissolution Date 1

The binary value “1010110” is equivalent to decimal _____

86 (According to Formula)

Divide-by-32 counter can be acheived by using

Flip-Flop and DIV 10
Flip-Flop and DIV 16
Flip-Flop and DIV 32
DIV 16 and DIV 32

The counter states or the range of numbers of a counter is determined by

the formula. (“n” represents the total number of flip-flops)

(n raise to power 2)
(n raise to power 2 and then minus 1)
(2 raise to power n)
(2 raise to power n and then minus 1)

A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

1001
1011
0011
1100

A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is_____

0001
1111
1000
1110

Divide-by-160 counter is acheived by using

Flip-Flop and DIV 10
Flip-Flop and DIV 16

DIV 16 and DIV 32
DIV 16 and DIV 10

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

3
7
8
15

RCO stands for _____

Reconfiguration Counter Output
Ripple Counter Output
Reconfiguration Clock Output
Ripple Clock Output

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition
Clock Skew
Ripple Effect
None of given options

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____

111
110
010
none of given options

A Divide-by-20 counter can be acheived by using

Flip-Flop and DIV 10
Flip-Flop and DIV 16
Flip-Flop and DIV 32
Div 10 and DIV 16

Ripple Clock Output
The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins

2
4
6
8

_____ Counters as the name indicates are not triggered simultaneously

Asynchronous
Synchronous
Positive-Edge triggered
Negative-Edge triggered

Q : A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

3
7
8
15

Q : Design of state diagram is one of many steps used to design

a clock
a truncated counter
an UP/DOWN counter
any counter

Q : A synchronous decade counter will have _____ flip-flops

3
4
7
10

Q : Karnaugh map is used in designing

a clock
a counter
an UP/DOWN counter
All of the above

Q : _____ is said to occur when multiple internal variables change due to change in one input variable

Hold and Wait
Clock Skew

Race condition
Hold delay

Q : Three cascaded modulus-10 counters have an overall modulus of

30
100
1000
10000

Q : An Astablemultivibrator is known as a(n) _____

Oscillator
Booster
One-shot
Dual-shot

Q: _____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition
Clock Skew
Ripple Effect
None of given options

Q:The glitches due to "Race Condition" can be avoided by using a _____

Gated flip-flops
Pulse triggered flip-flops
Positive-Edge triggered flip-flops
Negative-Edge triggered flip-flops

Q: In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple

counters together

True
False

Quiz: A flip-flop is presently in SET stae and must remain SET on the next cliock pulse. What must j and K be?

J = 1, K = 0
J = 1, K = X(Don't care)
J = X(Don't care), K = 0
J = 0, K = X(Don't care)

Q: The Synchronous counters are also known as Ripple Counters: :

True
False

Q:A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True
False

Quiz: The terminal count of a 4-bit binary counter in the DOWN mode is_____

0000
0011
1100
1111

Quiz: An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting_____

Q output of all flip-flops to clock input of next flip-flops
Q' output of all flip-flops to clock input of next flip-flops
Q output of all flip-flops to J input of next flip-flops
Q' output of all flip-flops to K input of next flip-flops

the terminal count of a modulus-13 binary counter is

0000
1111
1101
1100

Quiz: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True
False

Quiz: A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

1001
1011
0011
1100

Quiz: Design of state diagram is one of many steps used to design

a clock
a truncated counter
an UP/DOWN counter
any counter

Quiz: An Astable multivibrator is known as a(n) _____

Oscillator
Booster
One-shot
Dual-shot

Quiz: The glitches due to "Race Condition" can be avoided by using a _____

Gated flip-flops
Pulse triggered flip-flops
Positive-Edge triggered flip-flops
Negative-Edge triggered flip-flops

Quiz: A decade counter is _____

Mod-3 counter
Mod-5 counter
Mod-8 counter
Mod-10 counter

The terminal count of a 4-bit binary counter in the DOWN mode is_____

0000
0011
1100
1111

The Synchronous counters are also known as Ripple Counters:

True
False

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition
Clock Skew
Ripple Effect
None of given options

Divide-by-160 counter is acheived by using

Flip-Flop and DIV 10
Flip-Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

Design of state diagram is one of many steps used to design

a clock
a truncated counter
an UP/DOWN counter
any counter

In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is_____

0000
1111
0001
10000