CS-302 Digital Logic Design

Update MCQS For Quiz-4 File

Solve By Vu Topper RM

85 To 100% Marks

A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is_____

A. 1111
B. 1110
C. 0001
D. 1000

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _____

A. Set-up time **Page 234**
B. Hold time
C. Pulse Interval time
D. Pulse Stability time (PST)

The n flip-flops store _____ states.

A. 0
B. 1
C. 2^n
D. 2^(n+1)

Design of state diagram is one of many steps used to design

A. a clock
B. any counter
C. A truncated counter
D. an UP/DOWN counter

A Divide-by-20 counter can be acheived by using

A. Flip-Flop and DIV 10
B. Flip-Flop and DIV 16
C. Flip-Flop and DIV 32
D. Div 10 and DIV 16

The counter states or the range of numbers of a counter is determined by the formula. (“n” represents the total number of flip-flops)

A. (n raise to power 2)
B. (n raise to power 2 and then minus 1)
C. (2 raise to power n)
D. (2 raise to power n and then minus 1)

State of flip-flop can be switched by changing its_____.
A. Input signal
B. Output signal
C. Momentary Signal
D. Contemporary Signal

An Astable multivibrator is known as a(n) _____
A. Oscillator **Page 258**
B. Booster
C. One-shot
D. Dual-shot

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.
A. True
B. False

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to _____.
A. set
B. reset
C. latch
D. **Toggle**

_____ flip-flops are obsolete now.
A. Edge-triggered
B. **Master-Slave** **Page 257**
C. T-Flipflop
D. D-Flipflop

In designing any synchronous counter a modulus number is used which determine the number of..... used in a counter…..

A. Registers
B. **Flip Flops**
C. Counters
D. Latches

The _____ inputs can be directly mapped to Karnaugh maps.

A. J-K **Page 300**
B. S-R
C. External
D. Flip-flop

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

A. Hold time **Page 242**
B. Set-up time
C. Pulse Interval time
D. Pulse Stability time (PST)

The terminal count of a 4-bit binary counter in the DOWN mode is_____

A. 0000
B. 0011
C. 1100
D. 1111

RCO stands for _____

A. Reconfiguration Counter Output
B. Ripple Counter Output
C. Reconfiguration Clock Output
D. Ripple Clock Output **Page 285**

_____ is said to occur when multiple internal variables change due to change in one input variable

A. Hold delay
B. Clock Skew
C. Race condition Page 267
D. Hold and Wait

The synchronous counters are also known as Ripple Counters:
A. True
B. False

The 3-bit up counter can be implemented using _____ flip-flop(s).
A. D-Flip-flop Only
B. S-R Flip-flops Only
C. S-R Flip-flops or D-Flip-flops
D. S-R flip-flops and D-flip-flops Page 316

The 74HC163 is a 4-bit Synchronous Counter.it has.....parallel data inputs pins
A. 2
B. 4 Page 278
C. 6
D. 8

A-stable multi-vibrator continuously changes from one unstable state to the other without any_____.
A. Output
B. Variable
C. Flip flop
D. External trigger Page 258

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
A. Race condition
B. Clock Skew Page 226
C. Ripple Effect
D. None of given options

In designing any counter the transition from a current state to the next sate is determined by

A. Current state and inputs **Page 332**
B. Only inputs Only current state
C. Positive-Edge triggered
D. Negative-Edge triggered

The glitches due to "Race Condition" can be avoided by using a _____

A. Negative-Edge triggered flipflops **Page 260**
B. Positive -Edge triggered flipflops
C. Gated flip-flops
D. Pulse triggered flip-flops

Divide-by-160 counter is acheived by using
A. Flip-Flop and DIV 10
B. Flip-Flop and DIV 16
C. DIV 16 and DIV 32
D. **DIV 16 and DIV 10**

Two states are said to be equal if they have exactly same_____.
A. Output
B. Input **Page 325**
C. Both
D. None

A modulus-14 counter has fourteen states requiring_____
A. **4 flip flops**
B. 6 flip flops
C. 8 flip flops
D. 2 flip flops

Asynchronous mean that_____

A. Each flip-flop is enabled by the output of the preceding flip-flop
B. Each flip-flop after the first one is enabled by the output of the preceding flip-flop
C. Each flip-flop except the last one is enabled by the output of the preceding flip-flop
D. Each alternative flip-flop after the first one is enabled by the output of the preceding flip-flop

The characteristic equation of D-flip-flop implies that _____.

A. The next state is independent of inputs
B. The next state is dependent on present state
C. The next state is dependent on previous state
D. The next state is independent of the present state.
Page 381

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

A. 2
B. 4
C. 8 **Page 272**
D. 10

The term hold always means _____.

A. No change
B. Q=1, $\bar{Q}$=0
C. Q=0, $\bar{Q}$=0
D. Q=0, $\bar{Q}$=1

In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is _____

A. 0001

B. 0011
C. 0000
D. 10000

When the _____ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of _____ seconds.

A. 1,2
B. 3,4
C. 5,6
D. 8,7

The terminal count of a 4-bit binary counter in the UP mode is_____

A. 1111
B. 0011
C. 0000
D. 1211

Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state Select correct option:

A. Ten
B. Eight
C. Three
D. Two **Page 255**

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together

A. True
B. False

In moore machine the output depends on

A. Only inputs
B. The current state

C. The current state and inputs
D. The current state and the output of previous flip flop

The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins

A. 2
B. 4 Page 278
C. 6
D. 8

Divide-by-32 counter can be acheived by using

A. Flip-Flop and DIV 10
B. Flip-Flop and DIV 16
C. Flip-Flop and DIV 32
D. DIV 16 and DIV 32

Three cascaded modulus-10 counters have an overall modulus of.

A. 30
B. 100
C. 1000
D. 10000

A decade counter is _____

A. Mod-3 counter
B. Mod-5 counter
C. Mod-8 counter
D. Mod-10 counter Page 274

To implement the counter using S-R flip-flops instead of J-K flip-flops, the _____ transition table is used.

A. S-R Page 316
B. D-R
C. J-K
D. None

The terminal count of a modulus-13 binary counter is

A. 0000
B. 1111
C. 1101
D. 1100

In synchronous digital circuits the _____of one flip-flop is connected to the _____of a second flip-flop.

A. Input, Output
B. Output, input **Page 258**
C. Input, clock signal
D. Clock signal, Output

Question No:1 **(Marks:1)** **Vu-Topper RM**

Demultiplexer is also called _____

A. Data router
B. Data selector
C. Data encoder
D. Data Distributor **Page 178**

Question No:1 **(Marks:1)** **Vu-Topper RM**

2-Input, 8-bit Multiplexer, by setting the S input to logic ____ the __ inputs of both the multiplexers are selected.

A. Low, B
B. High, C
C. High, B
D. Low, C

Question No:1 **(Marks:1)** **Vu-Topper RM**

On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____

A. The clock pulse is LOW
B. The clock pulse is HIGH
C. The clock pulse transition from HIGH to LOW
D. The clock pulse transition from LOW to HIGH **Google**

Question No:1 **(Marks:1)** **Vu-Topper RM**

A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

A. XOR, NAND
B. NOR, XOR
C. NOR, NAND **Page 213**
D. OR, XOR

Question No:1 **(Marks:1)** **Vu-Topper RM**

When the number 29 is represented on 7-segment display, which BCD input is represented on LSD display unit?

A. 1001 **Page 172**
B. 1000
C. 1100
D. 1010

Question No:1 **(Marks:1)** **Vu-Topper RM**

The GAL22V10 is a popular GAL device having _____ inputs and ten inputs/outputs.

A. 10
B. 12 **Page 194**
C. 14
D. 16

Question No:1 **(Marks:1)** **Vu-Topper RM**

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

A. Doesn't have an invalid state **Page 232**
B. Sets to clear when both J = 0 and K = 0
C. It does not accept asynchronous inputs
D. It does not show transition on change in pulse

Question No:1 **(Marks:1)** **Vu-Topper RM**

Question No:1 **(Marks:1)** **Vu-Topper RM**

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), to supply the required frequency to each part of circuit, we can get help by using _____

A. J-K flip-flop **Page 257**

B. J-d flip-flop

C. Both

D. None of the these

Question No:10 **(Marks:1)** **Vu-Topper RM**

Tri-State Buffer is a _____ gate with a control line that disconnects the output from the input.

A. OR

B. AND

C. NOT **Page 196**

D. NAND

Question No:10 **(Marks:1)** **Vu-Topper RM**

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

A. Column, row **Page 191**

B. column, row

C. column, column

D. row, row

Question No:10 **(Marks:1)** **Vu-Topper RM**

When the control line in tri-state buffer is high, the buffer operates like a _____ gate

A. NOT **Page 196**

B. AND

C. OR

D. XOR

Question No:10 (Marks:1) Vu-Topper RM

8-bit parallel data can be converted into serial data by using _____ multiplexer.

A. 8-to-1 Page 175

B. 8-to-4

C. 4-to-2

D. 4-to-4

Question No:10 (Marks:1) Vu-Topper RM

In GAL16V8, each product term is implemented using a 32-bit input _____ gate.

A. OR

B. AND Page 200

C. NOT

D. NAND

Question No:10 (Marks:1) Vu-Topper RM

The declaration section of ABEL generally includes the device declaration, _____ declarations and set declarations.

A. Pin Page 207

B. Cell

C. Model

D. System

Question No:10 (Marks:1) Vu-Topper RM

System having memory elements are called_____ circuits.

A. Simplex

B. Sequential Google

C. Quadrantal

D. Combinational

Question No:10 (Marks:1) Vu-Topper RM

A standard interface for programming the In-System PLD consists of

A. 2 wire
B. **4 wire** **Page 194**
C. 8 wire
D. 16 wire

Question No:10 (Marks:1) Vu-Topper RM
In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?
A. 0
B. 1
C. 2
D. 3

Question No:10 (Marks:1) Vu-Topper RM
Question No:20 (Marks:1) Vu-Topper RM
Question No:20 (Marks:1) Vu-Topper RM
A synchronous decade counter will have _____ flip-flops
A. 3
B. 4 **Page 281**
C. 7
D. 10

Question No:20 (Marks:1) Vu-Topper RM
The _____ input overrides the _____ input
A. Asynchronous, synchronous **Page 369**
B. Synchronous, asynchronous
C. Preset input (PRE), Clear input (CLR)
D. Clear input (CLR), Preset input (PRE)

Question No:20 (Marks:1) Vu-Topper RM
To display the number ____ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-Segment display circuit connected to the MSD 7-Segment Display Digit.
A. 19
B. 29 **Page 172**

C. 39
D. 49

Question No:20 (Marks:1) Vu-Topper RM
In 16-input multiplexer, the decoder inputs ____ and ____ enable one out of the four multiplexers.

A. C and D Page 171
B. A and B
C. B and A
D. A and D

Question No:20 (Marks:1) Vu-Topper RM
Flip flops are also called _____

A. Bi-stable multivibrators Page 228
B. Bi-stable singlevibrators
C. Bi-stable dualvibrators
D. Bi-stable transformer

Question No:20 (Marks:1) Vu-Topper RM
Once the state diagram is drawn for any sequential circuit the next step is to draw

A. Transition table
B. Karnaugh map
C. Next- state table
D. Logic expression

Question No:20 (Marks:1) Vu-Topper RM
Question No:20 (Marks:1) Vu-Topper RM
Question No:20 (Marks:1) Vu-Topper RM
Question No:30 (Marks:1) Vu-Topper RM
For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____

A. Invalid
B. 1
C. 0

D. Q(t)

Question No:30 (Marks:1) Vu-Topper RM

Question No:30 (Marks:1) Vu-Topper RM

The_____ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

A. PLA
B. Combinational
C. Combinational input/
D. Programmed Polarity Page 18

Question No:30 (Marks:1) Vu-Topper RM

The latch is said to be in logic _____ state whenQ=1 and Q'=0 and it is in the logic low state when Q=0 and Q'=1.

A. Low
B. Zero
C. High Page 211
D. Constant

Question No:30 (Marks:1) Vu-Topper RM

The primary use of multiplexers is _____.

A. Data Router
B. Operation sequencing
C. Logic function generator
D. Parallel to Serial Converter Page 172

Question No:30 (Marks:1) Vu-Topper RM

If the S and R inputs of the gated S-R latch are connected together using a _____ gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

A. OR
B. And
C. **NOT Page 226**
D. XOR

Question No:30 (Marks:1) Vu-Topper RM

In Complex mode of GAL16V8, OLMCs can be configured in _____ ways.

A. Two **Page 202**

B. Fore

C. Five

D. Three

Question No:30 **(Marks:1)** **Vu-Topper RM**

In 1-to-4 demultiplexer, how many select lines are required

A. 1 select lines

B. 2 select lines **Page 396**

C. 3 select lines

D. 4 select lines

Question No:30 **(Marks:1)** **Vu-Topper RM**

Question No:30 **(Marks:1)** **Vu-Topper RM**

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

A. OR

B. AND **Page 182**

C. XOR

D. NAND

Question No:40 **(Marks:1)** **Vu-Topper RM**

The ____ enable input of the decoder when set to 1 disables the decoder and the multiplexers.

A. G **Page 171**

B. B

C. A

D. S

Question No:40 **(Marks:1)** **Vu-Topper RM**

If S=1 and R=1, for negative edge triggered flip-flop then

A. Direct

B. **Invalid** **Page 233**

C. Valid
D. Indirect

Question No:40 (Marks:1) Vu-Topper RM
Question No:40 (Marks:1) Vu-Topper RM
Question No:40 (Marks:1) Vu-Topper RM
Question No:40 (Marks:1) Vu-Topper RM
Question No:40 (Marks:1) Vu-Topper RM
A _____ attached to the Select inputs of the Demultiplexer routes the incoming serial bits to successive outputs where each bit is stored.

A. Data
B. Buffer
C. Memory
D. Counter Page 178

Question No:40 (Marks:1) Vu-Topper RM
The OLMC can be configured to provide a feedback input signal to the AND gate array input. There are _____ possibilities.

A. Two
B. Five
C. Four
D. Three Page 200

Question No:40 (Marks:1) Vu-Topper RM
The PLA can be programmed to give an output of constant ___ or _____.

A. 2.3
B. 0.1 Page 190
C. 0.0
D. 1.2

Question No:40 (Marks:1) Vu-Topper RM
PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

A. PALs
B. PLAs
C. PLDs **Page 194**
D. EPROM

Question No:50 **(Marks:1)** **Vu-Topper RM**
Question No:50 **(Marks:1)** **Vu-Topper RM**
In Combinational Output with feedback to AND array, the active-state of the output is determined by the _____ input.
A. OR
B. NOT
C. XOR **Page 201**
D. AND

Question No:50 **(Marks:1)** **Vu-Topper RM**
Karnaugh map is used in designing
A. a clock
B. a counter
C. an UP/DOWN counter
D. **All of the above**

Question No:50 **(Marks:1)** **Vu-Topper RM**
The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.
A. Four **Page 212**
B. Eight
C. Seven
D. Sixteen

Question No:50 **(Marks:1)** **Vu-Topper RM**
Question No:50 **(Marks:1)** **Vu-Topper RM**
Question No:50 **(Marks:1)** **Vu-Topper RM**
_____ is one of the examples of asynchronous inputs.
A. D input

B. J-K input
C. S-R input
D. Clear Input (CLR) **Page 235**

Question No:50 **(Marks:1)** **Vu-Topper RM**
The GAL16V8 has eight _____each connected to eight product terms.
A. OLMCs **Page 200**
B. POS
C. SOP
D. CELLS

Question No:50 **(Marks:1)** **Vu-Topper RM**
_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.
A. Combinational Input/Output **Page 185**
B. Combinational Input/Output
C. Combinational Output
D. Programmable polarity

Question No:50 **(Marks:1)** **Vu-Topper RM**
The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.
A. REQ0
B. OPEN
C. REQ1 **Page 370**
D. FLOOR1

Question No:60 **(Marks:1)** **Vu-Topper RM**
_____ Yellow signal controlling the traffic on the East-West section.
A. EWYel **Page 375**
B. NSRed

C. EWRed
D. TMRST

Question No:60 (Marks:1) Vu-Topper RM

An 8-bit converter requires_____weighted resistors which have exact values otherwise the output of the converter is not accurate.

A. Seven
B. Ten
C. Eight Page 451
D. Nine

Question No:60 (Marks:1) Vu-Topper RM

ROMs and PROMs retains information _____ even if the supply voltage is removed.

A. Two days
B. Four days
C. Permanently Page 417
D. Ten days

Question No:60 (Marks:1) Vu-Topper RM
Question No:60 (Marks:1) Vu-Topper RM
Question No:60 (Marks:1) Vu-Topper RM

FLASH memory cell is implemented using a single floating-gate_____transistor.

A. POS
B. MOS Page 412
C. LOS
D. GOS

Question No:60 (Marks:1) Vu-Topper RM

Two State variables allow a maximum of _____ states.

A. Two

B. Four Page 385

C. Six

D. Eight

Question No:60 (Marks:1) Vu-Topper RM

There are____type of EPROM

A. One

B. Two Page 411

C. Three

D. Four

Question No:60 (Marks:1) Vu-Topper RM

Synchronous SRAM uses a clock signal which is used by the _____ to synchronize its activities.

A. ALU

B. Control Unit

C. Address Bus

D. Microprocessor Page 398

Question No:60 (Marks:1) Vu-Topper RM

Analogue signals are converted into Digital signals by _____converters.

A. Analogue to Analogue (A/A)

B. Analogue to Digital (A/D) Page 434

C. Digital to Analogue (D/A)

D. Digital to Digital (D/D)

Question No:70 (Marks:1) Vu-Topper RM

The duration for which the elevator doors are opened, and remain open, and time it takes for the elevator to move from one floor to the next can be determined by a/an_____.

A. Input signal

B. Clock signal Page 365

C. Output signal

D. None

Question No:70 (Marks:1) Vu-Topper RM

Memories are implemented in_____bit data unit sizes

A. 1,2 and 6

B. 1.,4 and 8 Page 425

C. 2,3 and 6

D. 4,4 and 8

Question No:70 (Marks:1) Vu-Topper RM

PALs tend to execute _____ logic.

A. SPD

B. SOP

C. SAC

D. SAP

Question No:70 (Marks:1) Vu-Topper RM

There are _____ possible combinations of the Simple Mode in which OLMC can be configured.

A. Three Page 201

B. Four

C. Five

D. Six

Question No:70 (Marks:1) Vu-Topper RM

If S=1 and R=0, then for positive edge triggered flip-flop Q(t+1) = ___

A. 0

B. 1 Page 230

C. Invalid

D. Input is invalid

Question No:70 (Marks:1) Vu-Topper RM

According to Moore circuit, the output of synchronous sequential circuit depend/s on _____ of flip flop.

A. Previous state

B. Present state

C. Next state

D. External state

Question No:70 (Marks:1) Vu-Topper RM

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.

A. NOT

B. AND Page 372

C. OR

D. XOR

Question No:70 (Marks:1) Vu-Topper RM

In memory write cycle, the time for which the WE signal remains active is known as the _____.

A. Write address setup

B. Write pulse width Page 397

C. Write delay width

D. Write data time

Question No:70 **(Marks:1)** **Vu-Topper RM**

_____ is one of the examples of synchronous inputs.

A. J-K input **Page 235**

B. EN input

C. Preset input (PRE)

D. Clear Input (CL

Question No:70 **(Marks:1)** **Vu-Topper RM**

Question No:80 **(Marks:1)** **Vu-Topper RM**

A latch is a temporary storage device that has _____ stable states.

A. Two **Page 211**

B. Three

C. Four

D. Five

Question No:80 **(Marks:1)** **Vu-Topper RM**

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Question No:80 **(Marks:1)** **Vu-Topper RM**

Question No:80 **(Marks:1)** **Vu-Topper RM**

Flash memory Operation are classified into _____ different operation.

A. One

B. Two

C. Three **Page 413**

D. Four

Question No:80 **(Marks:1)** **Vu-Topper RM**

Question No:80 **(Marks:1)** **Vu-Topper RM**

A negative edge-triggered flip-flop changes its state when _____

Enable input (EN) is set

A. Preset input (PRE) is set

B. Enable input (EN) is set

C. Low-to-high transition of clock
D. High-to-low transition of clock Page 228

Question No:80 (Marks:1) Vu-Topper RM
In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in ___when Distributed refresh is used.
A. 4.8 microsec
B. 5.9 microsec
C. 7.8 microsec Page 406
D. 5.5 microsec

Question No:90 (Marks:1) Vu-Topper RM
The 64-cell array organized as 8 x 8 cell array is considered as a 64-byte memory
A. as a 16 byte memory
B. as an 8 byte memory Page 387
C. as an 4 byte memory
D. None of the given

Question No:90 (Marks:1) Vu-Topper RM
____ Counters as the name indicates are not triggered simultaneously
A. Asynchronous Page 262
B. Synchronous
C. Positive-Edge triggered
D. Negative-Edge triggered

Question No:90 (Marks:1) Vu-Topper RM
You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);
A. NSY2 or EWY2
B. NSSR or TMRST

C. EWSR or NSRED
D. EWRed or EWYel

Question No:90 (Marks:1) Vu-Topper RM
Which of the following is a volatile memory?
A. DRAM
B. PROM
C. EPROM
D. EEPROM

Question No:90 (Marks:1) Vu-Topper RM
The counter states or the range of the number of a counter is determined by the formula("n" represented the total number of flip-flops)
A. 2 raise to power n
B. (n raise to power 2)
C. (n raise to power 2 and then minus 1)
D. (2 raise to power n and then minus 1)

Question No:90 (Marks:1) Vu-Topper RM
In DRAM read cycle R /W^- signal is activated to read data which is made available on the _____ data line.
A. D(IN)
B. D(OUT) **Page 405**
C. D(AB)
D. D(INT)

Question No:90 (Marks:1) Vu-Topper RM
A SOP expression can be implemented by an _____ combination of gates.
A. AND-OR **Page 78**
B. OR-XOR
C. AND-NAND
D. XOR-NOR

Question No:90 (Marks:1) Vu-Topper RM

A 3-variable Karnaugh map has

A. Eight cells **Page 89**

B. three cells

C. sixteen cells

D. four cells

Question No:90 **(Marks:1)** **Vu-Topper RM**

The ABEL Input file can use a_____ instead of the equation to specify the Boolean expressions.

A. Truth Table **Page 370**

B. Logic Circuit

C. State Diagram

D. Karnaugh Map

Question No:90 **(Marks:1)** **Vu-Topper RM**

In the keyboard encoder, how many times per second does the ring counter scan the key board?

A. 650 scans/second

B. 600 scans/second

C. 625 scans/second

D. 700 scans/second

Question No:100 **(Marks:1)** **Vu-Topper RM**

In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

A. NAND, NAND **Page 211**

B. NOR, NAND

C. NAND, NOR

D. NOR, NOR

Question No:55 **(Marks:1)** **Vu-Topper RM**

Select the mode of programming in which GAL16V8 can be programmed:

A. All of the given

B. Simple Mode

C. Complex Mode
D. Registered Mode

Question No:56 (Marks:1) Vu-Topper RM

Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

A. 256
B. 257
C. 258
D. 259

Question No:58 (Marks:1) Vu-Topper RM

The Transition table is very similar to the _____ table.

A. State Page 382
B. Truth
C. State
D. Transition

Question No:59 (Marks:1) Vu-Topper RM

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.

A. Shift Registers Page 417
B. Circular Buffers
C. Ring Buffers
D. Reduce Registers

Question No:60 (Marks:1) Vu-Topper RM

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.

A. 110
B. 101
C. 100
D. 001

Question No:61 **(Marks:1)** **Vu-Topper RM**

The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

A. NAND
B. AND
C. OR
D. NOT

Question No:62 **(Marks:1)** **Vu-Topper RM**

The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.

A. Small **Page 423**
B. Heavy
C. High
D. Normal

Question No:63 **(Marks:1)** **Vu-Topper RM**

Cin is part of _____ Adder.

A. Full
B. Half
C. Single
D. Double

Question No:64 **(Marks:1)** **Vu-Topper RM**

Which one flip-flop has an invalid output state?

A. SR
B. T
C. JK
D. DK

Question No:65 **(Marks:1)** **Vu-Topper RM**

The maximum value, represented by a single hexadecimal digit is ____.

A. "F"
B. "E"
C. "G"

D. "H"

Question No:66 **(Marks:1)** **Vu-Topper RM**

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack __.

A. Top **Page 422**

B. Bottom

C. Down

D. Vertex

Question No:68 **(Marks:1)** **Vu-Topper RM**

Adding two octal numbers "36" and "71" result in _____.

A. 127

B. 213

C. 123

D. 345

Question No:69 **(Marks:1)** **Vu-Topper RM**

The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

A. High **Page 417**

B. Low

C. Medium

D. Hot

Question No:70 **(Marks:1)** **Vu-Topper RM**

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.

A. 1001

B. 1000

C. 1111

D. 0011

Question No:71 **(Marks:1)** **Vu-Topper RM**

A multiplexer with a register circuit converts

A. Parallel data to serial **Page 356**
B. Serial data to parallel
C. Serial data to serial
D. Parallel data to parallel

Question No:72 **(Marks:1)** **Vu-Topper RM**
Implementation of Latch is required almost _____ transistor.
A. Six **Page 417**
B. Two
C. Three
D. Four

Question No:73 **(Marks:1)** **Vu-Topper RM**
The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.
A. One
B. Two
C. Three
D. Four **Page 399**

Question No:75 **(Marks:1)** **Vu-Topper RM**
The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.
A. Three **Page 362**
B. Four
C. Five
D. One

Question No:76 **(Marks:1)** **Vu-Topper RM**
Subtractors also have output to check if 1 has been _____.
A. Primed
B. Shifted
C. Complemented
D. Borrowed

Question No:77 **(Marks:1)** **Vu-Topper RM**

Question No:78 **(Marks:1)** **Vu-Topper RM**

The power consumed by a flip-flop is defined by _

A. P = Vcc x Icc **Page 235**

B. P = Icc x Rcc

C. P = Vcc x Rcc

D. P = Mcc x Vcc

Question No:79 **(Marks:1)** **Vu-Topper RM**

The low to high or high to low transition of the clock is considered to be a(n) _____

A. Edge **Page 228**

B. Add

C. Odd

D. Out

Question No:81 **(Marks:1)** **Vu-Topper RM**

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

A. **25 mW** **Page 242**

B. 10 mW

C. 64 mW

D. 1024 mW

Question No:82 **(Marks:1)** **Vu-Topper RM**

The diagram above shows the general implementation of _____ form

A. POS **Page 122**

B. COS

C. GOS

D. FOS

Question No:83 **(Marks:1)** **Vu-Topper RM**

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

A. 0
B. 1 **Page 417**
C. 2
D. 3

Question No:84 **(Marks:1)** **Vu-Topper RM**
A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?
A. 1001
B. 1011
C. 0011
D. 1100

Question No:86 **(Marks:1)** **Vu-Topper RM**
Question No:87 **(Marks:1)** **Vu-Topper RM**
A positive edge-triggered flip-flop changes its state when _____
A. Preset input (PRE) is set
B. Enable input (EN) is set
C. High-to-low transition of clock
D. **Low-to-high transition of clock** **Page 221**

Question No:88 **(Marks:1)** **Vu-Topper RM**
The asynchronous inputs are normally labeled _____ and _____, and are normally active_____ inputs.
A. **PRE, CLR, LOW**
B. ON, OFF, HIGH
C. START, STOP, LOW
D. SET, RESET, HIGH

Question No:89 **(Marks:1)** **Vu-Topper RM**
Question No:90 **(Marks:1)** **Vu-Topper RM**
In synchronous systems, the exact times at which any output can change state are determined by a signal commonly called the _____.
A. traffic

B. D
C. flip-flop
D. **Clock**

Question No:91 (Marks:1) Vu-Topper RM
Which is not an example of a truncated modulus?
A. **8**
B. 9
C. 11
D. 15

Question No:93 (Marks:1) Vu-Topper RM
A Nibble consists of _____ bits
A. **4** **Page 394**
B. 6
C. 8
D. 10

Question No:94 (Marks:1) Vu-Topper RM
Question No:96 (Marks:1) Vu-Topper RM
When an eight bit serial in/serial out shift register is used for a 24 micro seconds time delay, the clock frequenct must be Select correct option:
A. 41.67 KHz
B. **333 KHz**
C. 125 KHz
D. 8 MHz

Question No:97 (Marks:1) Vu-Topper RM
Question No:99 (Marks:1) Vu-Topper RM
Question No:100 (Marks:1) Vu-Topper RM
A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is:
A. **1111**
B. 1110

C. 0001
D. 1000

Question No:101 (Marks:1) Vu-Topper RM
A divide-by-10 ring counter requires a minimum of
A. Twelve flip-flops
B. Four flip-flops
C. **Ten flip-flops** **Google**
D. Five flip-flops

Question No:102 (Marks:1) Vu-Topper RM
A 32-bit data word consists of:
A. 2 Byte
B. **4 Byte** **Google**
C. 6 Byte
D. 8 Byte

Question No:103 (Marks:1) Vu-Topper RM
Which of the following memories uses one transistor and one capacitor as basic memory unit?
A. ROM
B. PROM
C. RAM
D. **DRAM** **Google**

Question No:105 (Marks:1) Vu-Topper RM
Each stage of Master-slave flip-flop works at ____ of the clock signal
A. **One half**
B. Full
C. Center
D. None

Question No:106 **(Marks:1)** **Vu-Topper RM**

In memory read cycle, the read cycle is initiated by

A. **Applying the address signals** **Page 397**

B. Digital

C. Analog

D. None

Question No:107 **(Marks:1)** **Vu-Topper RM**

The chip enable access time which is the time for the valid data to appear after the _____ transition of the chip select signal ¯CS.

A. **High-to-low** **Page 397**

B. Low -to-high

C. High

D. Low

Question No:108 **(Marks:1)** **Vu-Topper RM**

The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

A. **Faster** **Page 406**

B. Slow

C. High

D. None

Question No:109 **(Marks:1)** **Vu-Topper RM**

Question No:110 **(Marks:1)** **Vu-Topper RM**

A memory organized to store nibble data values requires a _____ wide data bus.

A. **4-bit** **Page 390**

B. 2

C. 3

D. 1

Question No:111 **(Marks:1)** **Vu-Topper RM**

If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

A. **Very different** **Page 1**
B. Simple
C. Slow
D. Difficult

Question No:112 **(Marks:1)** **Vu-Topper RM**

A 8-bit serial in / parallel out shift register contains the value "8", clock signal(s) will be required to shift the value completely out of the register.

A. **8** **Page 356**
B. 6
C. 4
D. 2

Question No:113 **(Marks:1)** **Vu-Topper RM**

The terminal count of a modulus -13 binary counter is

A. **1101**
B. 1111
C. 0000
D. 1100

Question No:114 **(Marks:1)** **Vu-Topper RM**

THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____

A. NOT
B. XOR
C. GATE
D. **OR** **Page 171**

Question No:115 **(Marks:1)** **Vu-Topper RM**

Number of states in an 8-bit Johnson counter sequence are:

A. 12

B. **8** **Page 347**

C. 4

D. 16

Question No:117 **(Marks:1)** **Vu-Topper RM**

Consider A=1, B=0, C=1. A, B and C represent the input of three-bit NAND gate, the output of the NAND gate will be _____.

A. **One** **Page 46**

B. Two

C. Three

D. Four

Question No:118 **(Marks:1)** **Vu-Topper RM**

The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

A. **4** **Page 278**

B. 6

C. 2

D. 8

Question No:119 **(Marks:1)** **Vu-Topper RM**

For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minter) present in the expression.

A. 1 **Page 90**

B. 2

C. 3

D. 4

Question No:120 **(Marks:1)** **Vu-Topper RM**

Two signals _____ and _____ provide the timing inputs to the State Machine.

A. LTIME and STIME **Page 374**
B. NSSR and EWSR
C. LTIME and STIME
D. PTIME and QTIM

Question No:121 **(Marks:1)** **Vu-Topper RM**
Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

A. $\overline{WE}$ **Page 397**
B. CS
C. VS
D. OE

Question No:122 **(Marks:1)** **Vu-Topper RM**
Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.

A. RAM **Page 420**
B. ROM
C. Both
D. None

Question No:123 **(Marks:1)** **Vu-Topper RM**
The output of a NAND gate is _____ when all the inputs are one.

A. Zero **Page 47**
B. One
C. Available
D. Not available

Question No:124 **(Marks:1)** **Vu-Topper RM**
Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minters) with an 8-input OR gate.

A. 8 AND

B. 8 OR
C. 8 NOT
D. 8 XOR

Question No:125 (Marks:1) Vu-Topper RM

In Master-Slave flip-flop the Clock signal is connected to Slave flip-flip using _____ gate

A. NOT
B. OR
C. AND
D. XOR

Question No:127 (Marks:1) Vu-Topper RM

Smallest unit of binary data is a _____

A. Bit Page 387
B. Byte
C. Char
D. None

Question No:128 (Marks:1) Vu-Topper RM

To parallel load a byte of data into a shift register, there must be

A. One clock pulse
B. Two clock pulse
C. Three clock pulse
D. Four clock pulse

Question No:129 (Marks:1) Vu-Topper RM

Stack is an acronym for _____

A. LIFO memory Page 429
B. FIFO memory
C. Both
D. None

Question No:130 **(Marks:1)** **Vu-Topper RM**

The 4-bit 2"s complement representation of "+5" is _____

A. 0101

B. 1010

C. 0011

D. 1000

Question No:131 **(Marks:1)** **Vu-Topper RM**

The OR gate performs Boolean _____.

A. Addition **Page 42**

B. Old

C. Multiply

D. Sub

Question No:132 **(Marks:1)** **Vu-Topper RM**

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop of the shift register.

A. Ring counter **Page 355**

B. Star counter

C. Bus counter

D. System counter

Question No:134 **(Marks:1)** **Vu-Topper RM**

Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.

A. XNOR **Page 262**

B. NOT

C. OR

D. AND

Question No:135 **(Marks:1)** **Vu-Topper RM**

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

A. 80 micro seconds

B. 20 micro seconds
C. 40 micro seconds
D. 60 micro seconds

Question No:136 (Marks:1) Vu-Topper RM

The design and implementation of synchronous counters start from ___.

A. State diagram Page 319
B. level diagram
C. Both
D. None of the these

Question No:137 (Marks:1) Vu-Topper RM

In Synchronous systems, the output of all the digital circuits changes when an enable signal is applied instead of the clock signal.

A. True
B. False Page 228

Question No:138 (Marks:1) Vu-Topper RM

Question No:139 (Marks:1) Vu-Topper RM

A mono-stable device only has a single stable state----------

A. True Page 262
B. False

Question No:142 (Marks:1) Vu-Topper RM

When an Op-Amp is used as an inverting amplifier, the input signal is applied at its Inverted input through a _____resistance.

A. Parallel
B. Series Page 439

Question No:143 (Marks:1) Vu-Topper RM

In asynchronous digital systems all the circuits change their state with respect to a common clock

A. False Page 245

B. True

Question No:144 (Marks:1) Vu-Topper RM

Question No:145 (Marks:1) Vu-Topper RM

3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

A. True Page 161

B. False

Question No:146 (Marks:1) Vu-Topper RM

Memory is arranged in _____.

A. Two-dimensional manner Page 396

B. linear fashion

Question No:147 (Marks:1) Vu-Topper RM

A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BYTHE MANUFACTURER.

A. True Page 182

B. False

Question No:148 (Marks:1) Vu-Topper RM

A _____ can not operate without a memory element.

A. Counter Page 211

B. Register

Question No:150 (Marks:1) Vu-Topper RM

A complete unit of information is sometimes called a _____.

A. Word Page 387

B. Byte

Question No:151 (Marks:1) Vu-Topper RM

If a circuit suffers “Clock Skew “ problem, the output of circuit can’t be guarantied.

A. True
B. False

Question No:152 **(Marks:1)** **Vu-Topper RM**
The combinational digital circuits have _____ storage element; therefore, combinational circuits handle only instantaneous inputs.
A. No **Page 210**
B. Yes

Question No:153 **(Marks:1)** **Vu-Topper RM**
Following is standard POS expression
A. True
B. False

Question No:154 **(Marks:1)** **Vu-Topper RM**
Question No:155 **(Marks:1)** **Vu-Topper RM**
Question No:156 **(Marks:1)** **Vu-Topper RM**
To write data to the memory the memory the write cycle is initiated by
A. Applying the address signals **Page 397**
B. Applying the digital address

Question No:157 **(Marks:1)** **Vu-Topper RM**
Question No:158 **(Marks:1)** **Vu-Topper RM**
A-stable multi-vibrator is an Oscillator which does not have any_____.
Astable Multivibrator **Google**

Question No:159 **(Marks:1)** **Vu-Topper RM**
The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as ____ inputs.
Synchronous

Question No:160 **(Marks:1)** **Vu-Topper RM**
UVEPROM is stands for----------

Ultra-Violet Erasable Programmable Read Only Memory.

Question No:161 (Marks:1) Vu-Topper RM

--------are implemented by combining combinational circuits with memory elements.

A. PLA
B. PLDS
C. System
D. Sequential circuits Page 211

Question No:162 (Marks:1) Vu-Topper RM

The EPROM uses_____array with an isolated-gate structure.

NMOSFET Page 411

Question No:163 (Marks:1) Vu-Topper RM

A one-shot mono-stable device contains _____

NOR gate, Resistor, Capacitor and NOT Gate

Question No:164 (Marks:1) Vu-Topper RM

In sequential circuits memory elements are connected with_____.

Common clock

Question No:165 (Marks:1) Vu-Topper RM

The alternate solution for a multiplexer and a register circuit is ____.

Parallel in / Serial out shift register Page356

Question No:166 (Marks:1) Vu-Topper RM

Which of the following output equations determines the output of the state machine?

Max-Q0Q1EN Page 382

Question No:167 (Marks:1) Vu-Topper RM

The

CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

CONSTATE

Question No:168 (Marks:1) Vu-Topper RM

Question No:169 (Marks:1) Vu-Topper RM

Why demultiplexer is called a data distributor?

Single input to Single Output

Question No:170 (Marks:1) Vu-Topper RM

The AND Gate performs a logical _____ function.

Multiplication Page 40

Question No:171 (Marks:1) Vu-Topper RM

The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

AND,OR Page 146

Question No:172 (Marks:1) Vu-Topper RM

The domain of the expression AB'CD + AB' + C'D + B is

A, B, C and D

Question No:173 (Marks:1) Vu-Topper RM

When the transmission line is idle in an asynchronous transmission

A. It is set to logic high Page 349

B. It is set to logic low

C. It remains in previous state

D. State of transmission line is not used to start transmission

Question No:175 (Marks:1) Vu-Topper RM

Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

Negative-OR, Negative-AND Page 74

Question No:176 (Marks:1) Vu-Topper RM
An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.

A. Q output of all flip-flops to J input of next flip-flops
B. Q' output of all flip-flops to K input of next flip-flops
C. Q output of all flip-flops to clock input of next flip-flops
D. Q' output of all flip-flops to clock input of next flip-flops

Question No:177 (Marks:1) Vu-Topper RM
WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -------
THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED

Question No:178 (Marks:1) Vu-Topper RM
The _____ Encoder is used as a keypad encoder.
Decimal-to-BCD Priority Page 166

Question No:179 (Marks:1) Vu-Topper RM
NOR gate is formed by connecting _____
OR Gate and then NOT Gate Page 47

Question No:180 (Marks:1) Vu-Topper RM
A particular half adder has
2 INPUTS AND 2 OUTPUT Page 134

Question No:181 (Marks:1) Vu-Topper RM
Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to .
Toggle

Question No:182 (Marks:1) Vu-Topper RM
A stage in the shift register consists of

A flip flop

Question No:183 (Marks:1) Vu-Topper RM

flip-flops are obsolete now.

Master-Slave

Question No:184 (Marks:1) Vu-Topper RM

In Master-Slave flip-flop setup, the master flip-flop operators at

Both Master-Slave operator simultaneously Page 230

Question No:185 (Marks:1) Vu-Topper RM

Question No:186 (Marks:1) Vu-Topper RM

A transparent mode means _____

A. Input Hold time is zero (no need to maintain input after clock transition)
B. The changes in the data at the inputs of the latch are not seen at the output
C. The changes in the data at the inputs of the latch are seen at the output Page 245
D. Propagation Delay is zero (Output is immediately changed when clock signal is applied)

Question No:187 (Marks:1) Vu-Topper RM

In _____ outputs depend only on the current state.

Moore Machine Page 332

Question No:188 (Marks:1) Vu-Topper RM

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

State assignment

Question No:189 (Marks:1) Vu-Topper RM

Question No:190 (Marks:1) Vu-Topper RM

Question No:191 **(Marks:1)** **Vu-Topper RM**

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?

A. J = 1, K = 0

B. J=X(Don’tcare),K=0

C. J = 1, K = X(Don't care)

D. J = 0, K = X(Don't care)

Question No:192 **(Marks:1)** **Vu-Topper RM**

Invalid state of NOR based SR latch occurs when _____.

S=1, R=1

Question No:193 **(Marks:1)** **Vu-Topper RM**

74HC163 has two enable input pins which are _____ and _____

ENP, ENT

Question No:194 **(Marks:1)** **Vu-Topper RM**

Question No:195 **(Marks:1)** **Vu-Topper RM**

In asynchronous transmission when the transmission line is idle, ___

It is set to logic high **Page 356**

Question No:196 **(Marks:1)** **Vu-Topper RM**

LUT is acronym for _____

Look Up Table **Page 439**

Question No:197 **(Marks:1)** **Vu-Topper RM**

The three fundamental gates are _____

NOT, OR, AND **Page 40**

Question No:198 **(Marks:1)** **Vu-Topper RM**

The total amount of memory that is supported by any digital system depends upon _____

The size of the address bus of the microprocessor **Page 430**

Question No:199 **(Marks:1)** **Vu-Topper RM**

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Fist In First Out Memory **Page 425**

Question No:200 **(Marks:1)** **Vu-Topper RM**

A flip-flop changes its state when _____

Low-to-high transition of clock **Page 228**

Question No:201 **(Marks:1)** **Vu-Topper RM**

In a sequential circuit the next state is determined by ____and -----

Input and clock signal applied **Page 305**

Question No:202 **(Marks:1)** **Vu-Topper RM**

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

Accuracy **Page 460**

Question No:203 **(Marks:1)** **Vu-Topper RM**

Above is the circuit diagram of _____.

Asynchronous up-counter **Page 270**

Question No:204 **(Marks:1)** **Vu-Topper RM**

The sequence of states that are implemented by a n-bit Johnson counter is

2n (n multiplied by 2) **Page 354**

Question No:205 **(Marks:1)** **Vu-Topper RM**

"A + B = B + A" is _____

Commutative Law

Question No:206 **(Marks:1)** **Vu-Topper RM**

An alternate method of implementing Comparators which allows the

Comparators to be easily cascaded without the need for extra logic gates is _____

Using Iterative Circuit based Comparators Page 155

Question No:207 (Marks:1) Vu-Topper RM

DE multiplexer is also called

Data distributor Page 178

Question No:208 (Marks:1) Vu-Topper RM

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs Page 332

Question No:209 (Marks:1) Vu-Topper RM

The alternate solution for a demultiplexer-register combination circuit is

Serial in / Parallel out shift register Page 356

Question No:210 (Marks:1) Vu-Topper RM

The storage cell in SRAM is

A capacitor Page 407

Question No:211 (Marks:1) Vu-Topper RM

What is the difference between a D latch and a D flip-flop?

The D flip-flop has a clock input.

Question No:212 (Marks:1) Vu-Topper RM

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

Access Time Page 417

Question No:213 (Marks:1) Vu-Topper RM

THE HOURS COUNTER IS IMPLEMENTED USING _____

A SINGLE DECADE COUNTER AND A FLIP-FLOP

Question No:214 **(Marks:1)** **Vu-Topper RM**

The high density FLASH memory cell is implemented using _____

1 floating-gate MOS transistor **Page 419**

Question No:215 **(Marks:1)** **Vu-Topper RM**

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

Q2:= Q1 # X # Q3 **Page 210**

Question No:216 **(Marks:1)** **Vu-Topper RM**

The output of an AND gate is one when _____

All of the inputs are one **Page 40**

Question No:217 **(Marks:1)** **Vu-Topper RM**

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

A > B = 1, A < B = 0, A = B = 0 **Page 109**

Question No:218 **(Marks:1)** **Vu-Topper RM**

The device shown here is most likely a

Multiplexer

Question No:219 **(Marks:1)** **Vu-Topper RM**

DE multiplexer converts _____ data to _____data

Serial data, parallel data **Page 356**

Question No:220 **(Marks:1)** **Vu-Topper RM**

The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called_____

In-System Programming (ISP) **Page 194**

Question No:221 **(Marks:1)** **Vu-Topper RM**

In _____ outputs depend only on the combination of current state and inputs.

Mealy machine **Page 332**

Question No:222 **(Marks:1)** **Vu-Topper RM**

In the following statement Z PIN 20 ISTYPE „reg.invert";

Active-low Registered Mode output

Question No:223 **(Marks:1)** **Vu-Topper RM**

The process of converting the analogue signal into a digital representation (code) is known as _____

Quantization **Page 445**

Question No:224 **(Marks:1)** **Vu-Topper RM**

In elevator circuit, the floor display circuit is a combinational circuit which uses the _____ and _____ inputs two determine the floor number and the direction of the display arrow.

A. OPEN, DIR
B. MOTION, FB
C. CONSTATE, FB
D. MOTION and DIR **Page 374**

Question No:225 **(Marks:1)** **Vu-Topper RM**

Question No:228 **(Marks:1)** **Vu-Topper RM**

The GAL16V8 has_____.

A. 16 dedicated inputs
B. 8 special function pins
C. 8 pins that are used as inputs or outputs
D. All of the these **Page 200**

Question No:229 **(Marks:1)** **Vu-Topper RM**

The tri-state buffer connecting the output of the OLMC circuit to the output pin is controlled through _____ different sources.

A. One
B. Two
C. Four **Page 200**

D. Three

Question No:230 (Marks:1) Vu-Topper RM

In gated SR latch, what is the value of the output if EN=1, S=0 and R=0?

A. 1
B. 2
C. 3
D. 4

Question No:232 (Marks:1) Vu-Topper RM

To serially shift a byte of data into a shift register, there must be

A. One load pulse
B. One clock pulse
C. Eight clock pulses
D. One clock pulse for each 1 in the data

Question No:238 (Marks:1) Vu-Topper RM
Question No:239 (Marks:1) Vu-Topper RM

A NOR based S-R latches maintain the output state when both the set and reset inputs are _____.

A. Active
B. Invalid
C. Inactive Page 215
D. Consistent

Question No:240 (Marks:1) Vu-Topper RM

The absence of a _____ element in sequential circuit restricts the use of digital combinational circuits to certain application areas.

A. Memory Page 210
B. Logic
C. Both
D. None

Question No:242 (Marks:1) Vu-Topper RM

A Quad 1-of-4 MUX has four Multiplexers, each multiplexer has_____ inputs and a single output.

A. 2
B. 4 **Page 209**
C. 6
D. 8

Question No:243 **(Marks:1)** **Vu-Topper RM**

The _____ description is used to simulate the logic circuit and verify its operation.

A. Logic
B. Test file
C. Test vector **Page 207**
D. Declaration