

CS302 Quiz No.01 Solution Fall2021

Quiz #1 (1 to 20) Lectures♥

Inputs          Output

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

This function table represents \_\_\_\_\_ Gate.

Or gate

The ABEL symbol for “OR” operation is

#

A standard SOP form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.

Sum

Which one of the following is not a valid rule of Boolean algebra?

$$A = \bar{A}$$

How many data select lines are required for selecting eight inputs?

3 (correct)

If two adjacent 1s are detected in the input, the output is set to high. Input combinations will be

0011(ans)

The 4-variable Karnaugh Map (K-Map) has \_\_\_\_\_ rows and \_\_\_\_ columns

4,4, (ans)

The boolean expression  $A + B' + C$  is

A sum term(ans)

The boolean expression  $AB'CD'$  is

A product term(ans)

Don't care conditions are marked as \_\_\_\_\_ in the output column of the function table

X(ans)

An example of SOP expression is

Both (a) and (b)(ans)

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1 (ans)

A SOP expression having a domain of 3 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.

Select correct option:

2 (Correct)

Multiplexers are also known as \_\_\_\_\_.

**Data Selectors**

The OR Gate performs a Boolean \_\_\_\_\_ function

Addition (Correct)

Sum term (Max term) is implemented using \_\_\_\_\_ gates

OR (Correct)

The number "1259" may belong to \_\_\_\_\_ number system.

Binary or Hexadecimal system (Correct)

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result

1111 (Correct)

"1101" in signed representation is equivalent to \_\_\_\_\_

13 (Correct)

TTL based devices work with a dc supply of \_\_\_\_ Volts

+5 (Correct)

In decimal value "275" the weight of the digit "7" is \_\_\_\_\_

100 (Not Sure)

The decimal "10" will have an octal equivalent \_\_\_\_\_

9 (Not Sure)

Caveman number system is Base \_\_\_\_\_ number system

5 (Correct)

How many bits must each word have in one-to-four line de-multiplexer to be implemented using a memory?

1 bits

The total amount of memory is depends upon \_\_\_\_\_

The size of the address bus of the microprocessor

\_\_\_\_\_ can be determined the Instability condition.

### Logic diagram

If we add an inverter at the output of AND gate, what function is produced?

### NAND

Which is also known as coincidence detector?

### AND gate

Transition table include \_\_\_\_\_

### Squares

For every possible combination of logical states in the inputs, which table shows the logical state of a digital circuit output?

### Truth table

Stack is an acronym for \_\_\_\_\_

### LIFO memory

When an Asynchronous sequential circuit changes two or more binary states variables a Condition occurs called \_\_\_\_\_

### Race condition

Positive OR gate is also a negative

### AND gate

Time delay device is memory element of \_\_\_\_\_

### Asynchronous circuits

Boolean algebra is also called

- a) Arithmetic algebra
- b) Switching algebra

c) Both A & B

Boolean function must be brought into \_\_\_\_\_ To perform product of max terms

### OR terms

The binary number 10101 is equivalent to the decimal number \_\_\_\_\_.

21

The domain of expression  $ABCD + AB + CD + B$  is—

B only

The Boolean expression  $A BC D$  is—

Sum term

The universal gate is\_\_\_\_\_.

NAND gate

According to boolean algebra absorption law, which of the following is correct?

$Xy+y=x$

A Boolean function may be transformed into

Logical diagram

The inverter is \_\_\_\_\_

NOT gate

The resulting circuit of a NAND gate are connected together is\_\_\_\_\_

NOT gate

$X*y = y*x$  is the

Identity element

Minterms are also called

Standard product

OR gate and \_\_\_\_\_ will form The NOR gate?

NOT gate

The NAND gate is AND gate followed by .....

NOT gate

Max terms are also called \_\_\_\_\_.

Standard sum

In Boolean algebra Multiplicative inverse is

A

By the repeated use of \_\_\_\_\_ Digital circuit can be made

NAND gates

The only function of NOT gate is \_\_\_\_\_ of the following.

Invert input signal

Boolean algebra is defined as a set of \_\_\_\_\_.

Two values

First operator precedence for evaluating Boolean expressions is

Parenthesis

The output is \_\_\_\_\_ When an input signal 1 is applied to a NOT gate

0

The bar sign (-) indicates \_\_\_\_\_ In Boolean algebra?

NOT operation

The value of n is \_\_\_\_\_ when the resolution of an n bit DAC with a maximum input of 5 V is 5 mV.

10

2's complement of binary number 0101 is \_\_\_\_\_

1011

An OR gate has 4 inputs. The output is ..... When One input is high and the other three are low.

High

To convert BCD to seven segments \_\_\_\_\_ device is used.

Decoder

Decimal number 10 is equal to binary number \_\_\_\_\_.

1010

In 2's complement representation the number 11100101 represents the decimal number \_\_\_\_\_.

-27

BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are\_\_\_\_\_.

All

A decade counter skips \_\_\_\_\_.

Binary states 1010 to 1111

\_\_\_\_\_ Number of States A ring counter with 5 flip flops will have?

5

Positive edge-triggered flip-flop changes its state when \_\_\_\_\_

Low-to-high transition of clock

If S=1 and R=1, for negative edge triggered flip-flop then  $Q(t+1) =$  \_\_\_\_\_

Invalid

Adjacent 1s detector circuit will have active low output for the input

1101

A 5-variable karnaugh map has

Thirty two cells

8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer

8-to-1 ok

In asynchronous digital systems all the circuits change their state with respect to a common clock

False

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 16

The Synchronous counters are also known as Ripple Counters:

False ok

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

The 3-to-8 Decoder has active-low outputs and three extra \_\_\_\_ gates connected at the three inputs to reduce the four unit load to a single unit load.

Not

Which of the number is not a representative of hexadecimal system?

“1001” correct

High level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_

0.9 V correct

To get the answer “1” in Boolean addition of three variables, \_\_\_\_\_

One of the variables must be 1 correct

The 3-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms

8 correct

\_\_\_\_\_ is invalid number of cells in a single group formed by the adjacent cells in K-map

2 correct

Consider  $A=1, B=0, C=1$ . A, B and C represent the input of three bit NAND gate the output of the NAND gate will be \_\_\_\_\_

Zero

The Binary number 1011.101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_\_ separated by a decimal point.

1011, 101 correct

$1011+101 =$  \_\_\_\_\_

10000 correct

Adding two octal numbers "36" and "71" result in \_\_\_\_\_

127 correct

The first Least Most digit in decimal number system has

Has position 0 and weight equal to 1 not sure

Sum term (Max term) is implemented using \_\_\_\_\_ gates

OR correct

The OR Gate performs a Boolean \_\_\_\_\_ function

Addition correct

Adding two octal numbers "36" and "71" result in \_\_\_\_\_

127 correct

If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be \_\_\_\_\_

24582 not sure

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

TRUE correct

The three fundamental gates are \_\_\_\_\_

NOT, OR, AND correct

A SOP expression having a domain of 3 variables will have a truth table having \_\_\_\_ combinations of inputs and corresponding output values.

8 correct

The 4-variable K-Map has \_\_\_\_\_ rows and \_\_\_\_\_ columns of cells.

4, 4 correct

NAND gate is form by connecting \_\_\_\_\_

AND Gate and then NOT Gate correct

Which of the following is the octal equivalent of 28 decimal number?

34

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

$(2^{64})-1$

In a 4-variable K-map, a 2-variable product term is produced by

A 4-cell group of 1s

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term present in the expression.

1

The \_\_\_\_\_ input select/deselects both the decoders simultaneously.

Enable

NAND and \_\_\_\_\_ gates are known as Universal Gates.

NOR

The declaration section of ABEL generally includes the device declaration, \_\_\_\_\_ declarations and set declarations.

Pin

An SOP expression having a domain of 2 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.

4

In the 32-bit Single Precision Floating formation, the exponent value \_\_\_\_\_ is reserved to represent 0 exponents.

0

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

Slow

The complement of a variable is always

The inverse of the variable

$A(B + C) = A.B + A.C$  is the expression of \_\_\_\_\_.

Distributive Law

If the number 2025 is represented in floating point, then exponent is \_\_\_\_\_.

3

Excess-8 code of -6 is \_\_\_\_\_.

0010

A 3-variable Karnaugh map has

Eight cells

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is \_\_\_\_\_ to the range of values that are to be represented.

### Proportional

Suppose we want to transmit the data "10001101" and an "Even-Parity" bit scheme is used to detect errors, the parity bit added to the data will be\_\_\_\_\_.

### Both "0" and "1" can be used

The carry propagation delay problem in parallel binary adder can be solved by \_\_\_\_\_.

Using two full adders

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a \_\_\_\_\_ multiplexer.

2-input, 8-bit

The octal equivalent of the following binary number is \_\_\_\_\_.

117

A' is written in ABEL as\_\_\_\_\_.

!A

Which of the following is the hexadecimal equivalent of 28?

1C

High Level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_.

0.9 V

Adjacent 1s detector circuit will have active high output for the input.

0011

Modern information techniques are relying more on \_\_\_\_\_ transmission.

Digital

The \_\_\_\_\_ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.

Two

How many data select lines are required for selecting eight inputs?

3

Select the mode of programming in which GAL 16V8 can be programmed.

All of the given option

\_\_\_\_\_ has the fastest switching speed and low power requirement.

Advanced low power Schottky

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_.

0.1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called \_\_\_\_ of the flip-flop.

Hold time

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

Each stage of Master-slave flip-flop works at \_\_\_\_ of the clock signal.

One half

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using \_\_\_\_

NOT

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is \_\_\_\_

1111

\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

Race condition

The Synchronous counters are also known as Ripple Counters:

False

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the \_\_\_\_

Set-up time

The n flip-flops store \_\_\_\_ states.

$2^n$

When the \_\_\_\_ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of \_\_\_\_

1,2

A positive edge-triggered flip-flop changes its state when \_\_\_\_

Low-to-high transition of clock

A decade counter is \_\_\_\_

Mod-10 counter

The look-ahead carry circuits\_\_\_\_\_

Reduce propagation delay

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_ is added to the result

0110

Both the multiplexers are selected simultaneously when \_\_\_\_\_ is set to logic \_\_\_\_\_ in 2-inputs, 8-bit Multiplexer.

G, Low

Function labels required to represent the input/output combinations for each segment in 7-segment display

7

Multiplexers are also known as \_\_\_\_\_

Data selectors

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_

0, 1

Cin is part of \_\_\_\_\_ Adder.

Full

The look-ahead carry circuits\_\_\_\_\_

Reduce propagation delay

Which of the following gates has the outputs 1 if and only if at least one input is 1?

OR

A sop expression can be implemented by on \_\_\_combination of gates.

AND-OR

The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through \_\_\_ ALU units in 16-bit ALU.

Four

Digital circuits operates with \_\_\_\_\_ voltage value(s)

2

In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles \_\_\_\_\_

Lower priority outputs

To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_\_\_ variable Karnaugh maps are used.

4

The output of a NAND Gate is \_\_\_\_\_ when all the inputs are one.

Zero

The \_\_\_\_\_ is the slowest and consumes more power.

Standard TTL

The between expression  $X-AB+CD$  represents

Two ANDs ORed together

The expression  $F = A + B + C$  describes the operation of three bits \_\_\_ Gate.

OR

Which one of the following is NOT a valid rule of Boolean Algebra?

$A = A'$

A 5-Variable Karnaugh map has

Thirty two cells

\_\_\_ is invalid number of cells in a single group formed by the adjacent cells K-map

12

In 32-bit Single –Precision floating point format representation the range of exponent value is from \_\_\_ to \_\_\_

+127 to -126

\_\_\_\_\_ has the fastest switching speed and low power requirements

Advanced low power schottky

Which of the following is a volatile memory?

DRAM

\_\_\_\_\_ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

Combinational Input

The AND Gate performs a logical \_\_\_\_\_ function.

Division

The Adjacent 1s Detector accepts 4-bit inputs. If \_\_\_\_\_ adjacent 1s are detected in the input, the output is set to high.

1

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

The FAST Model Page Access allows \_\_\_\_\_ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a \_\_\_\_\_ with a \_\_\_\_\_.

Row, column

Which of the following Output Equations determines the output of the State Machine?

MAX = QQQ1EN

The maximum value, represented by a single hexadecimal digit is \_\_\_\_\_.

“F”

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a \_\_\_\_\_.

1

The Static Ram (SRAM) is non-volatile and is not a \_\_\_\_\_ density memory as a latch is required to store a single bit of information.

High

Demorgan's two theorems prove the equivalency of the NAND and \_\_\_\_\_ gates and the NOR and \_\_\_\_\_ gates respectively.

Negative-OR, Negative-AND

Two signals \_\_\_\_\_ and \_\_\_\_\_ provide the timing inputs to the State Machine.

PTIME and QTIME

The 74HC163 is a 4-bit Synchronous counter, it has \_\_\_\_\_ data output pins.

4

PLDs have In-System Programming (ISP) capability that allows the \_\_\_\_\_ to be programmed after they have been installed on a circuit board.

PLDs

The CONSTATE.CLK = Clock is used to indicate that the \_\_\_\_\_ state variables change on a clock transition.

CONSTATE

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using \_\_\_\_\_.

Shift Registers

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as \_\_\_\_\_ inputs.

Synchronous

For a down counter that counts from (111 to 000), if current state is "101" the next state will be \_\_\_\_\_.

None of the given

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

XOR, NAND

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to \_\_\_\_\_ location(s) using a single address.

Four

In NAND based S-R latch, output of each \_\_\_\_\_ gate is connected to the input of the other \_\_\_\_\_ gate.

NAND, NAND

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires \_\_\_\_\_ gates for the 8 product terms (minterms) with an 8-input OR gate.

8 AND

8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer.

8-to-1

The \_\_\_\_\_ input overrides the \_\_\_\_\_ input.

Asynchronous, synchronous

A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.

AND-OR

The 64-cell array organized as 8 x 8 cell array is considered

As an 8 byte memory

The terminal count of a 4-bit binary counter in the UP mode is \_\_\_\_\_.

1100

A 3-variable karnaugh map has

Eight cells

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_.

Q output of all flip-flops to clock input of next flip-flops

Memory is arranged in \_\_\_\_\_.

Two-dimensional manner

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result.

1001

Subtractors also have output to check if 1 has been \_\_\_\_\_.

Primed

The Test Vector definition defines the test vectors for all the three counter inputs and \_\_\_\_\_ counter output/outputs.

Three

A multiplexer with a register circuit converts

Parallel data to serial

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

The n flip-flops store \_\_\_\_\_ states.

$2^n$

The S-R latch has two inputs, therefore \_\_\_\_\_ different combinations of inputs can be applied to control the operation of the S-R latch.

Four

Why demultiplexer is called a data distributor?

Single input to Single Output

When the transmission line is idle in an asynchronous transmission

It is set to logic high

UVERPROM is stands for

Ultra-Violet

In memory write cycle, the time for which the WE signal remains active is known as the \_\_\_\_\_.

Write pulse width

The outputs of SR latches in elevator state machine are feed back to the \_\_\_\_\_ gate array for connection to the D-flipflops.

AND

PALs tend to execute \_\_\_\_\_ logic.

SOP

The ROM used by a computer is relatively \_\_\_\_\_ as it stores few buyers of code used to Boot the Computer system on power up.

Small

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration  $t_{WD}$ ?

-WE

You have to choose suitable option when your timer will reset by considering this given code:

```
TRSTATE.CLK = clk;
```

```
TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);
```

NSY2 or EWY2

A NOR based S-R latch is implemented using \_\_\_\_\_ gates instead of \_\_\_\_\_ gates.

NOR, NAND

Implementation of Latch is required almost \_\_\_\_\_ transistor.

Six

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in \_\_\_\_\_ when Distributed refresh is used.

7.8 microsec

The NOR logic gate is the same as the operation of the \_\_\_\_\_ gate with an inverter connected to the output.

NAND

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1

Select the mode of programming in which GAL16V8 can be programmed:

All of the given

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 32

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the \_\_\_\_\_ can be pressed at any time either on the first floor or the second floor in elevator.

REQ1

Consider  $A=1, B=0, C=1$ . A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be \_\_\_\_\_.

One

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1111

Adding two octal numbers "36" and "71" result in \_\_\_\_\_.

127

The ABEL Input file can use a \_\_\_\_\_ instead of the equation to specify the Boolean expressions.

Truth Table

The domain of the expression  $AB'CD + AB' + C'D + B$  is

A, B, C and D

If the number of samples that are collected is reduced by half, the reconstructed signal will be \_\_\_\_\_ from/to the original.

Same

In DRAM read cycle R /W- signal is activated to read data which is made available on the \_\_\_\_\_ data line.

D(OUT)

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

True

Implementation of the FIFO buffer in \_\_\_\_\_ is usually takes the form of a circular buffer.

RAM

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack \_\_\_\_\_.

Top

Which one flip-flop has an invalid output state?

SR

The output of a NAND gate is \_\_\_\_\_ when all the inputs are one.

Zero

The Transition table is very similar to the \_\_\_\_\_ table.

State

Consider the sum of weight method for converting decimal into binary value, \_\_\_\_\_ is the highest weight for 411.

256

Canonical form is a unique way of representing \_\_\_\_\_.

SOP

\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously.

Synchronous

Cin is part of \_\_\_\_\_ Adder.

Full

Flash memories Operation are classified into \_\_\_\_\_ different operation.

Two

A Product term is 0 when \_\_\_\_\_

Any one literal is 0

In 8-input multiplexer, the two outputs are connected through a/an \_\_\_ gate.

OR

\_\_\_\_\_ Device dissipate varying amount of power depending upon the frequency of operation.

CMOS

Boolean Addition operation is performed by a(an) \_\_\_ gate.

OR

A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.

AND-OR

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

$(2^{64})-1$

In 16-bit ALU, The G output is activated if the 4-bit unit generate a Carry \_\_\_\_\_ irrespective of Carry\_\_\_\_\_.

Out,In

A standard POS form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.

Sum

In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles\_\_\_\_\_.

Lower priority inputs

Which of the following is the example of comparater?

XNOR

IN CMOS 5 Volt series, Input voltage of Logic high signal ( $V_{IH}$ ) with a ranges from \_\_\_\_ to \_\_\_\_ volts.

3,5,5

The Adjacent 1 S Detector accepts 4-bits input. If \_\_\_\_ adjacent 1S are detected in the input, the output is set to high.

4

DE Morgan's two theorems prove the equivalency of the NAND and \_\_\_\_ gates and the NOR and \_\_\_\_ gates respectively.

Negative-AND, Negative-OR

Adding two octal numbers "36 and 71" result in \_\_\_\_.

127

Any of the \_\_\_\_ forms of the Karnaugh Map can be used to simplify Boolean expressions

Four

Quine-McCluskey and K-Map methods are used for \_\_\_\_\_ of Boolean expression.

Simplification

The number "1259" may belong to \_\_\_\_\_ number system.

Decimal or Hexadecimal system

The series of TTL chips are characterized by their \_\_\_\_\_.

Switching Speed only

All ABEL statements must end with \_\_\_\_\_.

;

In sequential circuit memory elements are connected with \_\_\_\_\_.

Clock

In the 32-bit Single Precision Floating Point format, the exponent value \_\_\_\_\_ is reserved to represent infinity exponents.

255

The \_\_\_\_\_ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

PLA

The limitation in implementation of parallel binary address is known as \_\_\_\_\_.

Carry input

The Gray code is different from the unsigned binary code because \_\_\_\_\_.

Successive value of Gray code by only one bit

Removing the NOT gate at the output of the NOR gate result in an \_\_\_\_\_.

OR gate

Portable devices that run on batteries use \_\_\_ circuit that have low power dissipation.

Integrated

The domain of the expression  $AB'CD+B$  is

B only

\_\_\_\_\_ is a single input gate

OR

To represent in digital value, the number of digit (0s and 1s) that represent a quantity is \_\_\_\_\_ to the range of values that are to be represented.

Equal

BCD code of 16 is \_\_\_\_\_.

00010001

To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_\_\_ variable Karnaugh Maps are used.

3

In Odd parity generator circuit which gate is used to detect parity errors?

XOR

A 3-variable Karnaugh map has

Eight cells

The measurable values generally change over a

Continuous range

\_\_\_\_\_ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.

GAL

When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?

1001

How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decorder?

Three

The simplified expression using either of the two K-maps are\_\_\_\_\_.

Identical

Which of the following expression in the product of sums form?

AB+CD

CMOS technology is characterized by low power dissipation with\_\_\_\_\_ switching speeds.

Slow

GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

True

High level Noise Margins (VNH) of CMOS 5 volt series circuits is\_\_\_\_\_

0.9 V

The output of the expression  $F=A+B+C$  will be Logic \_\_\_\_\_ when  $A=0$ ,  $B=1$ ,  $C=1$ . The symbol "+" here represents OR Gate

One

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be \_\_\_\_\_.

SET

3.3 v CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5 v CMOS series.

Fast switching speeds, very low power dissipation (page61)

The binary value "1010110" is equivalent to decimal \_\_\_\_\_

86

The \_\_\_\_\_ Encoder is used as a keypad encoder.

Decimal-to-BCD Priority

How many data select lines are required for selecting eight inputs?

3

The Quad Multiplexer has \_\_\_\_\_ outputs

4

Demultiplexer has

Single input and multiple outputs.

The expression \_\_\_\_\_ is an example of Commutative Law for Multiplication.

$AB=BA$

The look-ahead carry circuits\_\_\_\_\_

Reduce propagation delay

What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?

$B'+C'D'+CD$

2-input, 8-bit Multiplexer, by setting the S input to logic \_\_\_\_\_ the \_\_\_\_\_ inputs of both the multiplexers are selected.

High, B

The maximum decimal number that can be represented using the 64-bit unsigned representation \_\_\_\_\_

$(2^{64})-1$

When two or more products terms are assumed by Boolean addition, the result is a \_\_\_\_\_

SOP

Tri-State Buffer is a \_\_\_\_\_ gate with a control line that disconnects the

NOT

The 4-bits 2's complement representation of "7" is \_\_\_\_\_

1001

\_\_\_\_\_ and \_\_\_\_\_ are the steps of the Quine-McCluskey.

Find prime implicants and select minimal set of the prime implicants.

The binary number 1011,101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_\_ separated by a decimal point.

1011,101

Subtractors also have output to check if 1 has been \_\_\_\_\_

Borrowed

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

Slow

The \_\_\_\_\_ description is used to simulate the logic circuit and verify its operation.

Test vector

How many outputs can an integrated circuit comparator have?

Three

Which of the following is not the correct method of grouping?

Diagonally

The output of the expression  $F=A.B.C$  will be logic \_\_\_\_\_ when  $A=1, B=0, C=1$ .

Zero

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.

AND, OR

In the 32-bit Single Precision Floating point format, the exponent value \_\_\_\_\_ is reserved infinity exponent.

99

The Boolean expression  $(AB'CS')$  is used

A product term

The product of an XOR gate is zero(0), when \_\_\_\_\_ All the inputs are zero

I and IV only

\_\_\_\_\_ methods are used to Convert Decimal fractions to Binary.

2

To display the number \_\_\_\_\_ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

29

A SOP expression is equal to I \_\_\_\_\_

When one or more product terms in the expression are equal to 1

The output  $A \cdot B$  is set to 1 when the input combinations is

$A=01, B=10$

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

True

High level Noise Margins ( $V_{NH}$ ) of CMOS 5 volt series circuits is \_\_\_\_\_

0.9 V

If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them into floating point representation and then multiplying them, the value of mantissa of result will be

\_\_\_\_\_

24.582 (But not sure)

The output of the expression  $F = A + B + C$  will be Logic \_\_\_\_\_ represents OR Gate.

10(binary)

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be

SET

3.3  $\mu$ m CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5  $\mu$ m CMOS series.

Fast switch  $t_{sw}$  is characterized by \_\_\_\_\_ as compared to the 5  $\mu$ m CMOS series.

The binary value "1010110" is equivalent to decimal \_\_\_\_\_

86 (According to Formula)

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

Flip-Flop and DIV 32

DIV 16 and DIV 32

The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)

(n raise to power 2)

(n raise to power 2 and then minus 1)

(2 raise to power n)

(2 raise to power n and then minus 1)

A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state. On the next clock pulse, to what state does the counter go?

1001

1011

0011

1100

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is \_\_\_\_\_

0001

1111

1000

1110

Divide-by-160 counter is achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

DIV 16 and DIV 32

DIV 16 and DIV 10

A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.

3

7

8

15

RCO stands for \_\_\_\_\_

Reconfiguration Counter Output

Ripple Counter Output

Reconfiguration Clock Output

Ripple Clock Output

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

Clock Skew

Ripple Effect

None of given options

For a down counter that counts from (111 to 000), if current state is "101" the next state will be

\_\_\_\_\_

110

010

None of given options

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

Flip-Flop and DIV 32

Div 10 and DIV 16

Ripple Clock Output

The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins

2

4

6

8

\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously

Asynchronous

Synchronous

Positive-Edge triggered

Negative-Edge triggered

Q : A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.

3

7

8

15

Q : Design of state diagram is one of many steps used to design

A clock

A truncated counter

An UP/DOWN counter

Any counter

Q : A synchronous decade counter will have \_\_\_\_\_ flip-flops

3

4

7

10

Q : Karnaugh map is used in designing

A clock

A counter

An UP/DOWN counter

All of the above

Q : \_\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

Hold and Wait

Clock Skew

Race condition

Hold delay

Q : Three cascaded modulus-10 counters have an overall modulus of

30

100

1000

10000

Q : An Astablemultivibrator is known as a(n) \_\_\_\_\_

Oscillator

Booster

One-shot

Dual-shot

Q: \_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

Clock Skew

Ripple Effect

None of given options

Q: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_

Gated flip-flops

Pulse triggered flip-flops

Positive-Edge triggered flip-flops

Negative-Edge triggered flip-flops

Q: In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together

True

False

Quiz: A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must  $J$  and  $K$  be?

$J = 1, K = 0$

$J = 1, K = X$  (Don't care)

$J = X$  (Don't care),  $K = 0$

$J = 0, K = X$  (Don't care)

Q: The Synchronous counters are also known as Ripple Counters: :

True

False

Q:A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

False

Quiz: The terminal count of a 4-bit binary counter in the DOWN mode is\_\_\_\_\_

0000

0011

1100

1111

Quiz: An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting\_\_\_\_\_

Q output of all flip-flops to clock input of next flip-flops

Q' output of all flip-flops to clock input of next flip-flops

Q output of all flip-flops to J input of next flip-flops

Q' output of all flip-flops to K input of next flip-flops

The terminal count of a modulus-13 binary counter is

0000

1111

1101

1100

Quiz: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

False

Quiz: A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state. On the next clock pulse, to what state does the counter go?

1001

1011

0011

1100

Quiz: Design of state diagram is one of many steps used to design

A clock

A truncated counter

An UP/DOWN counter

Any counter

Quiz: An Astable multivibrator is known as a(n) \_\_\_\_\_

Oscillator

Booster

One-shot

Dual-shot

Quiz: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_

Gated flip-flops

Pulse triggered flip-flops

Positive-Edge triggered flip-flops

Negative-Edge triggered flip-flops

Quiz: A decade counter is \_\_\_\_\_

Mod-3 counter

Mod-5 counter

Mod-8 counter

Mod-10 counter

The terminal count of a 4-bit binary counter in the DOWN mode is \_\_\_\_\_

0000

0011

1100

1111

The Synchronous counters are also known as Ripple Counters:

True

False

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

Clock Skew

Ripple Effect

None of given options

Divide-by-160 counter is achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

DIV 16 and DIV 32

DIV 16 and DIV 10

Design of state diagram is one of many steps used to design

A clock

A truncated counter

An UP/DOWN counter

Any counter

In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is \_\_\_\_\_

0000

1111

0001

10000

# CS302

## ORANGE MONKEY

Which of the following is the octal equivalent of 28 decimal number?

34

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

$(2^{64})-1$

In a 4-variable K-map, a 2-variable product term is produced by

a 4-cell group of 1s

For a Standard SOP expression, a \_\_\_\_ is placed in the cell corresponding to the product term present in the expression.

1

The \_\_\_\_\_ input select/deselects both the decoders simultaneously.

Enable

NAND and \_\_\_\_\_ gates are known as Universal Gates.

**NOR**

The declaration section of ABEL generally includes the device declaration,  
\_\_\_\_\_ declarations and set declarations.

**Pin**

An SOP expression having a domain of 2 variables will have a truth table having  
\_\_\_\_\_ combinations of inputs and corresponding output values.

**4**

In the 32-bit Single Precision Floating formation, the exponent value \_\_\_\_\_ is reserved to represent 0 exponents.

**0**

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

**Slow**

The complement of a variable is always

**The inverse of the variable**

$A(B + C) = A.B + A.C$  is the expression of \_\_\_\_\_.

**Distributive Law**

If the number 2025 is represented in floating point, then exponent is \_\_\_\_\_.

3

Excess-8 code of -6 is \_\_\_\_\_.

0010

A 3-variable Karnaugh map has

Eight cells

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is \_\_\_\_\_ to the range of values that are to be represented.

Proportional

Suppose we want to transmit the data "10001101" and an "Even-Parity" bit scheme is used to detect errors, the parity bit added to the data will be \_\_\_\_\_.

Both "0" and "1" can be used

The carry propagation delay problem in parallel binary adder can be solved by \_\_\_\_\_.

Using two full adders

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a \_\_\_\_\_ multiplexer.

2-input, 8-bit

The octal equivalent of the following binary number is \_\_\_\_\_.

**117**

A' is written in ABEL as \_\_\_\_\_.

**!A**

Which of the following is the hexadecimal equivalent of 28?

**1C**

High Level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_.

**0.9 V**

Adjacent 1s detector circuit will have active high output for the input.

**0011**

Modern information techniques are relying more on \_\_\_\_\_ transmission.

**Digital**

The \_\_\_\_\_ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.

**Two**

How many data select lines are required for selecting eight inputs?

3

Select the mode of programming in which GAL 16V8 can be programmed.

All of the given option

\_\_\_\_\_ has the fastest switching speed and low power requirement.

Advanced low power Schottky

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_.

0.1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called \_\_\_\_ of the flip-flop.

Hold time

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

Each stage of Master-slave flip-flop works at \_\_\_\_ of the clock signal.

One half

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using \_\_\_\_

NOT

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is \_\_\_\_

**1111**

\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

**Race condition**

The Synchronous counters are also known as Ripple Counters:

**False**

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the \_\_\_

**Set-up time**

The n flip-flops store \_\_\_ states.

**$2^n$**

When the \_\_\_ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of \_\_\_

**1,2**

A positive edge-triggered flip-flop changes its state when \_\_\_

**Low-to-high transition of clock**

A decade counter is \_\_\_

**Mod-10 counter**

The look-ahead carry circuits \_\_\_\_\_  
**Reduce propagation delay**

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_ is added to the result

**0110**

Both the multiplexers are selected simultaneously when \_\_\_\_\_ is set to logic \_\_\_\_\_ in 2-inputs, 8-bit Multiplexer.

**G, Low**

Function labels required to represent the input/output combinations for each segment in 7-segment display

**7**

Multiplexers are also known as \_\_\_\_\_

**Data selectors**

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_

**0, 1**

Cin is part of \_\_\_\_\_ Adder.

**Full**

The look-ahead carry circuits \_\_\_\_\_

**Reduce propagation delay**

Which of the following gates has the outputs 1 if and only if at last one input is 1?

**OR**

A sop expression can be implemented by on \_\_\_ combination of gates.

**AND-OR**

The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through \_\_\_ ALU units in 16-bit ALU.

**Four**

Digital circuits operates with \_\_\_\_\_ voltage value(s)

**2**

In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles \_\_\_\_\_

**Lower priority outputs**

To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_\_\_ variable Karnaugh maps are used.

**4**

The output of a NAND Gate is \_\_\_\_\_ when all the inputs are one.

**Zero**

The \_\_\_\_\_ is the slowest and consumes more power.

**Standard TTL**

The between expression  $X-AB+CD$  represents

Two ANDs ORed together

The expression  $F-A+B+C$  describes the operation of three bits \_\_\_ Gate.

OR

Which one of the following is NOT a valid rule of Boolean Algebra?

$A=A'$

A 5-Variable Karnaugh map has

Thirty two cells

\_\_\_ is invalid number of cells in a single group formed by the adjacent cells K-map

12

In 32-bit Single –Precision floating point format representation the range of exponent value is from \_\_\_ to \_\_\_

+127 to -126

\_\_\_ has the fastest switching speed and low power requirements

Advanced low power schottky

Which of the following is a volatile memory?

**DRAM**

\_\_\_\_\_ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

**Combinational Input**

The AND Gate performs a logical \_\_\_\_\_ function.

**Division**

The Adjacent 1s Detector accepts 4-bit inputs. If \_\_\_\_\_ adjacent 1s are detected in the input, the output is set to high.

**1**

In the keyboard encoder, how many times per second does the ring counter scan the keyboard?

**650 scans/second**

The FAST Model Page Access allows \_\_\_\_\_ memory read and access times when reading successive data values stored in consecutive locations on the same row.

**Faster**

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a \_\_\_\_\_ with a \_\_\_\_\_.

**row, column**

Which of the following Output Equations determines the output of the State Machine?

**MAX = Q0Q1EN**

The maximum value, represented by a single hexadecimal digit is \_\_\_\_\_.

**"F"**

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a \_\_\_\_\_.

**1**

The Static Ram (SRAM) is non-volatile and is not a \_\_\_\_\_ density memory as a latch is required to store a single bit of information.

**High**

Demorgan's two theorems prove the equivalency of the NAND and \_\_\_\_\_ gates and the NOR and \_\_\_\_\_ gates respectively.

**Negative-OR, Negative-AND**

Two signals \_\_\_\_\_ and \_\_\_\_\_ provide the timing inputs to the State Machine.

**PTIME and QTIME**

The 74HC163 is a 4-bit Synchronous counter, it has \_\_\_\_\_ data **output pins.**

**4**

PLDs have In-System Programming (ISP) capability that allows the \_\_\_\_\_ to be programmed after they have been installed on a circuit board.

**PLDs**

The CONSTATE.CLK = Clock is used to indicate that the \_\_\_\_\_ state variables change on a clock transition.

**CONSTATE**

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using \_\_\_\_\_.

**Shift Registers**

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as \_\_\_\_\_ inputs.

**Synchronous**

For a down counter that counts from (111 to 000), if current state is "101" the next state will be \_\_\_\_\_.

**None of the given**

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

**XOR, NAND**

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to \_\_\_\_\_ location(s) using a single address.

**Four**

In NAND based S-R latch, output of each \_\_\_\_\_ gate is connected to the input of the other \_\_\_\_\_ gate.

**NAND, NAND**

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires \_\_\_\_\_ gates for the 8 product terms (minterms) with an 8-input OR gate.

**8 AND**

8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer.

**8-to-1**

The \_\_\_\_\_ input overrides the \_\_\_\_\_ input.

**Asynchronous, synchronous**

A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.

**AND-OR**

The 64-cell array organized as 8 x 8 cell array is considered as an 8 byte memory

The terminal count of a 4-bit binary counter in the UP mode is \_\_\_\_\_.

**1111**

A 3-variable karnaugh map has \_\_\_\_\_ cells

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_.

**Q output of all flip-flops to clock input of next flip-flops**

Memory is arranged in \_\_\_\_\_.

**Two-dimensional manner**

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result.

**1001**

Subtractors also have output to check if 1 has been \_\_\_\_\_.

**Primed**

The Test Vector definition defines the test vectors for all the three counter inputs and \_\_\_\_\_ counter output/outputs.

**Three**

A multiplexer with a register circuit converts  
**Parallel data to serial**

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

**True**

The n flip-flops store \_\_\_\_\_ states.

**$2^n$**

The S-R latch has two inputs, therefore \_\_\_\_\_ different combinations of inputs can be applied to control the operation of the S-R latch.

**four**

Why demultiplexer is called a data distributor?

**Single input to Single Output**

When the transmission line is idle in an asynchronous transmission

**It is set to logic high**

UVERPROM is stands for

**Ultra-Violet**

In memory write cycle, the time for which the WE signal remains active is known as the

**Write pulse width**

The outputs of SR latches in elevator state machine are feed back to the \_\_\_\_\_ gate array for connection to the D-flipflops.

**AND**

PALs tend to execute \_\_\_\_\_ logic.

**SOP**

The ROM used by a computer is relatively \_\_\_\_\_ as it stores few buyers of code used to Boot the Computer system on power up.

**Small**

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

**-WE**

You have to choose suitable option when your timer will reset by considering this given code:

`TRSTATE.CLK = clk;`

TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);  
NSY2 or EWY2

A NOR based S-R latch is implemented using \_\_\_\_\_ gates instead of \_\_\_\_\_ gates.  
NOR, NAND

Implementation of Latch is required almost \_\_\_\_\_ transistor.  
Six

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in \_\_\_\_\_ when Distributed refresh is used.  
7.8 microsec

The NOR logic gate is the same as the operation of the \_\_\_\_\_ gate with an inverter connected to the output.  
NAND

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.  
1

Select the mode of programming in which GAL16V8 can be programmed:  
All of the given

Divide-by-32 counter can be achieved by using  
Flip-Flop and DIV 32

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the \_\_\_\_\_ can be pressed at any time either on the first floor or the second floor in elevator.  
REQ1

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be \_\_\_\_\_.

One

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:  
1111

Adding two octal numbers "36" and "71" result in \_\_\_\_\_.  
127

The ABEL Input file can use a \_\_\_\_\_ instead of the equation to specify the Boolean expressions.

**Truth Table**

The domain of the expression  $AB'CD + AB' + C'D + B$  is

**A, B, C and D**

If the number of samples that are collected is reduced by half, the reconstructed signal will be \_\_\_\_\_ from/to the original.

**Same**

In DRAM read cycle R/W- signal is activated to read data which is made available on the \_\_\_\_\_ data line.

**D(OUT)**

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

**True**

Implementation of the FIFO buffer in \_\_\_\_\_ is usually takes the form of a circular buffer.

**RAM**

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack \_\_\_\_\_.

**Top**

Which one flip-flop has an invalid output state?

**SR**

The output of a NAND gate is \_\_\_\_\_ when all the inputs are one.

**Zero**

The Transition table is very similar to the \_\_\_\_\_ table.

**State**

Consider the sum of weight method for converting decimal into binary value, \_\_\_\_\_ is the highest weight for 411.

**256**

Canonical form is a unique way of representing \_\_\_\_\_.

**SOP**

\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously.

**Synchronous**

Cin is part of \_\_\_\_\_ Adder.

**Full**

Flash memories Operation are classified into \_\_\_\_\_ different operation.

**Two**

A Product term is 0 when \_\_\_\_\_

**Any one literal is 0**

In 8-inpit multiplexer, the two outputs are connected through a/an \_\_\_gate.

**OR**

\_\_\_\_\_ Device dissipate varying amount of power depending upon the frequency of operation.

**CMOS**

Boolean Addition operation is performed by a(an)\_\_\_ gate.

**OR**

A SOP expression can be implemented by an\_\_\_\_\_ combination of gates.

**AND-OR**

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

**$(2^{64})-1$**

In 16-bit ALU, The G output is activated if the 4-bi unit generate a Carry \_\_\_\_\_ irrespective of Carry\_\_\_\_\_.

**Out,In**

A standard POS form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.

**Sum**

In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles \_\_\_\_\_.

**Lower priority inputs**

Which of the following is the example of comparator?

**XNOR**

In CMOS 5 Volt series, Input voltage of Logic high signal ( $V_{IH}$ ) with a ranges from \_\_\_\_\_ to \_\_\_\_\_ volts.

**3,5,5**

The Adjacent 1 S Detector accepts 4-bits input. If \_\_\_\_\_ adjacent 1S are detected in the input, the output is set to high.

**4**

DE Morgan's two theorems prove the equivalency of the NAND and \_\_\_\_\_ gates and the NOR and \_\_\_\_\_ gates respectively.

**Negative-AND, Negative-OR**

Adding two octal numbers "36 and 71" result in \_\_\_\_\_.

**127**

Any of the \_\_\_\_\_ forms of the Karnaugh Map can be used to simplify Boolean expressions

**Four**

Quine-McCluskey and K-Map methods are used for \_\_\_\_\_ of Boolean expression.

**Simplification**

The number "1259" may belong to \_\_\_\_ number system.

**Decimal or Hexadecimal system**

The series of TTL chips are characterized by their \_\_\_\_.

**Switching Speed only**

All ABEL statements must end with \_\_\_\_.

**:**

In sequential circuit memory elements are connected with \_\_\_\_.

**Clock**

In the 32-bit Single Precision Floating Point format, the exponent value \_\_\_\_ is reserved to represent infinity exponents.

**255**

The \_\_\_\_ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

**PLA**

The limitation in implementation of parallel binary address is known as \_\_\_\_.

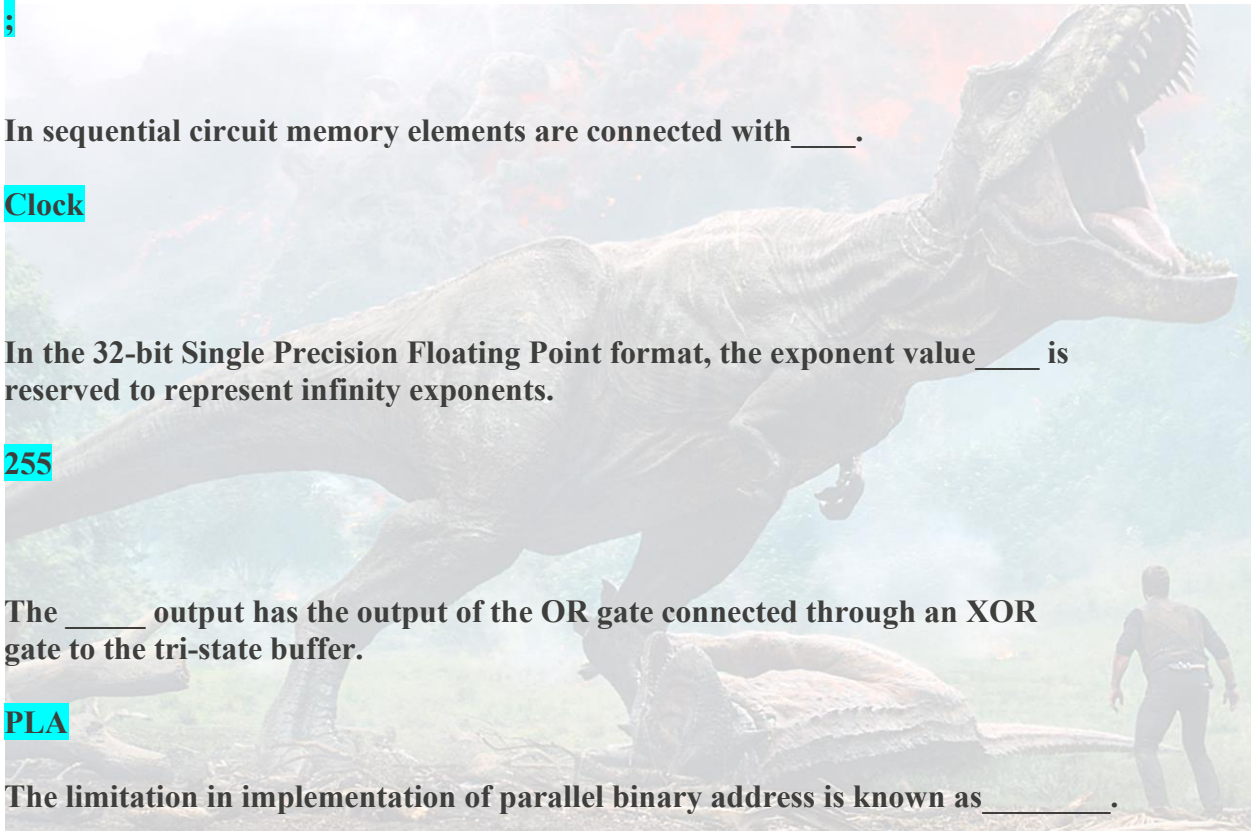
**Carry input**

The Gray code is different form the unsigned binary code because \_\_\_\_.

**Successive value of Gray code by only one bit**

Removing the NOT gate at the output of the NOR gate result in an \_\_\_\_.

**OR gate**



Portable devices that run on batteries use \_\_\_ circuit that have low power dissipation.

**Integrated**

The domain of the expression  $AB'CD+B$  is

**B only**

\_\_\_\_\_ is a single input gate

**OR**

To represent in digital value, the number of digit (0s and 1s) that represent a quantity is \_\_\_ to the range of values that are to be represented.

**Equal**

BCD code of 16 is \_\_\_\_\_.

**00010001**

To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_ variable Karnaugh Maps are used.

**3**

In Odd parity generator circuit which gate is used to detect parity errors?

**XOR**

A 3-variable Karnaugh map has

**Eight cells**

The measurable values generally change over a

**Continuous range**

\_\_\_\_\_ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.

**GAL**

When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?

**1001**

How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decoder?

**Three**

The simplified expression using either of the two K-maps are \_\_\_\_\_.

**Identical**

Which of the following expression in the product of sums form?

**AB+CD**

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

**Slow**

GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

**True**

High level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_

**0.9 V**

The output of the expression  $F=A+B+C$  will be Logic \_\_\_\_\_ when  $A=0, B=1, C=1$ . the symbol "+" here represents OR Gate

**One**

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be \_\_\_\_\_.

**SET**

3.3 v CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5 v CMOS series.

**Fast switching speeds, very low power dissipation (page61)**

The binary value "1010110" is equivalent to decimal \_\_\_\_\_

**86**

The \_\_\_\_\_ Encoder is used as a keypad encoder.

**Decimal-to-BCD Priority**

How many data select lines are required for selecting eight inputs?

**3**

The Quad Multiplexer has \_\_\_\_\_ outputs

**4**

Demultiplexer has

**Single input and multiple outputs.**

The expression \_\_\_\_\_ is an example of Commutative Law for Multiplication.

**AB=BA**

The look-ahead carry circuits \_\_\_\_\_

**Reduce propagation delay**

What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?

**$B'+C'D'+CD$**

2-input, 8-bit Multiplexer, by setting the S input to logic \_\_\_\_\_ the \_\_\_\_\_ inputs of both the multiplexers are selected.

**High, B**

The maximum decimal number that can be represented using the 64-bit unsigned representation \_\_\_\_\_

**$(2^{64})-1$**

When two or more products terms are assumed by Boolean addition, the result is a \_\_\_\_\_

**SOP**

Tri-State Buffer is a \_\_\_\_\_ gate with a control line that disconnects the

**NOT**

The 4-bits 2's complement representation of "7" is \_\_\_\_\_

**1001**

\_\_\_\_\_ and \_\_\_\_\_ are the steps of the Quine-McCluskey.

**Find prime implicants and select minimal set of the prime implicants.**

The binary number 1011,101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_ separated by a decimal point.

**1011,101**

Subtractors also have output to check if 1 has been \_\_\_\_\_

**Borrowed**

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

**Slow**

The \_\_\_\_\_ description is used to simulate the logic circuit and verify its operation.

**Test vector**

How many outputs can an integrated circuit comparator have?

**Three**

Which of the following is not the correct method of grouping?

**Diagonally**

The output of the expression  $F=A.B.C$  will be logic \_\_\_\_\_ when  $A=1, B=0, C=1$ .

**Zero**

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.

**AND, OR**

In the 32-bit Single Precision Floating point format, the exponent value \_\_\_\_\_ is reserved infinity exponent.

**99**

The Boolean expression  $(AB'CS')$  is used

**A product term**

The product of an XOR gate is zero(0), when \_\_\_\_\_ All the inputs are zero

**I and IV only**

\_\_\_\_\_ methods are used to Convert Decimal fractions to Binary.

**2**

To display the number \_\_\_\_\_ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

**29**

Divide-by-32 counter can be achieved by using  
Select correct option:

**Flip-Flop and DIV 10**

**Flip-Flop and DIV 16**

**Flip-Flop and DIV 32  
DIV 16 and DIV 32**

**Question # 2 of 10 ( Start time: 03:05:20 PM ) Total Marks: 1**

**The counter states or the range of numbers of a counter is determined by the formula. (“n” represents the total number of flip-flops)**

**Select correct option:**

**(n raise to power 2)**

**(n raise to power 2 and then minus 1)**

**(2 raise to power n)**

**(2 raise to power n and then minus 1)**

**Question # 3 of 10 ( Start time: 03:06:36 PM ) Total Marks: 1**

**A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?**

**Select correct option:**

**1001**

**1011**

**0011**

**1100**

**Question # 4 of 10 ( Start time: 03:07:37 PM ) Total Marks: 1**

**A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is \_\_\_\_\_**

**Select correct option:**

**0001**

**1111**

**1000**

**1110**

**Question # 5 of 10 ( Start time: 03:09:04 PM ) Total Marks: 1**

**Divide-by-160 counter is achieved by using**

**Select correct option:**

Flip-Flop and DIV 10  
Flip-Flop and DIV 16  
DIV 16 and DIV 32  
**DIV 16 and DIV 10**

Question # 6 of 10 ( Start time: 03:10:01 PM ) Total Marks: 1

A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.

Select correct option:

- 3
- 7
- 8**
- 15

Question # 7 of 10 ( Start time: 03:10:49 PM ) Total Marks: 1

RCO stands for \_\_\_\_\_

Select correct option:

- Reconfiguration Counter Output
- Ripple Counter Output
- Reconfiguration Clock Output
- Ripple Clock Output**

Question # 8 of 10 ( Start time: 03:11:38 PM ) Total Marks: 1

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Select correct option:

- Race condition**
- Clock Skew
- Ripple Effect
- None of given options

Question # 9 of 10 ( Start time: 03:12:20 PM ) Total Marks: 1

For a down counter that counts from (111 to 000), if current state is "101" the next state

will be \_\_\_\_\_  
Select correct option:

- 111
- 110
- 010
- none of given options**

Question # 10 of 10 ( Start time: 03:13:03 PM ) Total Marks: 1  
A Divide-by-20 counter can be achieved by using  
Select correct option:

- Flip-Flop and DIV 10**
- Flip-Flop and DIV 16
- Flip-Flop and DIV 32
- Div 10 and DIV 16

Q : Ripple Clock Output

The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins  
Select correct option:

- 2
- 4**
- 6
- 8

Q : \_\_\_\_\_ Counters as the name indicates are not triggered simultaneously.  
Select correct option:

**Asynchronous**

Q : A counter is implemented using three (3) flip-flops, possibly it will  
have \_\_\_\_\_ maximum output status.  
Select correct option:

- 3

7  
**8**  
15

**Q : Design of state diagram is one of many steps used to design**  
**Select correct option:**

a clock  
a truncated counter  
an UP/DOWN counter  
**any counter**

**Q : A synchronous decade counter will have \_\_\_\_\_ flip-flops.**  
**Select correct option:**

3  
**4**  
7  
10

**Q : Karnaugh map is used in designing.**  
**Select correct option:**

a clock  
a counter  
an UP/DOWN counter  
**All of the above**

**Q : \_\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable**  
**Select correct option:**

**Hold and Wait**  
**Clock Skew**

**Race condition**

Hold delay

Q : Three cascaded modulus-10 counters have an overall modulus of  
Select correct option:

30

100

1000

10000

Four cascaded modulus-10 counters have an overall modulus of \_\_\_\_\_.

- 1)  100
- 2)  10
- 3)  10000
- 4)  1000

Q : An Astable multivibrator is known as a(n) \_\_\_\_\_

Select correct option:

**Oscillator**

Booster

One-shot

Dual-shot

Q: \_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Select correct option:

Race condition

**Clock Skew**

Ripple Effect

None of given options

Q: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_

Select correct option:

Gated flip-flops

Pulse triggered flip-flops

Positive-Edge triggered flip-flops

Negative-Edge triggered flip-flops

Q: In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together

Select correct option:

True

False

vuhelp.pk

Quiz: A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must J and K be?

Select correct option:

J = 1, K = 0

J = 1, K = X (Don't care)

J = X (Don't care), K = 0

J = 0, K = X (Don't care)

Q: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

Select correct option:

True

False

Quiz: The terminal count of a 4-bit binary counter in the DOWN mode is \_\_\_\_\_

Select correct option:

0000

0011

1100

1111

Quiz: An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting\_\_\_\_\_

Select correct option:

Q output of all flip-flops to clock input of next flip-flops

**Q' output of all flip-flops to clock input of next flip-flops**

Q output of all flip-flops to J input of next flip-flops

Q' output of all flip-flops to K input of next flip-flops

the terminal count of a modulus-13 binary counter is

Select correct option:

0000

1111

**1101**

1100

Quiz: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

Select correct option:

**True**

False

Quiz: A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

Select correct option:

**1001**

1011

0011

1100

Quiz: Design of state diagram is one of many steps used to design

Select correct option:

- a clock
- a truncated counter
- an UP/DOWN counter
- any counter**

Quiz: An Astable multivibrator is known as a(n) \_\_\_\_\_  
Select correct option:

- Oscillator**
- Booster
- One-shot
- Dual-shot

Quiz: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_  
Select correct option:

- Gated flip-flops
- Pulse triggered flip-flops
- Positive-Edge triggered flip-flops
- Negative-Edge triggered flip-flops**

Quiz: A decade counter is \_\_\_\_\_  
Select correct option:

- Mod-3 counter
- Mod-5 counter
- Mod-8 counter
- Mod-10 counter**

Question # 1 of 10 ( Start time: 03:40:29 PM )      Total Marks: 1  
The terminal count of a 4-bit binary counter in the DOWN mode is \_\_\_\_\_  
Select correct option:

- 0000**
- 0011
- 1100
- 1111

Question # 3 of 10 ( Start time: 03:41:08 PM ) Total Marks: 1

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Select correct option:

Race condition

**Clock Skew**

Ripple Effect

None of given options

Question # 4 of 10 ( Start time: 03:41:27 PM ) Total Marks: 1

Divide-by-160 counter is achieved by using

Select correct option:

Flip-Flop and DIV 10

Flip-Flop and DIV 16

DIV 16 and DIV 32

**DIV 16 and DIV 10**

Question # 5 of 10 ( Start time: 03:41:44 PM ) Total Marks: 1

Design of state diagram is one of many steps used to design

Select correct option:

a clock

a truncated counter

an UP/DOWN counter

**any counter**

Question # 6 of 10 ( Start time: 03:42:01 PM ) Total Marks: 1

In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is \_\_\_\_\_

Select correct option:

0000

**1111**

0001

10000

The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins

Select correct option:

- 2
- 4**
- 6
- 8

Q : \_\_\_\_\_ Counters as the name indicates are not triggered simultaneously.  
Select correct option:

**Asynchronous**

Q : A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.  
Select correct option:

- 3
- 7
- 8**
- 15

Q : Design of state diagram is one of many steps used to design  
Select correct option:

- a clock
- a truncated counter
- an UP/DOWN counter
- any counter**

Q : A synchronous decade counter will have \_\_\_\_\_ flip-flops.  
Select correct option:

- 3
- 4**

7  
10

Q : Karnaugh map is used in designing.  
Select correct option:

- a clock
- a counter
- an UP/DOWN counter
- All of the above**

Q : \_\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable  
Select correct option:

- Hold and Wait
- Clock Skew
- Race condition**
- Hold delay

Q : Three cascaded modulus-10 counters have an overall modulus of  
Select correct option:

30  
100  
1000

**10000**

Four cascaded modulus-10 counters have an overall modulus of \_\_\_\_\_.

- 1)  100
- 2)  10
- 3)  10000
- 4)  1000

Q : An Astable multivibrator is known as a(n) \_\_\_\_\_  
Select correct option:

**Oscillator**

Booster

One-shot

Dual-shot

Q: \_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Select correct option:

Race condition

**Clock Skew**

Ripple Effect

None of given options

Q: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_

Select correct option:

Gated flip-flops

Pulse triggered flip-flops

Positive-Edge triggered flip-flops

**Negative-Edge triggered flip-flops**

Q: In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together

Select correct option:

**True**

False

vuhelp.pk

Quiz: A flip-flop is presently in SET state and must remain SET on the next clock pulse.

What must j and K be?

Select correct option:

J = 1, K = 0

**J = 1, K = X (Don't care)**

$J = X(\text{Don't care}), K = 0$   
 $J = 0, K = X(\text{Don't care})$

**Q: The Synchronous counters are also known as Ripple Counters:  
Select correct option:**

True  
**False**

**Q: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.  
Select correct option:**

**True**  
False

**Quiz: The terminal count of a 4-bit binary counter in the DOWN mode is \_\_\_\_\_  
Select correct option:**

**0000**  
0011  
1100  
1111

**Quiz: An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_  
Select correct option:**

Q output of all flip-flops to clock input of next flip-flops  
**Q' output of all flip-flops to clock input of next flip-flops**  
Q output of all flip-flops to J input of next flip-flops  
Q' output of all flip-flops to K input of next flip-flops

**the terminal count of a modulus-13 binary counter is  
Select correct option:**

0000  
1111  
**1101**  
1100

**Quiz: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.**

**Select correct option:**

**True**  
False

**Quiz: A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?**

**Select correct option:**

**1001**  
1011  
0011  
1100

**Quiz: Design of state diagram is one of many steps used to design**

**Select correct option:**

a clock  
a truncated counter  
an UP/DOWN counter  
**any counter**

**Quiz: An Astable multivibrator is known as a(n) \_\_\_\_\_**

**Select correct option:**

**Oscillator**  
Booster

One-shot  
Dual-shot

Quiz: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_  
Select correct option:

Gated flip-flops  
Pulse triggered flip-flops  
Positive-Edge triggered flip-flops  
Negative-Edge triggered flip-flops

Quiz: A decade counter is \_\_\_\_\_  
Select correct option:

Mod-8 counter  
Mod-10 counter

Question # 1 of 10 ( Start time: 03:40:29 PM ) Total Marks: 1  
The terminal count of a 4-bit binary counter in the DOWN mode is \_\_\_\_\_  
Select correct option:

0000  
0011  
1100  
1111

Question # 2 of 10 ( Start time: 03:40:50 PM ) Total Marks: 1  
The Synchronous counters are also known as Ripple Counters:  
Select correct option:

True  
False

Question # 3 of 10 ( Start time: 03:41:08 PM ) Total Marks: 1  
\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.  
Select correct option:

Race condition  
Clock Skew

**Ripple Effect**

**None of given options**

**Question # 4 of 10 ( Start time: 03:41:27 PM ) Total Marks: 1**

**Divide-by-160 counter is achieved by using**

**Select correct option:**

**Flip-Flop and DIV 10**

**Flip-Flop and DIV 16**

**DIV 16 and DIV 32**

**DIV 16 and DIV 10**

**Question # 5 of 10 ( Start time: 03:41:44 PM ) Total Marks: 1**

**Design of state diagram is one of many steps used to design**

**Select correct option:**

**a clock**

**a truncated counter**

**an UP/DOWN counter**

**any counter**

**Question # 6 of 10 ( Start time: 03:42:01 PM ) Total Marks: 1**

**In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is \_\_\_\_\_**

**Select correct option:**

**0000**

**1111**

**0001**

**10000**



**1. The terminal count of a 4-bit binary counter in the UP mode is .**

**a) 1100**

**b) 0011**

**c) 1111**

**d) 0000**

2. For a down counter that counts from (111 to 000). If current state is “101” the next state will be .

a) 111

**b) 110**

c) 010

d) None of given options

3. The n flip-flops store states.

a) 1

**b)  $2^n$**

c) 0

4. An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting

**a) Q output of all flip-flops to clock input of next flip-flops**

5. In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

**a) True**

b) False

6. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

a) True

**b) False**

7. The 74HC163 is a 4-bit Synchronous Counter, it has data output pins.

a) 2

**b) 4**

8. Counters as the name indicates are not triggered simultaneously

**a) Asynchronous**

b) Synchronous

c) Positive-Edge triggered

d) Negative-Edge triggered

9. Divide-by-32 counter can be achieved by using

a) Flip-Flop and DIV 10

**b) Flip-Flop and DIV 16**

c) Flip-Flop and DIV 32

d) DIV 16 and DIV 32

10. The input overrides the input

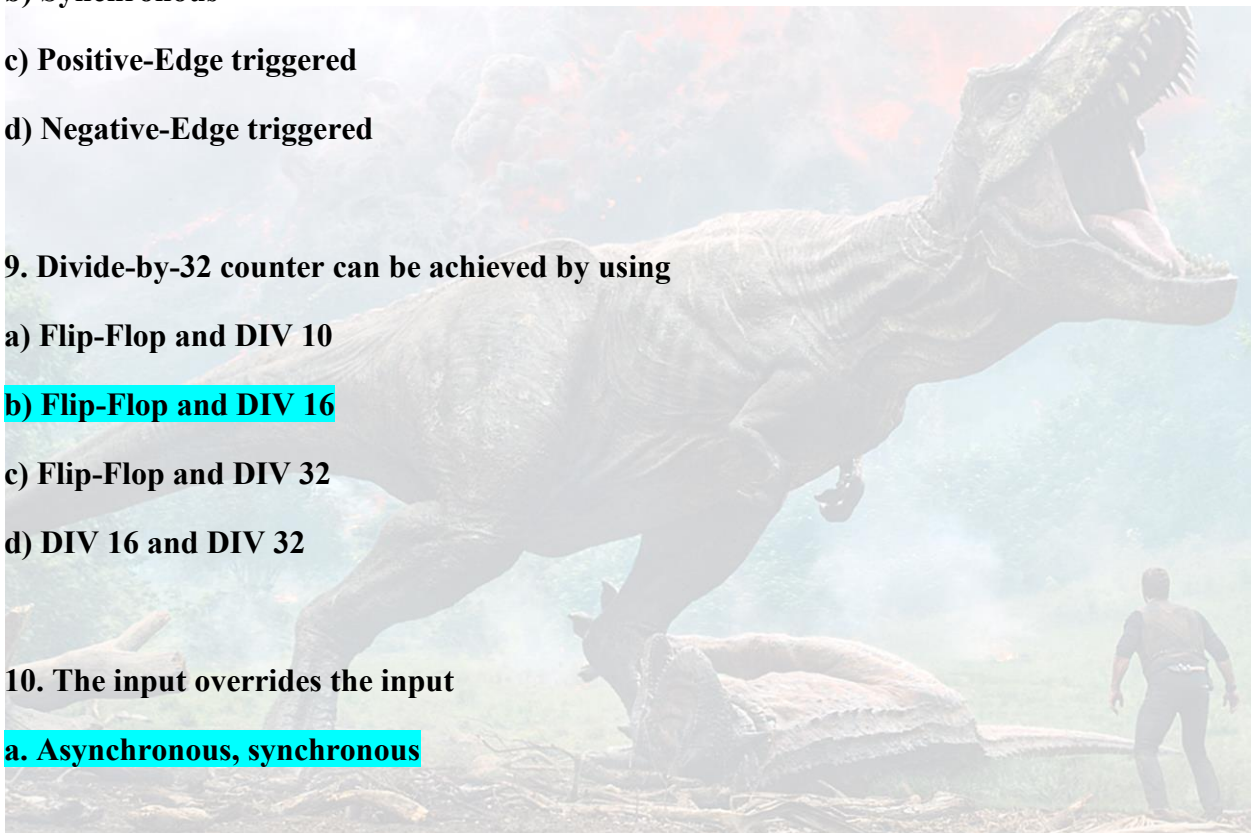
**a. Asynchronous, synchronous**

11. The synchronous counters are also known as Ripple Counters:

a) True

**b) False**

12. With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in



a) 80 micro seconds

b) 8 micro seconds

c) 80 mili seconds

d) 10 micro seconds

13. Number of states in an 8-bit Johnson counter sequence are:

a) 8

b) 12

c) 14

d) 16

14. A synchronous decade counter will have flip-flops

a) 3

b) 4

c) 7

15. is one of the examples of synchronous inputs.

a) J-K input

b) EN input

c) Preset input (PRE)

d) Clear input (CLR)

16. A decade counter is

d) Mod-10 counter



17. In gated SR latch, what is the value of the output if  $EN=1$ ,  $S=0$  and  $R=1$ ?

a)  $Q_t$

**b) 0**

c) 1

d) Invalid

18. A Divide-by-20 counter can be achieved by using

**a) Flip-Flop and DIV 10**

b) Flip-Flop and DIV 16

c) Flip-Flop and DIV 32

d) DIV 10 and DIV 16

19. A one-shot mono-stable device contains \_

a) AND gate, Resistor, Capacitor and NOT Gate

b) NAND gate, Resistor, Capacitor and NOT Gate

**c) NOR gate, Resistor, Capacitor and NOT Gate**

d) XNOR gate, Resistor, Capacitor and NOT Gate

20. The inputs can be directly mapped to Karnaugh maps.

a) S-R

**b) J-K**

c) Flip-Flop

d) External

21. A mono-stable device only has a single stable state

**a) True**

b) False

22. The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the

**a) Set-up time**

b) Hold time

c) Pulse interval time

d) Pulse stability time (PST)

23. The low to high or high to low transition of the clock is considered to be a(n)

a) State

**b) Edge**

c) Trigger

d) One-shot

24. A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state, on the next clock pulse, to what state does the counter go?

**a) 1001**

b) 1011

c) 0011

d) 1100

25. When the Hz sampling interval is selected, the signal at the output of the J-K flip-flop

has a time period of seconds.

a) 1, 2

b) 0, 2

c) 2, 5

d) 1, 1

26. Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to .

a) Set

b) Toggle

c) Latch

d) Reset

27. A stage in the shift register consists of

a) A latch

b) A flip flop

c) A byte of storage

d) Four bits of storage

28. When the both inputs of edge-triggered J-K flop-flop are set to logic zero

a) The flop-flop is triggered

b)  $Q=0$  and  $Q'=1$

d) The output of flip-flop remains unchanged

29. A positive edge-triggered flip-flop changes its state when

**c) Low-to-high transition of clock**

d) High-to-low transition of clock

30. If a circuit suffers “Clock Skew” problem, the output of circuit can’t be guaranteed.

**a) True**

b) False

31. The minimum time for which the input signal has to be maintained at the input of flip-flop is called of the flip-flop.

a) Set-up time

**b) Hold time**

c) Pulse interval time

d) Pulse stability time (PST)

34. A modulus-14 counter has fourteen states requiring

a) 14 flip flops

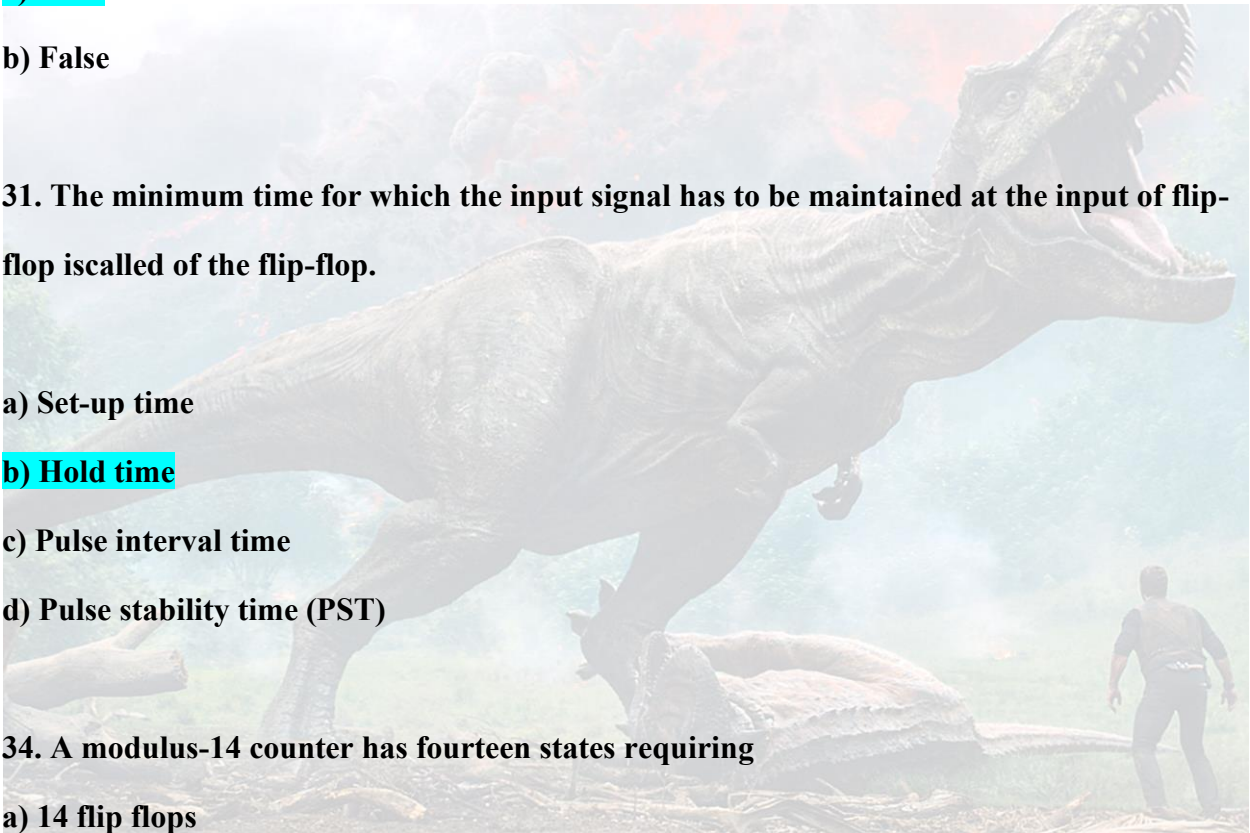
b) 14 registers

**c) 4 flip flops**

d) 4 registers

35. In Master-Slave flip-flop the clock signal is connected to slave flip-flop using gate.

a) AND



b) OR

c) NOT

d) NAND

36. flip-flops are obsolete now.

a) Edge-triggered

b) Master-Slave

c) T-flipflop

d) D-flipflop

37. The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flipflop

a) Doesn't have an invalid state

38. The glitches due to "Race Condition" can be avoided by using a .

a) Gated flip-flops

b) Pulse triggered flip-flops

c) Positive-Edge triggered flip-flops

d) Negative-Edge triggered flip-flops

39. For a gated D-Latch if  $EN=1$  and  $D=1$  then  $Q(t+1) =$

a) 0

b) 1

c)  $Q(t)$

d) Invalid

40. occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

a) Race condition

b) Clock skew

c) Ripple effect

d) None of given options



CS302-Digital Logic and Design

Solved MCQS for Midterms papers

Solved by JUNAID MALIK and Team



**AL-Junaid Institute**

Contact no: 03041659294



## LMS Handling

### **Subject Enrollment**

- 1) Online classes available  
HTML, CSS, Javascript  
Phyton..etc
- 2) Solved Graded Activities
  - Assignment's
  - Quizzes
  - GDB's
- 3) Solved Quiz File's
- 4) Short Note's
- 5) Past paper's &  
Current paper's

**Website Link**  
[vulmshelp.com](http://vulmshelp.com)

### **Final project CS619**

- 1) SRS  
(Software Requirement's  
Specification)
- 2) DD  
(Design Document)
- 3) Test phase + viva
- 4) Viva preparation
- 5) Final Deliverable

**Gmail**  
[junaidfazal08@gmail.com](mailto:junaidfazal08@gmail.com)

# AL-JUNAID INSTITUTE OF GROUP

1. Which of the following is a volatile memory?

1. PROM
2. DRAM
3. EPROM
4. EEPROM

2. \_\_\_\_\_ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

1. Combinational Input/output
2. Combinational Output
3. Combinational Input
4. Programmable polarity

3. The AND Gate performs a logical \_\_\_\_\_ function.

1. Addition
2. Subtraction
3. Multiplication
4. Division

4. The Adjacent 1s Detector accepts 4-bit inputs. If \_\_\_\_\_ adjacent 1s are detected in the input, the output is set to high.

1. 2
2. 4
3. 1
4. 0

5. In the keyboard encoder, how many times per second does the ring counter scan the key board?

1. 600 scans/second
2. 625 scans/second

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3. 650 scans/second

4. 700 scans/second

6. The FAST Model Page Access allows \_\_\_\_\_ memory read and access times when reading successive data values stored in consecutive locations on the same row.

1. Slow

2. Faster

3. Medium

4. Modern

7. GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a \_\_\_\_\_ with a \_\_\_\_\_.

1. column, row

2. row, column

3. column, column

4. row, row

8. Which of the following Output Equations determines the output of the State Machine?

1.  $MIN = Q0Q1$

2.  $MAX = Q0Q1EN$

3.  $MIN = Q0Q1EN$

4.  $MAX = Q1EN$

9. The maximum value, represented by a single hexadecimal digit is \_\_\_\_\_.

1. "E"

2. "F"

3. "G"

4. "H"

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**10. If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a \_\_\_\_\_.**

1. 0

2. 1

**11. The Static Ram (SRAM) is non-volatile and is not a \_\_\_\_\_ density memory as a latch is required to store a single bit of information.**

1. Low

2. High

3. Medium

4. Hot

**12. DE Morgan's two theorems prove the equivalency of the NAND and \_\_\_\_\_ gates and the NOR and \_\_\_\_\_ gates respectively.**

1. Negative-OR, Negative-AND

2. Negative-AND, Positive-OR

3. Positive-OR, Negative-AND

4. Positive-OR, Positive-AND

**13. Two signals \_\_\_\_\_ and \_\_\_\_\_ provide the timing inputs to the State Machine.**

1. NSSR and EWSR

2. LTIME and STIME

3. PTIME and QTIME

4. NSGrn and NSYel

**14. The 74HC163 is a 4-bit Synchronous counter, it has \_\_\_\_\_ data output pins.**

1. 2

2. 4

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3. 6

4. 8

**15. PLDs have In-System Programming (ISP) capability that allows the \_\_\_\_\_ to be programmed after they have been installed on a circuit board.**

1. PLAs

2. PALs

3. PLDs AL-JUNAID INSTITUTE OF GROUP

4. EPROM

**16. The CONSTATE.CLK = Clock is used to indicate that the \_\_\_\_\_ state variables change on a clock transition.**

1. CONSTATE

2. FLOOR

3. MOTION

4. OPEN

**17. Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using \_\_\_\_\_.**

1. Shift Registers

2. Circular Buffers

3. Ring Buffers

4. Reduce Registers

**18. The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as \_\_\_\_\_ inputs.**

1. Sequential

2. Asynchronous

3. Synchronous AL-JUNAID INSTITUTE OF GROUP

4. Combinational

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**19. For a down counter that counts from (111 to 000), if current state is "101" the next state will be \_\_\_\_\_.**

1. 111
2. 110
3. 010
4. None of the given

**20. The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.**

1. AND, NOR
2. AND, NOT
3. AND, OR
4. XOR, NAND

**21. The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to \_\_\_\_\_ location(s) using a single address.**

1. One
2. Two
3. Three
4. Four

**22. In NAND based S-R latch, output of each \_\_\_\_\_ gate is connected to the input of the other \_\_\_\_\_ gate.**

1. NOR, NAND
2. NAND, NOR
3. NOR, NOR
4. NAND, NAND

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**23. Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires \_\_\_\_\_ gates for the 8 product terms (minterms) with an 8-input OR gate.**

1. 8 OR
2. 8 AND
3. 8 XOR
4. 8 NOR

**24. 8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer.**

1. 4-to-2
2. 8-to-1
3. 4-to-4
4. 8-to-4

**25. The \_\_\_\_\_ input overrides the \_\_\_\_\_ input.**

1. Asynchronous, synchronous
2. Synchronous, asynchronous
3. Preset input (PRE), Clear input (CLR)
4. Clear input (CLR), Preset input (PRE)

**26. A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.**

1. OR-XOR
2. AND-NAND
3. AND-OR
4. XOR-NOR

**27. The 64-cell array organized as 8 x 8 cell array is considered**

1. as an 64 byte memory
2. as a 16 byte memory

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3. as an 8 byte memory  
4. as an 4 byte memory
- 28. The terminal count of a 4-bit binary counter in the UP mode is \_\_\_\_\_.**
1. 1100  
2. 0011  
3. 1111  
4. 0000
- 29. A 3-variable karnaugh map has \_\_\_\_\_.**
1. eight cells  
2. three cells  
3. sixteen cells  
4. four cells
- 30. An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_.**
1. Q output of all flip-flops to clock input of next flip-flops  
2. Q' output of all flip-flops to clock input of next flip-flops  
3. Q output of all flip-flops to J input of next flip-flops  
4. Q' output of all flip-flops to K input of next flip-flops
- 31. Memory is arranged in \_\_\_\_\_.**
1. linear fashion  
2. two-dimensional manner  
3. three-dimensional manner  
4. random fashion
- 32. If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result.**
1. 1001  
2. 0110

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3. 1111

4. 1100

**33. Subtractors also have output to check if 1 has been**

\_\_\_\_\_.

1. Primed

2. Shifted

3. Complemented

4. Borrowed

**34. The Test Vector definition defines the test vectors for all the three counter inputs and \_\_\_\_\_ counter output/outputs.**

1. One

2. Two

3. Three

4. Four

**35. A multiplexer with a register circuit converts**

1. Serial data to parallel

2. Parallel data to serial

3. Serial data to serial

4. Parallel data to parallel

**36. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.**

1. True

2. False

**37. The n flip-flops store \_\_\_\_\_ states.**

1. 1

2.  $2^n$

3. 0

4.  $2^{(n+1)}$

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**38. The S-R latch has two inputs, therefore \_\_\_\_\_ different combinations of inputs can be applied to control the operation of the S-R latch.**

1. two
2. four
3. eight
4. sixteen

**39. Why demultiplexer is called a data distributor?**

1. The input will be distributed to one of the outputs
2. The input will be selected for the output
3. The output will be distributed to one of the inputs
4. Single input to Single Output

**40. When the transmission line is idle in an asynchronous transmission**

1. It is set to logic low
2. It is set to logic high
3. It remains in previous state
4. State of transmission line is not used to start transmission

**41. UVERPROM is stands for**

1. Ultra-Variant
2. Ultra-Vibrant
3. Ultra-Voilet
4. Ultra-Visible

**42. In memory write cycle, the time for which the WE signal remains active is known as the \_\_\_\_\_.**

1. Write address setup
  2. Write pulse width
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3. Write delay width
4. Write data time
43. The outputs of SR latches in elevator state machine are feed back to the \_\_\_\_\_ gate array for connection to the D-flipflops.
  1. NOT
  2. AND
  3. OR
  4. XOR
44. PALs tend to execute \_\_\_\_\_ logic.
  1. SPD
  2. SOP
  3. SAC
  4. SAP
45. The ROM used by a computer is relatively \_\_\_\_\_ as it stores few byres of code used to Boot the Computer system on power up.
  1. Small
  2. Large
  3. Heavy
  4. High
46. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?
  1. CS
  2. WE
  3. W
  4. OE
47. You have to choose suitable option when your timer will reset by considering this given code:

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TRSTATE.CLK = clk;

TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);

1. NSY2 or EWY2
2. NSSR or TMRST
3. EWSR or NSRED
4. EWRed or EWYel

48. A NOR based S-R latch is implemented using \_\_\_\_\_ gates instead of \_\_\_\_\_ gates.

1. XOR, NAND
2. NOR, XOR
3. NOR, NAND
4. OR, XOR

49. Implementation of Latch is required almost \_\_\_\_\_ transistor.

1. Two
2. Four
3. Six
4. Eight

50. In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in \_\_\_\_\_ when Distributed refresh is used.

1. 4.8 microsec
2. 5.9 microsec
3. 7.8 microsec
4. 5.5 microsec

51. The NOR logic gate is the same as the operation of the \_\_\_\_\_ gate with an inverter connected to the output.

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1. AND
2. NAND
3. OR
4. NOT

52. For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1. 0
2. 1
3. x (don't care condition)
4. Any of given option depending on SOP term

53. Select the mode of programming in which GAL16V8 can be programmed:

1. Simple Mode
2. Complex Mode
3. Registered Mode
4. All of the given

54. Divide-by-32 counter can be achieved by using

1. Flip-Flop and DIV 10
2. Flip-Flop and DIV 16
3. Flip-Flop and DIV 32
4. DIV 16 and DIV 32

55. The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the \_\_\_\_\_ can be pressed at any time either on the first floor or the second floor in elevator.

1. REQ0
2. OPEN
3. REQ1
4. FLOOR1

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56. Consider  $A=1$ ,  $B=0$ ,  $C=1$ . A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be \_\_\_\_\_.

1. Zero
2. One
3. Undefined
4. No output as input is invalid

57. A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1. 0001
2. 1000
3. 1110
4. 1111

58. Adding two octal numbers "36" and "71" result in \_\_\_\_\_.

1. 213
2. 123
3. 127
4. 345

59. The ABEL Input file can use a \_\_\_\_\_ instead of the equation to specify the Boolean expressions.

1. Truth Table
2. State Diagram
3. Karnaugh Map
4. Logic Circuit

60. The domain of the expression  $AB'CD + AB' + C'D + B$  is

1. A and D
2. B only

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3. A, B, C and D

4. None of the given

**61. If the number of samples that are collected is reduced by half, the reconstructed signal will be \_\_\_\_\_ from/to the original.**

1. Different

2. Same

3. Equal

4. Opposite

**62. In DRAM read cycle R /W- signal is activated to read data which is made available on the \_\_\_\_\_ data line.**

1. D(IN)

2. D(OUT)

3. D(AB)

4. D(INT)

**63. In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.**

1. True

2. False

**64. Implementation of the FIFO buffer in \_\_\_\_\_ is usually takes the form of a circular buffer.**

1. RAM AL-JUNAID INSTITUTE OF GROUP

2. ROM

3. PPRM

4. Flash Memory

**65. As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack \_\_\_\_\_.**

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1. Bottom
2. Top
3. Down
4. Vertex

**66. Which one flip-flop has an invalid output state?**

1. T
2. JK
3. SR
4. D

**67. The output of a NAND gate is \_\_\_\_\_ when all the inputs are one.**

1. Zero
2. One
3. Available
4. Not available

**68. The Transition table is very similar to the \_\_\_\_\_ table.**

1. Truth
2. State
3. Transition
4. None of the given

**69. Consider the sum of weight method for converting decimal into binary value, \_\_\_\_\_ is the highest weight for 411.**

1. 64
2. 128
3. 256
4. 512

**70. Canonical form is a unique way of representing \_\_\_\_\_.**

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1. SOP

2. Minterm

3. Boolean Expression

4. POS

71. \_\_\_\_\_ Counters as the name indicates are not triggered simultaneously.

1. Asynchronous

2. Synchronous

3. Positive-Edge triggered

4. Negative-Edge triggered

72.  $C_{in}$  is part of \_\_\_\_\_ Adder.

1. Half

2. Full

3. Single

4. Double

73. Flash memory Operation are classified into \_\_\_\_\_ different operation.

1. Two

2. Three

3. Four

4. Five

1. A Product term is 0 when \_\_\_\_\_

a. Any one literal is 0

b. Any of the literals is 1

c. At least two literals are 1

d. All the literals are 1

2. In 8-input multiplexer, the two outputs are connected through a/an \_\_\_\_\_ gate.

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a. AND

**5. OR** AL-JUNAID INSTITUTE OF GROUP

b. NOT

c. NOR

3. \_\_\_\_ Device dissipate varying amount of power depending upon the frequency of operation.

a. TTL

**b. CMOS**

c. Storage

d. Peripheral

4. Boolean Addition operation is performed by a(an) \_\_\_\_ gate.

a. AND

**b. OR**

c. XOR

d. NAND

5. A SOP expression can be implemented by an \_\_\_\_ combination of gates.

a. OR-XOR

b. AND-AND

**c. AND-OR**

d. XOR-NOR

6. The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

a.  $2^{63}$

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- b.  $(2^{64})-1$**
- c.  $(2^{64}+$
- d.  $2^{64}$
7. In 16-bit ALU, The G output is activated if the 4-bit unit generate a Carry \_\_\_\_\_ irrespective of Carry\_\_\_\_\_.
- a. In,In
- b. In,Out
- c. Out,In**
- d. Out,Out
8. A standard POS form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.
- a. Sum**
- b. Product
- c. Min
- d. Composite
9. In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles\_\_\_\_\_.
- a. Lower priority outputs
- b. Higher priority outputs
- c. Lower priority inputs**
- d. Higher priority inputs
10. Which of the following is the example of comparator?
- a. OR
- b. AND
- c. XOR

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**d. XNOR**

11. IN CMOS 5 Volt series, Input voltage of Logic high signal ( $V_{IH}$ ) with a ranges from \_\_\_\_ to \_\_\_\_ volts.

- a. 4,5,5
- b. 0 ,5
- c. 0,3,5

**d. 3,5,5**

12. The Adjacent 1 S Detector accepts 4-bits input. If \_\_\_\_ adjacent 1S are detected in the input, the output is set to high.

- a. 2

**b. 4**

- c. 1
- d. 0

13. DE Morgan's two theorems prove the equivalency of the NAND and \_\_\_\_ gates and the NOR and \_\_\_\_ gates respectively.

- a. Negative-OR, Negative-AND

**b. Negative-AND, Negative-OR**

- c. positive-OR, Negative-AND
- d. positive-AND, Negative-OR

14. Adding two octal numbers "36 and 71" result in \_\_\_\_.

- a. 213
- b. 123

**c. 127**

- d. 345

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15. Any of the \_\_\_\_\_ forms of the Karnaugh Map can be used to simplify Boolean expressions

- a. Three
- b. Four**
- c. Two
- d. Five

16. Quine-McCluskey and K-Map methods are used for \_\_\_\_\_ of Boolean expression.

- a. Multiplication
- b. Addition

**6. Simplification** AL-JUNAID INSTITUTE OF GROUP

- c. Subtraction

17. The number "1259" may belong to \_\_\_\_\_ number system.

- a. Binary number system
- b. Octal or Decimal system
- c. Decimal or Hexadecimal system**
- d. Binary or Hexadecimal system

18. The series of TTL chips are characterized by their \_\_\_\_\_.

- a. Switching Speed only**
- b. Power Dissipation only
- c. Both
- d. None of these

19. All ABEL statements must end with \_\_\_\_\_.

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a. :

b. ,

**c. ;**

d. “

20. In sequential circuit memory elements are connected with\_\_\_\_\_.

a. Logical circuit

**b. Clock**

c. Feedback path

d. External Event

21. In the 32-bit Single Precision Floating Point format, the exponent value\_\_\_\_\_ is reserved to represent infinity exponents.

a. 98

b. 99

**c. 255**

d. 256

22. The \_\_\_\_\_ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

a. Combinational

b. Combinational input/

**c. PLA**

d. None

23. The limitation in implementation of parallel binary address is known as\_\_\_\_\_.

a. Delay

b. Carry propagation

**c. Carry input**

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d. Carry output

24. The Gray code is different from the unsigned binary code

because\_\_\_\_\_.

**a. Successive value of Gray code by only one bit**

b. Gray code is positional code

c. Gray code not support negative values

d. Gray code ranges from "0" to "9"

25. Removing the NOT gate at the output of the NOR gate result in an\_\_\_\_\_.

**7. OR gate**

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a. NAND gate

b. AND gate

c. NOT gate

26. Portable devices that run on batteries use\_\_\_\_\_ circuit that have low power dissipation.

a. Series

**b. Integrated**

c. Parallel

d. Electric

27. The domain of the expression  $AB'CD+B$  is

a. A and D

b. A,B,C and D

c. C and D only

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**d. B only**

28. \_\_\_\_\_ is a single input gate

a. AND

**b. OR**

c. NOT

d. XOR

29. To represent in digital value, the number of digit (0s and 1s) that represent a quantity is \_\_\_\_\_ to the range of values that are to be represented.

**a. Equal**

b. Greater

c. Lesser

d. Not equal

30. BCD code of 16 is \_\_\_\_\_.

a. 10001

**b. 00010001**

c. 00010111

d. 01110001

31. To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_\_\_ variable Karnaugh Maps are used.

**8. 3**

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a. 4

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b. 5

c. 2

32. In Odd parity generator circuit which gate is used to detect parity errors?

a. OR

b. NOR

**c. XOR**

d. AND

33. A 3-variable Karnaugh map has

**a. Eight cells**

b. Three cells

c. Sixteen cells

d. Four cells

34. The measurable values generally change over a

a. Specified period

b. Discrete range

c. Time

**d. Continuous range**

35. \_\_\_\_\_ uses E2CMOS technology which is Electrically Erasable CMOS

instead of Bipolar technology and fusible links.

a. PAL

**b. GAL**

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- c. PLA
  - d. PROM
36. When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?
- a. 1000
  - b. 1001**
  - c. 1010
  - d. 1100
37. How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decoder?
- a. One
  - b. Two
  - c. Three**
  - d. Four
38. The simplified expression using either of the two K-maps are\_\_\_\_\_.
- a. Similar
  - b. Different
  - c. Identical**
  - d. None-identical
39. Which of the following expression in the product of sums form?
- a.  $(A + B)(C+D)$
  - b.  $(AB)(CD)$

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c.  $AB(CD)$

d.  $AB+CD$

40. CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

a. **Slow**

b. Fast

c. Average

d. Medium

41. GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

a. **True**

b. False

42. High level Noise Margins ( $V_{NH}$ ) of CMOS 5 volt series circuits is

\_\_\_\_\_

a. 0.2 V

b. 0.5 V

c. **0.9 V**

d. 3.3 V

43. The output of the expression  $F=A+B+C$  will be Logic \_\_\_\_\_

when  $A=0$ ,  $B=1$ ,  $C=1$ . the symbol "+" here represents OR Gate

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a. Undefined

**b. One**

c. Zero

d. 10(binary)

44. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be \_\_\_\_\_.

**a. SET**

b. RESET

c. Clear

d. Invalid

45. 3.3 v CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5 v CMOS series.

a. Low switching speeds, high power dissipation

b. Fast switching speeds, high power dissipation

**c. Fast switching speeds, very low power dissipation (page61)**

d. Low switching speeds, very low power dissipation

46. The binary value "1010110" is equivalent to decimal \_\_\_\_\_

**a. 86**

b. 87

c. 88

d. 89

47. The \_\_\_\_\_ Encoder is used as a keypad encoder.

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- a. 2-to-8 encoder
- b. 4-to-16 encoder
- c. BCD-to-Decimal

**d. Decimal-to-BCD Priority**

48. How many data select lines are required for selecting eight inputs?

- a. 1
- b. 2
- c. 3**
- d. 4

49. The Quad Multiplexer has \_\_\_\_\_ outputs

- a. 4**
- b. 8
- c. 12
- d. 16

50. Demultiplexer has

- a. Single input and single outputs.
- b. Multiple inputs and multiple outputs.

**c. Single input and multiple outputs.**

- d. Multiple inputs and single output.

51. The expression \_\_\_\_\_ is an example of Commutative Law for Multiplication.

- a.  $AB+C = A+BC$
- b.  $A(B+C) = B(A+C)$

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c.  $AB=BA$

d.  $A+B=B+A$

52. The look-ahead carry circuits\_\_\_\_\_

a. Add a 1 to complemented inputs

b. Reduce propagation delay

c. Increase ripple delay

d. Determine sign and magnitude

53. What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?

a.  $B+C'D'+CD$

b.  $B'+C'D'+CD$

c.  $B+C'D'+C'D$

d.  $B'+C'D'+CD'$

54. 2-input, 8-bit Multiplexer, by setting the S input to logic\_\_\_\_\_

the\_\_\_\_\_ inputs of both the multiplexers are selected.

a. Low

b. High, B

c. Low, C

d. Low, C

55. The maximum decimal number that can be represented using the

64-bit unsigned representation\_\_\_\_\_

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- a.  $2^{63}$
- b.  $(2^{64})-1$
- c.  $(2^{64})+1$
- d.  $2^{64}$
56. When two or more products terms are assumed by Boolean addition, the result is a \_\_\_\_
- a. POS
- b. SOP
- c. Boolean
- d. Simplified
57. Tri-State Buffer is a \_\_\_\_ gate with a control line that disconnects the
- a. OR
- b. AND
- c. NAND
- d. NOT
58. The 4-bits 2's complement representation of "7" is \_\_\_\_\_
- a. 0111
- b. 1111
- c. 1001
- d. 0110
59. \_\_\_\_\_ and \_\_\_\_\_ are the steps of the Quine-McCluskey.

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- a. Draw a table and make groups
  - b. Write binary codes and write SOP
  - c. Find prime implicants and select minimal set of the prime implicants.
  - d. None of the given
60. The binary number 1011,101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_ separated by a decimal point.
- a. 1011,101
  - b. 101,1011
  - c. 101,1101
  - d. 10111,11
61. Subtractors also have output to check if 1 has been \_\_\_\_\_
- a. Primed
  - b. Shifted
  - c. Complemented
  - d. Borrowed
62. CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.
- a. Slow
  - b. Fast
  - c. Average
  - d. Medium
63. The \_\_\_\_\_ description is used to simulate the logic circuit and verify its operation.

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- a. Test file
- b. Declaration
- c. Logic
- d. Test vector

64. How many outputs can an integrated circuit comparator have?

- a. One
- b. Two
- c. Three
- d. Four

65. Which of the following is not the correct method of grouping?

- a. Along adjacent columns
- b. On comers
- c. Diagonally
- d. Along adjacent rows

66. The output of the expression  $F=A.B.C$  will be logic \_\_\_\_\_  
when  $A=1, B=0, C=1$ .

- a. Undefined
- b. One
- c. Zero
- d. No output as input is valid

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67. The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B

input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.

- a. AND,NOR
- b. AND,NOT
- c. AND,OR
- d. XOR,NAND

68. In the 32-bit Single Precision Floating point format, the exponent value \_\_\_\_\_ is reserved infinity exponent.

- a. 98
- b. 99
- c. 255
- d. 256

69. The Boolean expression  $(AB'CS')$  is used

- a. A sum term
- b. A product term
- c. A literal term
- d. A max term

70. The product of an XOR gate is zero(0), when \_\_\_\_\_

- I. All the inputs are zero
- II. Any of the inputs is zero

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III. An of the inputs is one IV.

All the inputs are one

- a. I only
- b. IV only
- c. I and IV only
- d. II and III

71. \_\_\_\_\_ methods are used to Convert Decimal fractions to Binary.

- a. 1
- b. 2
- c. 3
- d. 4

72. To display the number \_\_\_\_\_ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

- a. 19
- b. 29
- c. 39
- d. 49

73. The look-ahead carry circuits \_\_\_\_\_

- a. Add a 1 to complemented inputs
- b. Reduce propagation delay
- c. Increase ripple delay

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d. Determine sign and magnitude.

74. If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_ is added to the result

a. 1001

b. 0110

c. 1111

d. 1100

75. Both the multiplexers are selected simultaneously when \_\_\_\_\_ is set to logic \_\_\_\_\_ in 2-inputs, 8-bit Multiplexer.

a. G, Low

b. G, High

c. S, Slow

d. S, High

76. Function labels required to represent the input/output combinations for each segment in 7-segment display

a. 5

b. 7

c. 8

d. 10

77. Multiplexers are also known as \_\_\_\_\_

a. Data distributors

b. Data selectors

c. Data manipulators

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d. Data setters

78. The PLA can be programmed to give an output of constant

\_\_\_\_\_ or \_\_\_\_\_

a. 0,1

b. 1,2

c. 2,3

d. 0,0

79. Cin is part of \_\_\_\_\_ Adder.

a. Half

b. Full

c. Single

d. Double

80. The look-ahead carry circuits \_\_\_\_\_

a. Add 1 to complemented inputs

b. Reduce propagation delay

c. Increase ripple delay

d. Determine sign and magnitude

81. Which of the following gates has the outputs 1 if and only if at least one input is 1?

a. AND

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- b. NOR
- c. NAND
- d. OR

82. A sop expression can be implemented by on \_\_\_\_ combination of gates.

- a. OR-XOR
- b. AND-NAND
- c. AND-OR
- d. XOR-NOR

83. The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through \_\_\_\_ ALU units in 16-bit ALU.

- a. Two
- b. Four
- d. 9

91. Digital circuits operates with \_\_\_\_\_ voltage value(s)

- a. 1
- b. 2
- c. 3
- d. 4

92. Which of the following is the octal equivalent of 28 decimal numbers?

- a. 31
- b. 32

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c. 33

d. 34

93. In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles \_\_\_\_\_

a. Lower priority outputs

b. Higher priority outputs

c. Lower priority inputs

d. Higher priority inputs

94. To determine the seven expressions for each of the seven outputs in

7-segment display, seven \_\_\_\_\_ variable Karnaugh maps are used.

a. 3

b. 4

c. 5

d. 2

95. The output of a NAND Gate is \_\_\_\_\_ when all the inputs are one.

a. Zero

b. One

c. Available

d. Not available

96. The \_\_\_\_\_ is the slowest and consumes more power.

a. Standard TTL

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- b. Schottky TTL
  - c. Advanced Schokottky TTL
  - d. Low-Power Schottky TTL
97. The between expression  $X-AB+CD$  represents
- a. Two Ors ANDed together
  - b. A 4-input AND gate
  - c. Two ANDs ORed together
  - d. An eclusive-OR
98. The expression  $F-A+B+C$  describes the operation of three bits \_\_\_ Gate.
- a. OR
  - b. AND
  - c. NOT
  - d. NAND
99. Which one of the following is NOT a valid rule of Boolean Algebra?
- a.  $A+1=1$
  - b.  $A=A'$
  - c.  $AA=A$
  - d.  $A+0=A$
100. A 5-Variable Karnaugh map has
- a. Sixteen cells
  - b. Thirty two cells
  - c. Sixty four cells
  - d. None of these

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101. \_\_\_\_ is invalid number of cells in a single group formed by the adjacent cells K-map
- a. 2
  - b. 8
  - c. 12**
  - d. 16
102. In 32-bit Single –Precision floating point format representation the range of exponent value is from \_\_\_\_ to \_\_\_\_
- a. +127 to -126**
  - b. +127 to -254
  - c. +128 to -254
  - d. +256 to -255
103. \_\_\_\_ has the fastest switching speed and low power requirements
- a. Advanced low power schottky**
  - b. Fast TTL
  - c. Standard TTL
  - d. Schottky TTL

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Paper # 1

**MIDTERM EXAMINATION**  
**Spring 2010**  
**CS302- Digital Logic Design**

**Time: 60 min**  
**Marks: 38**

**Question No: 1 ( Marks: 1 ) - Please choose one**

---

A SOP expression is equal to 1 \_\_\_\_\_

- ▶ All the variables in domain of expression are present
- ▶ At least one variable in domain of expression is present.

▶ When one or more product terms in the expression are equal to 0.

▶ When one or more product terms in the expression are equal to 1. Page86

**Question No: 2 ( Marks: 1 ) - Please choose one**

---

The output  $A < B$  is set to 1 when the input combinations is

▶ A=10, B=01

▶ A=11, B=01

▶ A=01, B=01

▶ A=01, B=10

**Question No: 3 ( Marks: 1 ) - Please choose one**

---

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

▶ True

▶ False

**Question No: 4 ( Marks: 1 ) - Please choose one**

---

High level Noise Margins ( $V_{NH}$ ) of CMOS 5 volt series circuits is

▶ 0.3 V

▶ 0.5 V

▶ 0.9 V

▶ 3.3 V

**Question No: 5 ( Marks: 1 ) - Please choose one**

---

If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be \_\_\_\_\_

- ▶ 24.582
- ▶ 2.4582
- ▶ 24582
- ▶ 0.24582

**Question No: 6 ( Marks: 1 ) - Please choose one**

---

The output of the expression  $F=A+B+C$  will be Logic \_\_\_\_\_ when  $A=0, B=1, C=1$ . the symbol '+' here represents OR Gate.

- ▶ Undefined
- ▶ One
- ▶ Zero
- ▶ 10 (binary)

**Question No: 7 ( Marks: 1 ) - Please choose one**

---

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be \_\_\_\_\_.

- ▶ SET
- ▶ RESET
- ▶ Clear
- ▶ Invalid

**Question No: 8 ( Marks: 1 ) - Please choose one**

3.3 v CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5 v CMOS series.

- ▶ Low switching speeds, high power dissipation
- ▶ Fast switching speeds, high power dissipation
- ▶ **Fast switching speeds, very low power dissipation**

page61

- ▶ Low switching speeds, very low power dissipation

**Question No: 9 ( Marks: 1 ) - Please choose one**

The binary value "1010110" is equivalent to decimal \_\_\_\_\_

▶ **86**

- ▶ 87
- ▶ 88
- ▶ 89

**Question No: 10 ( Marks: 1 ) - Please choose one**

The \_\_\_\_\_ Encoder is used as a keypad encoder.

- ▶ 2-to-8 encoder
- ▶ 4-to-16 encoder
- ▶ BCD-to-Decimal
- ▶ **Decimal-to-BCD Priority**

**Question No: 11 ( Marks: 1 ) - Please choose one**

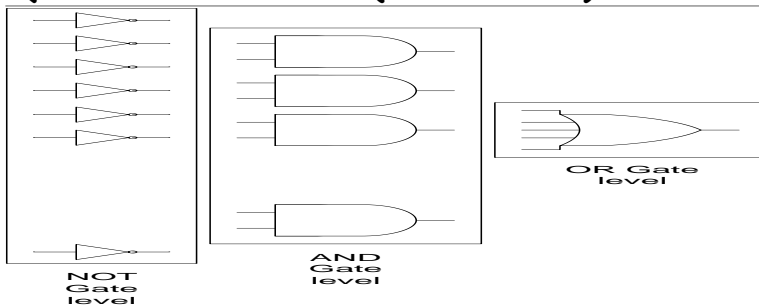
---

How many data select lines are required for selecting eight inputs?

- ▶ 1
- ▶ 2
- ▶ 3
- ▶ 4

---

Question No: 12 ( Marks: 1 ) - Please choose one



the diagram above shows the general implementation of \_\_\_\_\_ form

- ▶ Boolean
- ▶ Arbitrary
- ▶ POS
- ▶ SOP

page122

---

Question No: 13 ( Marks: 1 ) - Please choose one

The Quad Multiplexer has \_\_\_\_\_ outputs

- ▶ 4
- ▶ 8
- ▶ 12
- ▶ 16

---

Question No: 14 ( Marks: 1 ) - Please choose one

Demultiplexer has

- ▶ Single input and single outputs.
- ▶ Multiple inputs and multiple outputs.
- ▶ **Single input and multiple outputs.**
- ▶ Multiple inputs and single output.

**Question No: 15 ( Marks: 1 ) - Please choose one**

---

The expression \_\_\_\_\_ is an example of Commutative Law for Multiplication.

- ▶  $AB+C = A+BC$
- ▶  $A(B+C) = B(A+C)$
- ▶  **$AB=BA$**
- ▶  $A+B=B+A$

**Question No: 16 ( Marks: 1 ) - Please choose one**

---

"Sum-of-Weights" method is used \_\_\_\_\_

- ▶ **to convert from one number system to other**
- ▶ to encode data
- ▶ to decode data
- ▶ to convert from serial to parallel data

**Question No: 17 ( Marks: 2 )**

---

**Why a 2-bit comparator is called parallel comparator?**

**Answer:**

The 2-bit Comparator discussed earlier is considered to be a Parallel Comparator as all the bits are compared simultaneously. External Logic has to be used to Cascade together two such Comparators to form a 4-bit Comparator.

**Question No: 18 ( Marks: 2 )**

---

Explain at least two advantages of the circuit having low power consumption :

**Answer:**

**Power Dissipation**

Logic Gates and Logic circuits consume varying amount of power during their operation.

Ideally, logic gates and logic circuit should consume minimal power. Advantages of low power consumption are circuits that can be run from batteries instead of mains power supplies. Thus portable devices that run on batteries use Integrated circuits that have low power dissipation. Secondly, low power consumption means less heat is dissipated by the logic devices; this means that logic gates can be tightly packed to reduce the circuit size without having to worry about dissipating the access heat generated by the logic devices.

Microprocessors for example generate considerable heat which has to be dissipated by mounting small fans. Generally, the Power dissipation of TTL devices remains constant throughout their operation. CMOS device on the other hand dissipate varying amount power depending upon the frequency of operation.

**Question No: 19 ( Marks: 2 )**

---

**Name the four OLMC configurations**

**Answer:**

The four OLMC configurations are

- Combination Mode with active-low output
- Combinational Mode with active-high output
- Registered Mode with active-low output
- Registered Mode with active-high output

**Question No: 20 ( Marks: 3 )**

---

**Explain "Test Vector" in context of ABEL**

**Answer:**

The programming of a PLD device involves entering the logic function in the form of a Boolean equation, truth table or a state diagram. Any errors during the entry process are corrected. The software compiler processes the information in the input file and translates it into a suitable format. The compiler also minimizes the logic. The minimized logic is then tested by using a set of hypothetical inputs known as test vectors. The testing verifies the design of the logic circuit before committing it to the PLD.

**Question No: 22 ( Marks: 5 )**

---

**Explain Tri-State Buffers with the help of block diagram**

**Answer:**

**Tri-State Buffers**

Tri-State Buffer is a NOT gate with a control line that disconnects the output from the input. When the control line is high the buffer operates like a NOT gate and when the control line is low the output is disconnected from the output and high impedance is seen at the output. Tri-state buffers are used to disconnect the outputs of devices which are connected or share a common output line. Figure 20.9

Figure 20.9a Tri-State Buffer

**Question No: 23 ( Marks: 5 )**

---

**Explain the Operation of Odd-Parity Generator Circuit with the help of timing diagram**

**Answer:**

Operation of Odd-Parity Generator Circuit

The timing diagram shows the operation of the Odd-Parity generator circuit. Figure 14.3.

The A, B, C and D timing diagrams represent the changing 4-bit data values. During time interval t<sub>0</sub> the 4-bit data value is 0000, during time interval t<sub>1</sub>, the data value changes to 0001.

Similarly during time intervals t<sub>2</sub>, t<sub>3</sub>, t<sub>4</sub> up to t<sub>8</sub> the data values change to 0010, 0011, 0100 and 1000 respectively. During interval t<sub>0</sub> the output of the two XOR gates is 0 and 0, therefore the output of the XNOR gate is 1. At interval t<sub>1</sub>, the outputs of the two XOR gates is 1 and 0, therefore the output of the XNOR gate is 0. The output P can similarly be traced for intervals t<sub>2</sub> to t<sub>8</sub>.

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Paper # 2

MIDTERM EXAMINATION  
Spring 2009  
CS302- Digital Logic Design (Session - 1)

Question No: 1 ( Marks: 1 ) - Please choose one

---

In the binary number "10011" the weight of the most significant digit is \_\_\_\_\_

- ▶ **2<sup>4</sup> (2 raise to power 4)**
- ▶ 2<sup>3</sup> (2 raise to power 3)
- ▶ 2<sup>0</sup> (2 raise to power 0)
- ▶ 2<sup>1</sup> (2 raise to power 1)

Question No: 2 ( Marks: 1 ) - Please choose one

---

An S-R latch can be implemented by using \_\_\_\_\_ gates

- ▶ AND, OR
- ▶ **NAND, NOR**
- ▶ NAND, XOR
- ▶ NOT, XOR

Question No: 3 ( Marks: 1 ) - Please choose one

---

A latch has \_\_\_\_\_ stable states

- ▶ One
- ▶ **Two**
- ▶ Three
- ▶ Four

**Question No: 4 ( Marks: 1 ) - Please choose one**

---

Sequential circuits have storage elements

**▶ True**

▶ False

**Question No: 5 ( Marks: 1 ) - Please choose one**

---

The ABEL symbol for "XOR" operation is

**▶ \$**

▶ #

▶ !

▶ &

**Question No: 6 ( Marks: 1 ) - Please choose one**

---

A Demultiplexer is not available commercially.

**▶ True**

▶ False

**Question No: 7 ( Marks: 1 ) - Please choose one**

---

Using multiplexer as parallel to serial converter requires \_\_\_\_\_ connected to the multiplexer

**▶ A parallel to serial converter circuit**

▶ A counter circuit

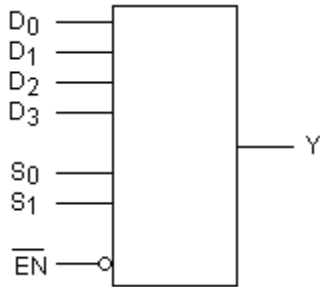
▶ A BCD to Decimal decoder

▶ A 2-to-8 bit decoder

**Question No: 8 ( Marks: 1 ) - Please choose one**

---

The device shown here is most likely a



- ▶ Comparator
- ▶ **Multiplexer**
- ▶ Demultiplexer
- ▶ Parity generator

**Question No: 9 ( Marks: 1 ) - Please choose one**

The main use of the Multiplexer is to

▶ **Select data from multiple sources and to route it to a single Destination**

- ▶ Select data from Single source and to route it to a multiple Destinations
- ▶ Select data from Single source and to route to single destination
- ▶ Select data from multiple sources and to route to multiple destinations

**Question No: 10 ( Marks: 1 ) - Please choose one**

A logic circuit with an output  $X = \overline{A}BC + A\overline{B}$  consists of

\_\_\_\_\_.

- ▶ two AND gates, two OR gates, two inverters
- ▶ three AND gates, two OR gates, one inverter
- ▶ **two AND gates, one OR gate, two inverters**

- ▶ two AND gates, one OR gate

**Question No: 11 ( Marks: 1 ) - Please choose one**

The binary value of 1010 is converted to the product term  $\overline{A}B\overline{C}D$

- ▶ True

▶ False

**Question No: 12 ( Marks: 1 ) - Please choose one**

The 3-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms

- ▶ 4

▶ 8

- ▶ 12

- ▶ 16

**Question No: 13 ( Marks: 1 ) - Please choose one**

Following is standard POS expression

$$(A + \overline{B} + C + \overline{D})(A + \overline{B} + C + D)(A + B + \overline{C} + \overline{D})(A + B + C + \overline{D})(A + \overline{B} + \overline{C} + D)$$

▶ True

- ▶ False

**Question No: 14 ( Marks: 1 ) - Please choose one**

The output of the expression  $F=A+B+C$  will be Logic \_\_\_\_\_ when  $A=0, B=1, C=1$ . the symbol '+' here represents OR Gate.

- ▶ Undefined
- ▶ **One**
- ▶ Zero
- ▶ 10 (binary)

**Question No: 15 ( Marks: 1 ) - Please choose one**

---

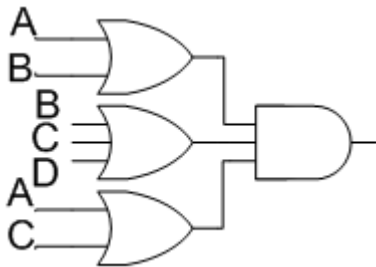
The Extended ASCII Code (American Standard Code for Information Interchange) is a \_\_\_\_\_ code

- ▶ 2-bit
- ▶ 7-bit
- ▶ **8-bit**
- ▶ 16-bit

**Question No: 16 ( Marks: 1 ) - Please choose one**

---

The diagram given below represents \_\_\_\_\_



- ▶ Demorgans law
- ▶ Associative law
- ▶ **Product of sum form**
- ▶ Sum of product form

**Question No: 17 ( Marks: 1 )**

---

How can a PLD be programmed?

Answer:

PLDs are programmed with the help of computer which runs the programming software. The computer is connected to a programmer socket in which the PLD is inserted for programming. PLDs can also be programmed when they are installed on a circuit board

**Question No: 18 ( Marks: 1 )**

---

How many input and output bits do a Half-Adder contain?

**Answer:**

The Half-Adder has a 2-bit input and a 2-bit output.

**Question No: 19 ( Marks: 2 )**

---

Explain the difference between 1-to-4 Demultiplexer 2-to-4 Binary Decoder?

**Answer:**

The circuit of the 1-to-4 Demultiplexer is similar to the 2-to-4 Binary Decoder described earlier figure 16.9. The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit figure

**Question No: 20 ( Marks: 3 )**

---

Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL.

**Answer:**

Device declaration, pin declarations and set declarations.

**Question No: 21 ( Marks: 5 )**

---

Explain with example how noise affects Operation of a CMOS AND Gate circuit.

**Answer:**

Two CMOS 5 volt series AND gates are connected together. Figure 7.3 The first AND gate has both its inputs connected to logic high, therefore the output of the gate is guaranteed to be logic high. The logic high voltage output of the first AND gate is assumed to be 4.6 volts well within the valid VOH range of 5-4.4 volts. Assume the same noise signal (as described earlier) is added to the output signal of the first AND gate.

**Question No: 22 ( Marks: 10 )**

---

**explain the SOP based implementation of the Adjacent 1s Detector Circuit:**

**Answer:**

The Adjacent 1s Detector accepts 4-bit inputs. If two adjacent 1s are detected in the input, the output is set to high. The operation of the Adjacent 1s Detector is represented by the function table. Table 13.6. In the function table, for the input combinations 0011, 0110, 0111, 1011, 1100, 1101, 1110 and 1111 the output function is a 1. Implementing the circuit directly from the function table based on the SOP form requires 8 AND gates for the 8 product terms (minterms) with an 8-input OR gate. Figure 13.3.

The total gate count is

- One 8 input OR gate
- Eight 4 input AND gates
- Ten NOT gates

The expression can be simplified using a Karnaugh map, figure 13.4, and then the simplified expression can be implemented to reduce the gate count. The simplified expression

is  $AB + CD + BC$  . The circuit implemented using the expression  $AB + CD + BC$  has reduced to 3 input OR gate and 2 input AND gates.

The simplified Adjacent 1s Detector circuit uses only four gates reducing the cost, the size of the circuit and the power requirement. The propagation delay of the circuit is of the order of two gates

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Paper # 3

**MIDTERM EXAMINATION**

Fall 2009  
CS302- Digital Logic Design (Session - 5)

Ref No: 1022709

Time: 60 min

Marks: 38

Question No: 1 ( Marks: 1 ) - Please choose one

---

According to Demorgan's theorem:

$$\overline{A+B+C} = \underline{\hspace{2cm}}$$

- ▶  $A.B.C$
- ▶  $A+\overline{B.C}$
- ▶  $\overline{A.B.C}$
- ▶  $\overline{A.B+C}$

Question No: 2 ( Marks: 1 ) - Please choose one

---

The Extended ASCII Code (American Standard Code for Information Interchange) is a \_\_\_\_\_ code

- ▶ 2-bit
- ▶ 7-bit
- ▶ 8-bit
- ▶ 16-bit

Question No: 3 ( Marks: 1 ) - Please choose one

---

The AND Gate performs a logical \_\_\_\_\_ function

- ▶ Addition
- ▶ Subtraction
- ▶ Multiplication
- ▶ Division

**Question No: 4 ( Marks: 1 ) - Please choose one**

---

NOR gate is formed by connecting \_\_\_\_\_

- ▶ OR Gate and then NOT Gate
- ▶ NOT Gate and then OR Gate
- ▶ **AND Gate and then OR Gate**
- ▶ OR Gate and then AND Gate

page50

**Question No: 5 ( Marks: 1 ) - Please choose one**

---

Generally, the Power dissipation of \_\_\_\_\_ devices remains constant throughout their operation.

- ▶ **TTL**
- ▶ CMOS 3.5 series
- ▶ CMOS 5 Series
- ▶ Power dissipation of all circuits increases with time.

**Question No: 6 ( Marks: 1 ) - Please choose one**

---

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

- ▶ **True**
- ▶ False

**Question No: 7 ( Marks: 1 ) - Please choose one**

---

When the control line in tri-state buffer is high the buffer operates like a \_\_\_\_\_ gate

- ▶ AND
- ▶ OR
- ▶ NOT
- ▶ XOR

**Question No: 8 ( Marks: 1 ) - Please choose one**

---

The GAL22V10 has \_\_\_\_\_ inputs

- ▶ 22
- ▶ 10
- ▶ 44
- ▶ 20

**Question No: 9 ( Marks: 1 ) - Please choose one**

---

The ABEL symbol for "OR" operation is

- ▶ !
- ▶ &
- ▶ #
- ▶ \$

Logic Operation ABEL Symbol

NOT	!
AND	&
OR	#
XOR	\$

**Question No: 10 ( Marks: 1 ) - Please choose one**

---

The OLMC of the GAL16V8 is \_\_\_\_\_ to the OLMC of the GAL22V10

- ▶ Similar
- ▶ Different
- ▶ **Similar with some enhancements**
- ▶ Depends on the type of PALs input size

**Question No: 11 ( Marks: 1 ) - Please choose one**

---

All the ABEL equations must end with \_\_\_\_\_

- ▶ "." (a dot)
- ▶ "\$" (a dollar symbol)
- ▶ **":" (a semicolon)**
- ▶ "endl" (keyword "endl")

**Question No: 12 ( Marks: 1 ) - Please choose one**

---

The Quad Multiplexer has \_\_\_\_\_ outputs

- ▶ **4**
- ▶ 8
- ▶ 12
- ▶ 16

**Question No: 13 ( Marks: 1 ) - Please choose one**

---

"Sum-of-Weights" method is used \_\_\_\_\_

- ▶ **to convert from one number system to other**
- ▶ to encode data
- ▶ to decode data
- ▶ to convert from serial to parralel data

**Question No: 14 ( Marks: 1 ) - Please choose one**

---

Circuits having a bubble at their outputs are considered to have an active-low output.

▶ True

▶ False

**Question No: 15 ( Marks: 1 ) - Please choose one**

---

$(A+B)(A+\bar{B}+C)(\bar{A}+C)$  is an example of \_\_\_\_\_

▶ Product of sum form

- ▶ Sum of product form
- ▶ Demorgans law
- ▶ Associative law

**Question No: 16 ( Marks: 1 ) - Please choose one**

---

Which one is true:

▶ Power consumption of TTL is higher than of CMOS

- ▶ Power consumption of CMOS is higher than of TTL
- ▶ Both TTL and CMOS have same power consumption
- ▶ Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

**Question No: 17 ( Marks: 1 )**

---

Which device performs an operation which is the opposite of the Decoder function?

Answer:

Encoder function.

**Question No: 18 ( Marks: 1 )**

---

Name any two modes in which PALs are programmed.

**Answer:**

PAL devices are programmed by blowing the fuses permanently using over voltage.

**Question No: 19 ( Marks: 2 )**

---

Explain Combinational Function Devices?

**Ans;**

Xor, Xnor, NAND, NOR are combinational function devices.

**Question No: 20 ( Marks: 3 )**

---

Differentiate between hexadecimal and octal number system

**Answer:**

**Octal - base 8**

**Hexadecimal - base 16**

Octal and hex are used to represent numbers instead of decimal because there is a very easy and direct way to convert from the "real" way that computers store numbers (binary) to something easier for humans to handle (fewer symbols). To translate a binary number to octal, simply group the binary digits three at a time and convert each group. For hex, group the binary digits four at a time.

**Question No: 21 ( Marks: 5 )**

---

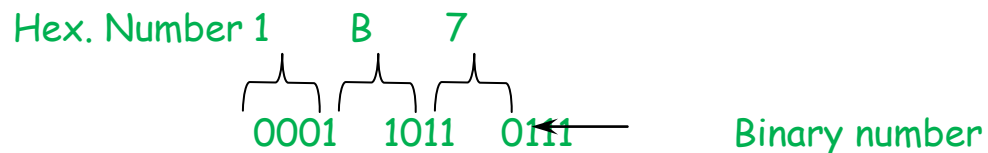
Explain "Sum-of-Weights Method" for Hexadecimal to Decimal Conversion with at least one example ?

**Answer:**

The hexadecimal (Hex) numbering system provides even shorter notation than octal. Hexadecimal uses a base of 16. It employs 16 digits: number 0 through 9, and letters A through F, with A through F substituted for numbers 10 to 15, respectively, Hexadecimal numbers can be expressed as their decimal equivalents by using the sum of weights method, as shown in the following example:

Weight	2	1	0	
Hex. Number	1	B	7	
				$7 \times 16^0 = 7 \times 1 = 7$
				$11 \times 16^1 = 11 \times 16 = 176$
				$1 \times 16^2 = 1 \times 256 = 256$
Sum of products				439 <sub>10</sub>

Like octal numbers, hexadecimal numbers can easily be converted to binary or vice versa. Conversion is accomplished by writing the 4-bit binary equivalent of the hex digit for each position, as illustrated in the following example:



Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7

8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

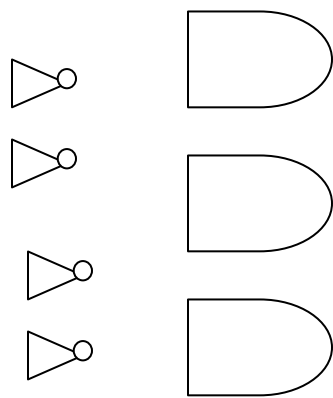
**Question No: 22 ( Marks: 10 )**

Draw the function table of two-bit comparator circuit, map it to K-Map and derive the expression for  $(A > B)$

Ans:

$X_1$	$X_0$	$Y_1$	$Y_0$	$X < Y$	$X = Y$	$X > Y$
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1

1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0



The circuit has inputs  $X_1X_0$  and  $Y_1Y_0$  and outputs  $X \succ Y$ ,  
the expression for  $\succ$  is  $X_1 \bar{Y}_1 + X_0 \bar{Y}_1 \bar{Y}_0 + X_1 X_0 \bar{Y}_0$   
time is out.....

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**Hearthacker124@gmail.com**

**MIDTERM EXAMINATION**  
**Spring 2010**  
**CS302- Digital Logic Design (Session - 6)**  
**Ref No: 1351363**  
**Time: 60 min**  
**Marks: 38**

**Question No: 1 ( Marks: 1 ) - Please choose one**

---

The maximum number that can be represented using unsigned octal system is \_\_\_\_\_

- ▶ 1
- ▶ 7
- ▶ 9
- ▶ 16

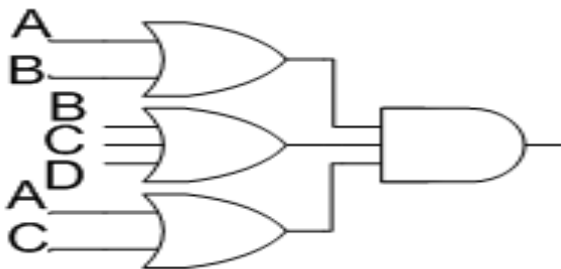
**Question No: 2 ( Marks: 1 ) - Please choose one**

If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be \_\_\_\_\_

- ▶ 0
- ▶ 1
- ▶ 2
- ▶ 3

**Question No: 3 ( Marks: 1 ) - Please choose one**

The diagram given below represents \_\_\_\_\_



- ▶ Demorgans law
- ▶ Associative law
- ▶ Product of sum form
- ▶ Sum of product form

**Question No: 4 ( Marks: 1 ) - Please choose one**

The range of Excess-8 code is from \_\_\_\_\_ to \_\_\_\_\_

▶ +7 to -8

▶ +8 to -7

▶ +9 to -8

▶ -9 to +8

**Question No: 5 ( Marks: 1 ) - Please choose one**

A non-standard POS is converted into a standard POS by using the rule \_\_\_\_\_

▶  $A + \bar{A} = 1$

▶  $A\bar{A} = 0$

▶  $1 + A = 1$

▶  $A + B = B + A$

**Question No: 6 ( Marks: 1 ) - Please choose one**

The 3-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms

▶ 4

▶ 8

▶ 12

▶ 16

**Question No: 7 ( Marks: 1 ) - Please choose one**

The binary numbers  $A = 1100$  and  $B = 1001$  are applied to the inputs of a comparator. What are the output levels?

▶  $A > B = 1, A < B = 0, A < B = 1$

- ▶  $A > B = 0, A < B = 1, A = B = 0$
- ▶  $A > B = 1, A < B = 0, A = B = 0$
- ▶  $A > B = 0, A < B = 1, A = B = 1$

**Question No: 8 ( Marks: 1 ) - Please choose one**

---

A particular Full Adder has

- ▶ 3 inputs and 2 output
- ▶ 3 inputs and 3 output
- ▶ 2 inputs and 3 output
- ▶ 2 inputs and 2 output

**Question No: 9 ( Marks: 1 ) - Please choose one**

---

The function to be performed by the processor is selected by set of inputs known as \_\_\_\_\_

- ▶ *Function Select Inputs*
- ▶ MicroOperation selectors
- ▶ OPCODE Selectors
- ▶ None of given option

**Question No: 10 ( Marks: 1 ) - Please choose one**

---

For a 3-to-8 decoder how many 2-to-4 decoders will be required?

- ▶ 2
- ▶ 1
- ▶ 3

▶ 4

**Question No: 11 ( Marks: 1 ) - Please choose one**

---

GAL is an acronym for \_\_\_\_\_.

- ▶ Giant Array Logic
- ▶ General Array Logic
- ▶ **Generic Array Logic** page183
- ▶ Generic Analysis Logic

**Question No: 12 ( Marks: 1 ) - Please choose one**

---

The Quad Multiplexer has \_\_\_\_\_ outputs

▶ 4

- ▶ 8
- ▶ 12
- ▶ 16

**Question No: 13 ( Marks: 1 ) - Please choose one**

---

$A.(B.C) = (A.B).C$  is an expression of \_\_\_\_\_

- ▶ Demorgan's Law
- ▶ Distributive Law
- ▶ Commutative Law
- ▶ **Associative Law**

**Question No: 14 ( Marks: 1 ) - Please choose one**

---

2's complement of any binary number can be calculated by

- ▶ adding 1's complement twice
- ▶ **adding 1 to 1's complement**
- ▶ subtracting 1 from 1's complement.
- ▶ calculating 1's complement and inverting most significant bit

**Question No: 15 ( Marks: 1 ) - Please choose one**

---

The binary value "1010110" is equivalent to decimal \_\_\_\_\_

- ▶ **86**
- ▶ 87
- ▶ 88
- ▶ 89

**Question No: 16 ( Marks: 1 ) - Please choose one**

---

Tri-State Buffer is basically a/an \_\_\_\_\_ gate.

- ▶ AND
- ▶ OR
- ▶ NOT
- ▶ **XOR**

**Question No: 17 ( Marks: 2 )**

---

For what values of A, B, C and D, value of the expression given below will be logic 1. Explain at least one combination.

$$\overline{A}B + \overline{\overline{A}B.CD}$$

**Ans:**

The Multiplexers are used to route the contents of any two registers to the ALU inputs.

Many Audio signals in telephone network.

Computer use Dynamic Memory addressing using same address line for row and column addressing to access data.

**Question No: 18 ( Marks: 2 )**

---

Provide some of the inputs for which the adjacent 1s detector circuit have active high output?

**Ans:**

The Adjacent 1s Detector accepts 4-bit inputs.

If two adjacent 1s are detected in the input, the output is set to high.

input combinations will be

1. 0011,
2. 0110,
3. 0111,
4. 1011,
5. 1100,
6. 1101,
7. 1110 and
8. 1111

the output function is a 1.

**Question No: 19 ( Marks: 2 )**

---

**Draw the Truth-Table of NOR based S-R Latch**

S	R	Action
0	0	Keep state
0	1	Q=0
1	0	Q=1
1	1	Restricted combination

**Question No: 20 ( Marks: 3 )**

---

**For a two bit comparator circuit specify the inputs for which  $A > B$**

**Ans:**

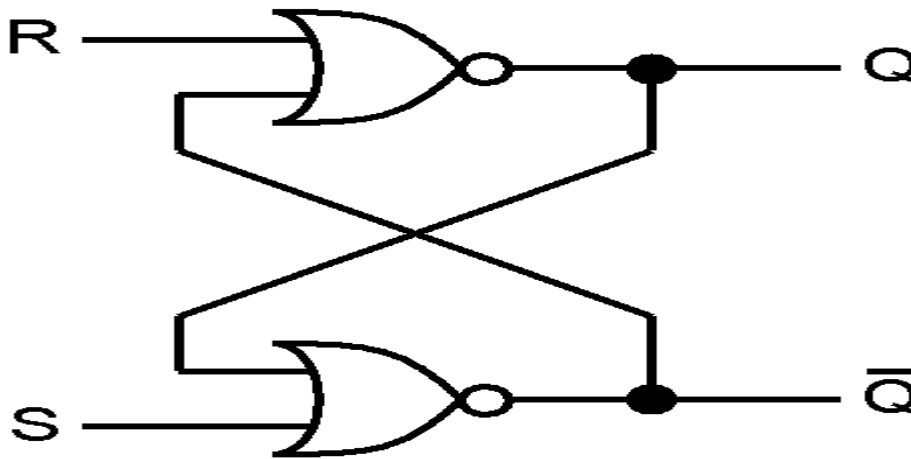
1. 01 00,
2. 10 00,
3. 10 01,
4. 11 00,
5. 11 01 and
6. 11 10

Question No: 21 ( Marks: 3 )

---

Draw the circuit diagram of NOR based S-R Latch ?

Ans:



Question No: 22 ( Marks: 5 )

---

One of the ABEL entry methods uses logic equations; explain it with at least a single example.

Ans:

In ABEL any letter or combination of letters and numbers can be used to identify variables.

ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'.

All ABEL equations must end with ';'.

Boolean expression  $F = AB' + AC + (BD)'$  is written in ABEL as  $F = A \&! B \# A \& C \#! B \& !D;$

Question No: 23 ( Marks: 5 )

---

Explain Carry propagation in Parallel binary adder?

Ans:

Parallel binary adder:

A binary adder circuit is described using dynamic transistor logic in which for high speed carry propagation the adder stages are grouped in pairs or larger numbers and additional dynamic logic means is provided in each group to control a single transistor connected in series in the carry propagation path over the group.

The transistors used in the specific embodiments are MOS transistors, but some or all of these could be replaced by junction FET's or bipolar transistors.

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Paper # 4

**MIDTERM EXAMINATION**  
**Spring 2009**  
**CS302- Digital Logic Design (Session - 1)**

Question No: 1 ( Marks: 1 ) - Please choose one

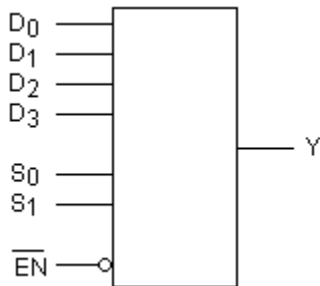
GAL can be reprogrammed because instead of fuses \_\_\_\_\_  
logic is used in it

▶ E<sup>2</sup>CMOS

- ▶ TTL
- ▶ CMOS+
- ▶ None of the given options

Question No: 2 ( Marks: 1 ) - Please choose one

The device shown here is most likely a



- ▶ Comparator
- ▶ Multiplexer
- ▶ Demultiplexer
- ▶ Parity generator

Question No: 3 ( Marks: 1 ) - Please choose one

If "1110" is applied at the input of BCD-to-Decimal decoder  
which output pin will be activated?

- ▶ 2<sup>nd</sup>
- ▶ 4<sup>th</sup>
- ▶ 14<sup>th</sup>

▶ No output wire will be activated

**Question No: 4 ( Marks: 1 ) - Please choose one**

---

Half-Adder Logic circuit contains 2 XOR Gates

- ▶ True
- ▶ False

**Question No: 5 ( Marks: 1 ) - Please choose one**

---

A particular Full Adder has

- ▶ 3 inputs and 2 output
- ▶ 3 inputs and 3 output
- ▶ 2 inputs and 3 output
- ▶ 2 inputs and 2 output

**Question No: 6 ( Marks: 1 ) - Please choose one**

---

$$\text{Sum} = A \oplus B \oplus C$$

$\text{CarryOut} = C(A \oplus B) + AB$  are the Sum and CarryOut expression of

- ▶ Half Adder
- ▶ Full Adder
- ▶ 3-bit parralel adder
- ▶ MSI adder cicuit

**Question No: 7 ( Marks: 1 ) - Please choose one**

---

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

▶ True

▶ False

**Question No: 8 ( Marks: 1 ) - Please choose one**

---

The output  $A < B$  is set to 1 when the input combinations is

---

▶ A=10, B=01

▶ A=11, B=01

▶ A=01, B=01

▶ A=01, B=10

Here output combination should  $A < B$

**Question No: 9 ( Marks: 1 ) - Please choose one**

---

The 4-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms

▶ 4

▶ 8

▶ 12

▶ 16

**Question No: 10 ( Marks: 1 ) - Please choose one**

---

Generally, the Power dissipation of \_\_\_\_\_ devices remains constant throughout their operation.

▶ TTL

- ▶ CMOS 3.5 series
- ▶ CMOS 5 Series
- ▶ Power dissipation of all circuits increases with time.

**Question No: 11 ( Marks: 1 ) - Please choose one**

---

The decimal "8" is represented as \_\_\_\_\_ using Gray-Code.

- ▶ 0011
- ▶ 1100
- ▶ 1000
- ▶ 1010

**Question No: 12 ( Marks: 1 ) - Please choose one**

---

$(A+B).(A+C) =$  \_\_\_\_\_

- ▶ B+C
- ▶ A+BC
- ▶ AB+C
- ▶ AC+B

**Question No: 13 ( Marks: 1 ) - Please choose one**

---

$A.(B + C) = A.B + A.C$  is the expression of \_\_\_\_\_

- ▶ Demorgan's Law
- ▶ Commutative Law
- ▶ Distributive Law
- ▶ Associative Law

**Question No: 14 ( Marks: 1 ) - Please choose one**

---

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

- FALSE
- TRUE

**Question No: 15 ( Marks: 1 ) - Please choose one**

---

In ANSI/IEEE Standard 754 "Mantissa" is represented by \_\_\_\_-bits\_\_\_\_\_ bits

- 8-bits
- 16-bits
- 32-bits
- 64-bits

**Question No: 16 ( Marks: 1 ) - Please choose one**

---

Caveman number system is Base \_\_\_\_\_ number system

- 2
- 5
- 10
- 16

**Question No: 17 ( Marks: 1 )**

---

Briefly state the basic principle of **Repeated Multiplication-by-2 Method**.

Ans:

**Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary.**

**Question No: 18 ( Marks: 1 )**

---

How standard Boolean expressions can be converted into truth table format.

**Ans:**

Standard Boolean expressions can be converted into truth table format using binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.

**Question No: 19 ( Marks: 2 )**

---



What will be the out put of the diagram given below  
 $A.B + A.B.C.D$

**Question No: 20 ( Marks: 3 )**

---

When an Input (source) file is created in ABEL a module is created which has three sections. Name These three sections.

**Answer:**

The three sections are:

- Boolean Equations
- Truth Tables
- State Diagrams

**Question No: 21 ( Marks: 5 )**

---

Explain "AND" Gate and some of its uses :

**Answer:**

AND gates are used to combine multiple signals, if all the signals are TRUE then the output will also be TRUE. If any of the signals are FALSE, then the output will be false. ANDs aren't used as much as NAND gates; NAND gates use less components and have the advantage that they be used as an inverter.

Question No: 22 ( Marks: 10 )

---

Write down different situations where we need the sequential circuits.

Answer:

Digital circuits that use memory elements for their operation are known as Sequential circuits. Thus Sequential circuits are implemented by combining combinational circuits with memory elements.

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**Question No: 1 ( Marks: 1 ) - Please choose one**

---

Which of the number is not a representative of hexadecimal system

- ▶ 1234
- ▶ ABCD
- ▶ 1001
- ▶ DEFH

**Question No: 2 ( Marks: 1 ) - Please choose one**

---

The Unsigned Binary representation can only represent positive binary numbers

- ▶ True
- ▶ False

**Question No: 3 ( Marks: 1 ) - Please choose one**

---

The values that exceed the specified range can not be correctly represented and are considered as \_\_\_\_\_

- ▶ Overflow page23
- ▶ Carry
- ▶ Parity
- ▶ Sign value

**Question No: 4 ( Marks: 1 ) - Please choose one**

---

The 4-bit 2's complement representation of "-7" is

---

- ▶ 0111
- ▶ 1111

▶ 1001

▶ 0110

L-2

**Question No: 5 ( Marks: 1 ) - Please choose one**

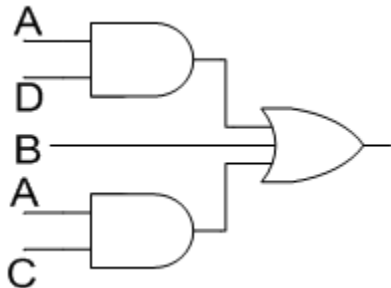
$\overline{AB} + \overline{ABC} + AC$  is an example of \_\_\_\_\_

▶ Product of sum form

- ▶ Sum of product form
- ▶ Demorgans law
- ▶ Associative law

**Question No: 6 ( Marks: 1 ) - Please choose one**

The diagram given below represents \_\_\_\_\_



- ▶ Demorgans law
- ▶ Associative law
- ▶ Product of sum form
- ▶ Sum of product form

**Question No: 7 ( Marks: 1 ) - Please choose one**

The output of an AND gate is one when \_\_\_\_\_

- ▶ All of the inputs are one
- ▶ Any of the input is one
- ▶ Any of the input is zero

- ▶ All the inputs are zero

**Question No: 8 ( Marks: 1 ) - Please choose one**

---

The 4-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms

- ▶ 4
- ▶ 8
- ▶ 12
- ▶ 16

**Question No: 9 ( Marks: 1 ) - Please choose one**

---

A BCD to 7-Segment decoder has

- ▶ 3 inputs and 7 outputs
- ▶ 4 inputs and 7 outputs
- ▶ 7 inputs and 3 outputs
- ▶ 7 inputs and 4 outputs

**Question No: 10 ( Marks: 1 ) - Please choose one**

---

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a \_\_\_\_\_ multiplexer.

- ▶ 4-input, 8-bit
- ▶ 4-input, 16-bit
- ▶ 2-input, 8-bit
- ▶ 2-input, 4-bit

**Question No: 11 ( Marks: 1 ) - Please choose one**

---

The PROM consists of a fixed non-programmable  
\_\_\_\_\_ Gate array configured as a decoder.

- AND
- OR
- NOT
- XOR

---

**Question No: 12 ( Marks: 1 ) - Please choose one**

In ABEL the variable 'A' is treated separately from variable 'a'

- True
- False

---

**Question No: 13 ( Marks: 1 ) - Please choose one**

The ABEL notation equivalent to Boolean expression  $A+B$  is:

- A & B
- A ! B
- A # B
- A \$ B

L-21

---

**Question No: 14 ( Marks: 1 ) - Please choose one**

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be

\_\_\_\_\_.

- SET
- RESET
- Clear
- Invalid

**Question No: 15 ( Marks: 1 ) - Please choose one**

---

Demultiplexer has

- ▶ Single input and single outputs.
- ▶ Multiple inputs and multiple outputs.
- ▶ **Single input and multiple outputs.**
- ▶ Multiple inputs and single output.

**Question No: 16 ( Marks: 1 ) - Please choose one**

---

Which one is true:

- ▶ **Power consumption of TTL is higher than of CMOS**
- ▶ Power consumption of CMOS is higher than of TTL
- ▶ Both TTL and CMOS have same power consumption
- ▶ Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

**Question No: 17 ( Marks: 1 )**

---

Briefly state the basic principle of **Repeated Division-by-2** method.

**Repeated Division-by-2**

Repeated Division-by-2 method allows decimal numbers of any magnitude to be converted into binary. In this method the Decimal number to be converted into its Binary equivalent is repeatedly divided by 2. The divisor is selected as 2 because the decimal number is being converted into Binary a Base-2 Number system. Repeated division method can be used to convert decimal number into any Number system by repeated division by the Base-Number. For example, the decimal number can be converted into the Caveman Number system by repeatedly dividing by 5, the Base number of the Caveman Number System. The Repeated

Division method will be used in latter lectures to convert decimal into Hexadecimal and Octal Number Systems.

In the Repeated-Division method the Decimal number to be converted is divided by the Base Number, in this particular case 2. A quotient value and a remainder value is generated, both values are noted down. The remainder value in all subsequent divisions would be either a 0 or a 1. The quotient value obtained as a result of division by 2 is divided again by 2. The new quotient and remainder values are again noted down. In each step of the repeated division method the remainder values are noted down and the quotient values are repeatedly divided by the base number. The process of repeated division stops when the quotient value becomes zero. The remainders that have been noted in consecutive steps are written out to indicate the Binary equivalent of the Original Decimal Number.

**Question No: 18 ( Marks: 1 )**

---

Briefly state the basic principle of **Repeated Multiplication-by-2 Method**.

**Repeated Multiplication-by-2 Method**

An alternate to the Sum-of-Weights method used to convert Decimal fractions to equivalent Binary fractions is the repeated multiplication by 2 methods. In this method the number to be converted is repeatedly multiplied by the Base Number to which the number is being converted to, in this case 2. A new number having an Integer part and a

Fraction part is generated after each multiplication. The Integer part is noted down and the fraction part is again multiplied with the Base number 2. The process is repeated until the fraction term becomes equal to zero.

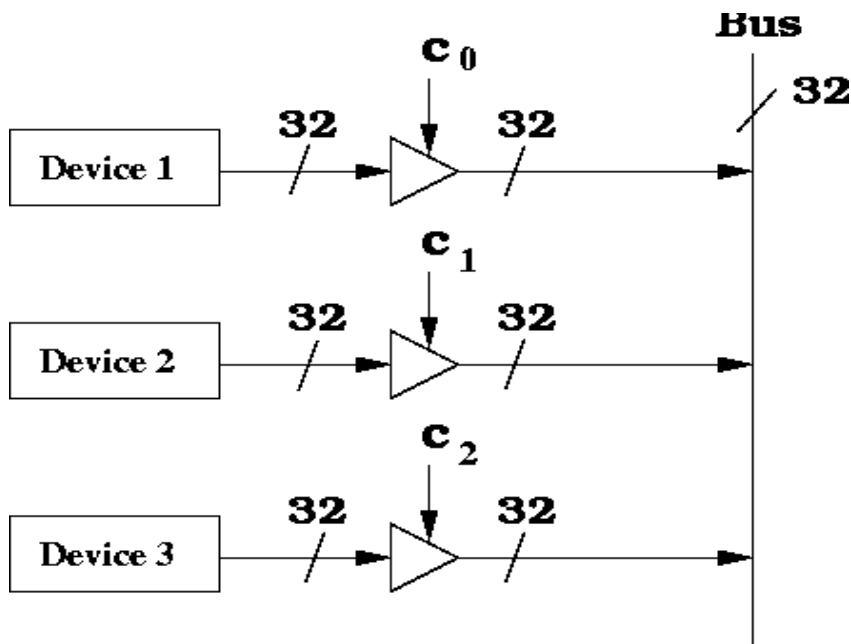
Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary. The conversion of Decimal fraction 0.625 into Binary equivalent using the

Repeated Multiplication-by-2 method is illustrated in a tabular form.

Table 2.4. Reading the Integer column from bottom to top and placing a decimal point in the left most position gives 0.101 the binary equivalent of decimal fraction 0.625

**Question No: 19 ( Marks: 2 )**

Draw the circuit diagram of a Tri-State buffer.



**Question No: 20 ( Marks: 3 )**

Add -13 and +7 by converting them in binary system your result must be in binary.

**Question No: 21 ( Marks: 5 )**

Explain "Sum of Weights" method with example for "Octal to Decimal" conversion

1. Sum-of-Weights Method

Sum-of-weights as the name indicates sums the weights of the Binary Digits (bits) of a Binary Number which is to be

represented in Decimal. The Sum-of-Weights method can be used to convert a Binary number of any magnitudes to its equivalent Decimal representation.

In the Sum-of-Weights method an extended expression is written in terms of the Binary Base Number 2 and the weights of the Binary number to be converted. The weights correspond to each of the binary bits which are multiplied by the corresponding binary value. Binary bits having the value 0 do not contribute any value towards the final sum expression.

The Binary number 101102 is therefore written in the form of an expression having weights  $2^0, 2^1, 2^2, 2^3$  AND  $2^4$  corresponding to the bits 0, 1, 1, 0 and 1 respectively.

Weights  $2^0$  AND  $2^3$  do not contribute in the final sum as the binary bits corresponding to these weights have the value 0.

$$\begin{aligned} 101102 &= 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 \\ &= 16 + 0 + 4 + 2 + 0 \\ &= 22 \end{aligned}$$

**Question No: 22 ( Marks: 10 )**

---

Explain the Implementation of an Odd-Parity Generator Circuit i.e by drawing function table, mapping it to K-map and then simplifying the expression.

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**Hearthacker124@gmail.com**

## **Current paper subjective question:**

Was my CS302\_DLD paper. Total 23 questions out of which 16 MCQ's.

2 questions of two marks each were from the topic Adder.  
A boolean expression was given and had to find a logic 1 for it.  
One 5 marks question from parity method.

2day was my 2nd paper of cs302  
this was my papers

SOP to POS conversion	3mark
S-R latch Diagram	5mark
Nor gate table	3mark

8 to 3 bit encoder      5mark

Tri-stuff diagram      3mark

mcqz zyda tar start lec mn say aye thay

binary additin

2's complemnt

k-map

Assalam o Alaikum

Today I attempted CS302 paper

Paper was of 38 marks.

16 MCQs and 22 marks paper comprised of long questions.

2 marks question was "Write the uses of multiplexer".

2 marks question was "Write any two advantages of boolean expressions".

2 marks question was "Draw the diagram of odd parity generator circuit".

3 marks question was "What does a 8-bit adder/subtracter circuit do"?

3 marks question was "Draw the function table of 3 to 8 decoder".

5 marks question was "Describe 16 bit ALU".

5 marks question was "Describe in your own words about latches".

## CS302 CURRENT MIDTERM PAPER

What is the role of MOS transistor in Mask ROM?

How many input and output bits do a Half-Adder contain?

How can a PLD be programmed?

DRAW THE CIRCUIT DIAGRAM OF GATED S-R LATCH.?

Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL?

Explain with example how noise affects Operation of a CMOS AND Gate circuit?

GIVEN THE FOLLOWING STATEMENT USED IN PLD

PROGRAMMING:

```
Y PIN 23 ISTYPE 'COM';
```

Explain what does this statement mean?

VARIABLE Y AT OUTPUT PIN 23 WHICH IS A COMBINATIONAL OUTPUT AVAILABLE DIRECTLY FROM THE AND-OR GATE ARRAY OUTPUT.

Y = VARIABLE Y

PIN 23 = PIN NUMBER 23

ISTYPE "COM" = OUTPUT TYPE COMBINATIONAL

**ASSALAM O ALAIKUM all fellows**  
**ALL IN ONE Mega File**  
**CS302 Midterm PAPERS,**  
**MCQz & subjective**  
**Created BY Farhan& Ali**  
**BS (cs) 3rd sem**  
**Hackers Group**  
**Mandi Bahauddin**

**Remember us in your prayers**

**Mindhacker124@gmail.com**

**Hearthacker124@gmail.com**

Inputs                      Output

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

this function table represents \_\_\_\_\_ Gate.

Or gate

The ABEL symbol for “OR” operation is

#

A standard SOP form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.

Sum

which one of the following is not a valid rule of Boolean algebra?

$A = \bar{A}$

How many data select lines are required for selecting eight inputs?

3 (correct)

If two adjacent 1s are detected in the input, the output is set to high. input combinations will be

0011(ans)

The 4-variable Karnaugh Map (K-Map) has \_\_\_\_\_ rows and \_\_\_\_\_ columns

4,4, (ans)

The boolean expression  $A + B' + C$  is

a sum term(ans)

the boolean expression  $AB'CD'$  is

a product term(ans)

Don't care conditions are marked as \_\_\_\_\_ in the output column of the function table

X(ans)

An example of SOP expression is

both (a) and (b)(ans)

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1 (ans)

A SOP expression having a domain of 3 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values. Select correct option:

2 (Correct)

Multiplexers are also known as \_\_\_\_\_.

Data Selectors

The OR Gate performs a Boolean \_\_\_\_\_ function

Addition (Correct)

Sum term (Max term) is implemented using \_\_\_\_\_ gates

OR (Correct)

The number "1259" may belong to \_\_\_\_\_ number system.

Binary or Hexadecimal system (Correct)

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result

1111 (Correct)

"1101" in signed representation is equivalent to \_\_\_\_\_

13 (Correct)

TTL based devices work with a dc supply of \_\_\_\_\_ Volts

+5 (Correct)

In decimal value “275” the weight of the digit “7” is \_\_\_\_\_

100 (Not Sure)

The decimal “10” will have an octal equivalent \_\_\_\_\_

9 (Not Sure)

Caveman number system is Base \_\_\_\_\_ number system

5 (Correct)

How many bits must each word have in one-to-four line de-multiplexer to be implemented using a memory?

1 bits

The total amount of memory is depends upon \_\_\_\_\_

The size of the address bus of the microprocessor

\_\_\_\_\_ can be determined the Instability condition.

logic diagram

If we add an inverter at the output of AND gate, what function is produced?

NAND

Which is also known as coincidence detector?

AND gate

Transition table include \_\_\_\_\_

squares

For every possible combination of logical states in the inputs, which table shows the logical state of a digital circuit output?

**Truth table**

Stack is an acronym for \_\_\_\_\_

**LIFO memory**

When an Asynchronous sequential circuit changes two or more binary states variables a Condition occurs called \_\_\_\_\_

**Race condition**

positive OR gate is also a negative

**AND gate**

Time delay device is memory element of \_\_\_\_\_

**asynchronous circuits**

Boolean algebra is also called

- a) arithmetic algebra
- b) switching algebra
- c) **Both A & B**

Boolean function must be brought into \_\_\_\_\_ To perform product of max terms

**OR terms**

The binary number 10101 is equivalent to the decimal number \_\_\_\_\_.

**21**

The domain of expression  $ABCD + AB + CD + B$  is—

**B only**

The Boolean expression  $A BC D$  is—

**Sum term**

The universal gate is\_\_\_\_\_.

**NAND gate**

According to boolean algebra absorption law, which of the following is correct?

**$xy+y=x$**

A Boolean function may be transformed into  
**logical diagram**

The inverter is \_\_\_\_\_

**NOT gate**

The resulting circuit of a NAND gate are connected together is\_\_\_\_\_

**NOT gate**

**$x*y = y*x$  is the  
identity element**

Minterms are also called

**standard product**

OR gate and \_\_\_\_\_ will form The NOR gate?

**NOT gate**

The NAND gate is AND gate followed by .....

**NOT gate**

Max terms are also called\_\_\_\_\_.

**standard sum**

In Boolean algebra Multiplicative inverse is

**a**

By the repeated use of \_\_\_\_\_ Digital circuit can be made  
**NAND gates**

The only function of NOT gate is \_\_\_\_\_ of the following.

**Invert input signal**

Boolean algebra is defined as a set of \_\_\_\_\_.

**two values**

First operator precedence for evaluating Boolean expressions is

**Parenthesis**

The output is \_\_\_\_\_ When an input signal 1 is applied to a NOT gate

**0**

The bar sign (-) indicates \_\_\_\_\_ In Boolean algebra?

**NOT operation**

The value of n is \_\_\_\_\_ when the resolution of an n bit DAC with a maximum input of 5 V is 5 mV.

**10**

2's complement of binary number 0101 is \_\_\_\_\_

**1011**

An OR gate has 4 inputs. The output is ..... When One input is high and the other three are low.

**High**

To convert BCD to seven segments \_\_\_\_\_ device is used.

**Decoder**

Decimal number 10 is equal to binary number \_\_\_\_\_.

1010

In 2's complement representation the number 11100101 represents the decimal number \_\_\_\_\_.

-27

BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are \_\_\_\_\_.

All

A decade counter skips \_\_\_\_\_.

binary states 1010 to 1111

\_\_\_\_\_ Number of States A ring counter with 5 flip flops will have?

5

Positive edge-triggered flip-flop changes its state when \_\_\_\_\_

Low-to-high transition of clock

If  $S=1$  and  $R=1$ , for negative edge triggered flip-flop then  $Q(t+1) =$

Invalid

Adjacent 1s detector circuit will have active low output for the input

1101

A 5-variable karnaugh map has

**Thirty two cells**

8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer

**8-to-1 ok**

In asynchronous digital systems all the circuits change their state with respect to a common clock

**False**

Divide-by-32 counter can be achieved by using

**Flip-Flop and DIV 16**

The Synchronous counters are also known as Ripple Counters:

**False ok**

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

**25 mW**

The 3-to-8 Decoder has active-low outputs and three extra \_\_\_\_\_ gates connected at the three inputs to reduce the four unit load to a single unit load.

**Not**

Which of the number is not a representative of hexadecimal system?

**“1001” correct**

High level Noise Margins (VNH) of CMOS 5 volt series circuits is

\_\_\_\_\_

**0.9 V correct**

To get the answer “1” in Boolean addition of three variables, \_\_\_\_\_

**One of the variables must be 1 correct**

The 3-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms

8 correct

\_\_\_\_\_ is invalid number of cells in a single group formed by the adjacent cells in K-map

2 correct

Consider  $A=1, B=0, C=1$ . A, B and C represent the input of three bit NAND gate the output of the NAND gate will be \_\_\_\_\_

Zero

The Binary number 1011.101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_\_ separated by a decimal point.

1011, 101 correct

$1011+101 =$  \_\_\_\_\_

10000 correct

Adding two octal numbers "36" and "71" result in \_\_\_\_\_

127 correct

The first Least Most digit in decimal number system has

Has position 0 and weight equal to 1 not sure

Sum term (Max term) is implemented using \_\_\_\_\_ gates

OR correct

The OR Gate performs a Boolean \_\_\_\_\_ function

Addition correct

Adding two octal numbers “36” and “71” result in \_\_\_\_\_

127 correct

If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be \_\_\_\_\_

24582 not sure

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

TRUE correct

The three fundamental gates are \_\_\_\_\_

NOT, OR, AND correct

A SOP expression having a domain of 3 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.

8 correct

The 4-variable K-Map has \_\_\_\_\_ rows and \_\_\_\_\_ columns of cells.

4, 4 correct

NAND gate is form by connecting \_\_\_\_\_

AND Gate and then NOT Gate correct

Which of the following is the octal equivalent of 28 decimal number?

34

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

$(2^{64})-1$

In a 4-variable K-map, a 2-variable product term is produced by  
a 4-cell group of 1s

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term present in the expression.

1

The \_\_\_\_\_ input select/deselects both the decoders simultaneously.

Enable

NAND and \_\_\_\_\_ gates are known as Universal Gates.

NOR

The declaration section of ABEL generally includes the device declaration, \_\_\_\_\_ declarations and set declarations.

Pin

An SOP expression having a domain of 2 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.

4

In the 32-bit Single Precision Floating formation, the exponent value \_\_\_\_\_ is reserved to represent 0 exponents.

0

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

Slow

The complement of a variable is always

The inverse of the variable

$A(B + C) = A.B + A.C$  is the expression of \_\_\_\_\_.

Distributive Law

If the number 2025 is represented in floating point, then exponent is \_\_\_\_\_.

3

Excess-8 code of -6 is \_\_\_\_\_.

0010

A 3-variable Karnaugh map has

Eight cells

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is \_\_\_\_\_ to the range of values that are to be represented.

Proportional

Suppose we want to transmit the data "10001101" and an "Even-Parity" bit scheme is used to detect errors, the parity bit added to the data will be \_\_\_\_\_.

Both "0" and "1" can be used

The carry propagation delay problem in parallel binary adder can be solved by \_\_\_\_\_.

Using two full adders

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a \_\_\_\_\_ multiplexer.

2-input, 8-bit

The octal equivalent of the following binary number is

\_\_\_\_\_.

**117**

A' is written is ABEL as \_\_\_\_\_.

**!A**

Which of the following is the hexadecimal equivalent of 28?

**1C**

High Level Noise Margins (VNH) of CMOS 5 volt series circuits is

\_\_\_\_\_.

**0.9 V**

Adjacent 1s detector circuit will have active high output for the input.

**0011**

Modern information techniques are relying more on \_\_\_\_\_ transmission.

**Digital**

The \_\_\_\_\_ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.

**Two**

How many data select lines are required for selecting eight inputs?

**3**

Select the mode of programming in which GAL 16V8 can be programmed.

All of the given option

\_\_\_\_\_ has the fastest switching speed and low power requirement.

Advanced low power Schottky

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_.

0.1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called \_\_\_\_ of the flip-flop.

Hold time

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

Each stage of Master-slave flip-flop works at \_\_\_\_ of the clock signal.

One half

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using \_\_\_\_

NOT

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is \_\_\_\_

1111

\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

Race condition

The Synchronous counters are also known as Ripple Counters: **False**

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the \_\_\_\_

**Set-up time**

The n flip-flops store \_\_\_\_ states.

**$2^n$**

When the \_\_\_\_ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of \_\_\_\_

**1,2**

A positive edge-triggered flip-flop changes its state when \_\_\_\_

**Low-to-high transition of clock**

A decade counter is \_\_\_\_

**Mod-10 counter**

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## Low-to-high transition of clock

A decade counter is \_\_\_\_

## Mod-10 counter

The look-ahead carry circuits \_\_\_\_\_

## Reduce propagation delay

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_ is added to the result

0110

Both the multiplexers are selected simultaneously when \_\_\_\_\_ is set to logic \_\_\_\_\_ in 2-inputs, 8-bit Multiplexer.

G, Low

Function labels required to represent the input/output combinations for each segment in 7-segment display

7

Multiplexers are also known as \_\_\_\_\_

Data selectors

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_

0, 1

Cin is part of \_\_\_\_\_ Adder.

Full

The look-ahead carry circuits \_\_\_\_\_

## Reduce propagation delay

Which of the following gates has the outputs 1 if and only if at least one input is 1?

OR

A sop expression can be implemented by on \_\_\_\_ combination of gates.

AND-OR

The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through \_\_\_ ALU units in 16-bit ALU.

**Four**

Digital circuits operates with \_\_\_\_\_ voltage value(s)

**2**

In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles \_\_\_\_\_

**Lower priority outputs**

To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_\_\_ variable Karnaugh maps are used.

**4**

The output of a NAND Gate is \_\_\_\_\_ when all the inputs are one.

**Zero**

The \_\_\_\_\_ is the slowest and consumes more power.

**Standard TTL**

The between expression  $X-AB+CD$  represents

**Two ANDs ORed together**

The expression  $F-A+B+C$  describes the operation of three bits \_\_\_\_\_ Gate.

**OR**

Which one of the following is NOT a valid rule of Boolean Algebra?

**$A=A'$**

A 5-Variable Karnaugh map has

**Thirty two cells**

\_\_\_\_\_ is invalid number of cells in a single group formed by the adjacent cells K-map

**12**

In 32-bit Single –Precision floating point format representation the range of exponent value is from \_\_\_\_\_ to \_\_\_\_\_

**+127 to -126**

\_\_\_\_\_ has the fastest switching speed and low power requirements

Advanced low power schottky

Which of the following is a volatile memory?

DRAM

---

\_\_\_\_\_ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

Combinational Input

The AND Gate performs a logical \_\_\_\_\_ function.

Division

The Adjacent 1s Detector accepts 4-bit inputs. If \_\_\_\_\_ adjacent 1s are detected in the input, the output is set to high.

1

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

The FAST Model Page Access allows \_\_\_\_\_ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a \_\_\_\_\_ with a \_\_\_\_\_.

row, column

Which of the following Output Equations determines the output of the State Machine?

**MAX = Q0Q1EN**

The maximum value, represented by a single hexadecimal digit is \_\_\_\_\_.

**"F"**

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a \_\_\_\_\_.

**1**

The Static Ram (SRAM) is non-volatile and is not a \_\_\_\_\_ density memory as a latch is required to store a single bit of information.

**High**

Demorgan's two theorems prove the equivalency of the NAND and \_\_\_\_\_ gates and the NOR and \_\_\_\_\_ gates respectively.

**Negative-OR, Negative-AND**

Two signals \_\_\_\_\_ and \_\_\_\_\_ provide the timing inputs to the State Machine.

**PTIME and QTIME**

The 74HC163 is a 4-bit Synchronous counter, it has \_\_\_\_\_ data output pins.

**4**

PLDs have In-System Programming (ISP) capability that allows the \_\_\_\_\_ to be programmed after they have been installed on a circuit board.

**PLDs**

The CONSTATE.CLK = Clock is used to indicate that the \_\_\_\_\_ state variables change on a clock transition.

**CONSTATE**

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using \_\_\_\_\_.

**Shift Registers**

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as \_\_\_\_\_ inputs.

**Synchronous**

For a down counter that counts from (111 to 000), if current state is "101" the next state will be \_\_\_\_\_.

**None of the given**

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

**XOR, NAND**

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to \_\_\_\_\_ location(s) using a single address.

**Four**

In NAND based S-R latch, output of each \_\_\_\_\_ gate is connected to the input of the other \_\_\_\_\_ gate.

**NAND, NAND**

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires \_\_\_\_\_ gates for the 8 product terms (minterms) with an 8-input OR gate.

**8 AND**

8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer.

**8-to-1**

The \_\_\_\_\_ input overrides the \_\_\_\_\_ input.

**Asynchronous, synchronous**

A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.

**AND-OR**

The 64-cell array organized as 8 x 8 cell array is considered as an 8 byte memory

The terminal count of a 4-bit binary counter in the UP mode is

\_\_\_\_\_.

**1100**

A 3-variable karnaugh map has

**eight cells**

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_.

**Q output of all flip-flops to clock input of next flip-flops**

Memory is arranged in \_\_\_\_\_.

**Two-dimensional manner**

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result.

**1001**

Subtractors also have output to check if 1 has been \_\_\_\_\_.

**Primed**

The Test Vector definition defines the test vectors for all the three counter inputs and \_\_\_\_\_ counter output/outputs.

**Three**

A multiplexer with a register circuit converts

**Parallel data to serial**

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

**True**

The n flip-flops store \_\_\_\_\_ states.

**$2^n$**

The S-R latch has two inputs, therefore \_\_\_\_\_ different combinations of inputs can be applied to control the operation of the S-R latch.

**four**

Why demultiplexer is called a data distributor?

**Single input to Single Output**

When the transmission line is idle in an asynchronous transmission

**It is set to logic high**

UVERPROM is stands for

**Ultra-Violet**

In memory write cycle, the time for which the WE signal remains active is known as the \_\_\_\_\_.

**Write pulse width**

The outputs of SR latches in elevator state machine are feed back to the \_\_\_\_\_ gate array for connection to the D-flipflops.

**AND**

PALs tend to execute \_\_\_\_\_ logic.

**SOP**

The ROM used by a computer is relatively \_\_\_\_\_ as it stores few buyers of code used to Boot the Computer system on power up.

**Small**

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration  $t_{WD}$ ?

**-WE**

You have to choose suitable option when your timer will reset by considering this given code:

```
TRSTATE.CLK = clk;
```

```
TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);
```

**NSY2 or EWY2**

A NOR based S-R latch is implemented using \_\_\_\_\_ gates instead of \_\_\_\_\_ gates.

**NOR, NAND**

Implementation of Latch is required almost \_\_\_\_\_ transistor.

**Six**

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in \_\_\_\_\_ when Distributed refresh is used.

**7.8 microsec**

The NOR logic gate is the same as the operation of the \_\_\_\_\_ gate with an inverter connected to the output.

**NAND**

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.

**1**

Select the mode of programming in which GAL16V8 can be programmed:

**All of the given**

Divide-by-32 counter can be achieved by using

**Flip-Flop and DIV 32**

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the \_\_\_\_\_ can be pressed at any time either on the first floor or the second floor in elevator.

**REQ1**

Consider  $A=1$ ,  $B=0$ ,  $C=1$ . A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be \_\_\_\_\_.

**One**

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

**1111**

Adding two octal numbers "36" and "71" result in \_\_\_\_\_.

**127**

The ABEL Input file can use a \_\_\_\_\_ instead of the equation to specify the Boolean expressions.

**Truth Table**

The domain of the expression  $AB'CD + AB' + C'D + B$  is

**A, B, C and D**

If the number of samples that are collected is reduced by half, the reconstructed signal will be \_\_\_\_\_ from/to the original.

**Same**

In DRAM read cycle R /W<sup>-</sup> signal is activated to read data which is made available on the \_\_\_\_\_ data line.

**D(OUT)**

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

**True**

Implementation of the FIFO buffer in \_\_\_\_\_ is usually takes the form of a circular buffer.

**RAM**

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack

\_\_\_\_\_.

**Top**

Which one flip-flop has an invalid output state?

**SR**

The output of a NAND gate is \_\_\_\_\_ when all the inputs are one.

**Zero**

The Transition table is very similar to the \_\_\_\_\_ table.

**State**

Consider the sum of weight method for converting decimal into binary value, \_\_\_\_\_ is the highest weight for 411.

**256**

Canonical form is a unique way of representing \_\_\_\_\_.

**SOP**

\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously.

**Synchronous**

Cin is part of \_\_\_\_\_ Adder.

**Full**

Flash memories Operation are classified into \_\_\_\_\_ different operation.

**Two**

A Product term is 0 when \_\_\_\_\_

**Any one literal is 0**

In 8-input multiplexer, the two outputs are connected through a/an \_\_\_\_\_ gate.

**OR**

\_\_\_\_\_ Device dissipate varying amount of power depending upon the frequency of operation.

**CMOS**

Boolean Addition operation is performed by a(an) \_\_\_\_\_ gate.

**OR**

A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.

**AND-OR**

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

**$(2^{64})-1$**

In 16-bit ALU, The G output is activated if the 4-bit unit generate a Carry \_\_\_\_ irrespective of Carry \_\_\_\_.

**Out, In**

A standard POS form has \_\_\_\_ terms that have all the variables in the domain of the expression.

**Sum**

In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles \_\_\_\_.

**Lower priority inputs**

Which of the following is the example of comparator?

**XNOR**

IN CMOS 5 Volt series, Input voltage of Logic high signal ( $V_{IH}$ ) with a ranges from \_\_\_\_ to \_\_\_\_ volts.

**3, 5, 5**

The Adjacent 1 S Detector accepts 4-bit input. If \_\_\_\_ adjacent 1S are detected in the input, the output is set to high.

**4**

De Morgan's two theorems prove the equivalency of the NAND and \_\_\_\_ gates and the NOR and \_\_\_\_ gates respectively.

**Negative-AND, Negative-OR**

Adding two octal numbers "36 and 71" result in \_\_\_\_.

**127**

Any of the \_\_\_\_ forms of the Karnaugh Map can be used to simplify Boolean expressions

**Four**

Quine-McCluskey and K-Map methods are used for \_\_\_\_\_ of Boolean expression.

**Simplification**

The number “1259” may belong to \_\_\_\_\_ number system.

**Decimal or Hexadecimal system**

The series of TTL chips are characterized by their\_\_\_\_\_.

**Switching Speed only**

All ABEL statements must end with\_\_\_\_\_.

**;**

In sequential circuit memory elements are connected with\_\_\_\_\_.

**Clock**

In the 32-bit Single Precision Floating Point format, the exponent value\_\_\_\_\_ is reserved to represent infinity exponents.

**255**

The \_\_\_\_\_ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

**PLA**

The limitation in implementation of parallel binary address is known as\_\_\_\_\_.

**Carry input**

The Gray code is different form the unsigned binary code because\_\_\_\_\_.

**Successive value of Gray code by only one bit**

Removing the NOT gate at the output of the NOR gate result in an\_\_\_\_\_.

**OR gate**

Portable devices that run on batteries use \_\_\_ circuit that have low power dissipation.

**Integrated**

The domain of the expression  $AB'CD+B$  is

**B only**

\_\_\_\_\_ is a single input gate

**OR**

To represent in digital value, the number of digit (0s and 1s) that represent a quantity is \_\_\_\_\_ to the range of values that are to be represented.

**Equal**

BCD code of 16 is\_\_\_\_\_.

**00010001**

To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_\_\_ variable Karnaugh Maps are used.

**3**

In Odd parity generator circuit which gate is used to detect parity errors?

**XOR**

A 3-variable Karnaugh map has

**Eight cells**

The measurable values generally change over a

**Continuous range**

\_\_\_\_\_ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.

**GAL**

When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?

**1001**

How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decoder?

**Three**

The simplified expression using either of the two K-maps are \_\_\_\_\_.

**Identical**

Which of the following expression in the product of sums form?

**AB+CD**

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

**Slow**

GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

**True**

High level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_

**0.9 V**

The output of the expression  $F=A+B+C$  will be Logic \_\_\_\_\_ when  $A=0, B=1, C=1$ . the symbol "+" here represents OR Gate

**One**

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be \_\_\_\_\_.

**SET**

3.3 v CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5 v CMOS series.

**Fast switching speeds, very low power dissipation (page61)**

The binary value “1010110” is equivalent to decimal \_\_\_\_\_

**86**

The \_\_\_\_\_ Encoder is used as a keypad encoder.

**Decimal-to-BCD Priority**

How many data select lines are required for selecting eight inputs?

**3**

The Quad Multiplexer has \_\_\_\_\_ outputs

**4**

Demultiplexer has

**Single input and multiple outputs.**

The expression \_\_\_\_\_ is an example of Commutative Law for Multiplication.

**AB=BA**

The look-ahead carry circuits \_\_\_\_\_

**Reduce propagation delay**

What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?

$B' + C'D' + CD$

2-input, 8-bit Multiplexer, by setting the S input to logic \_\_\_\_\_ the \_\_\_\_\_ inputs of both the multiplexers are selected.

High, B

The maximum decimal number that can be represented using the 64-bit unsigned representation \_\_\_\_\_

$(2^{64}) - 1$

When two or more products terms are assumed by Boolean addition, the result is a \_\_\_\_\_

SOP

Tri-State Buffer is a \_\_\_\_\_ gate with a control line that disconnects the \_\_\_\_\_

The 4-bits 2's complement representation of "7" is \_\_\_\_\_

1001

\_\_\_\_\_ and \_\_\_\_\_ are the steps of the Quine-McCluskey.

Find prime implicants and select minimal set of the prime implicants.

The binary number 1011,101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_\_ separated by a decimal point.

1011,101

Subtractors also have output to check if 1 has been \_\_\_\_\_

Borrowed

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

**Slow**

The \_\_\_\_\_ description is used to simulate the logic circuit and verify its operation.

**Test vector**

How many outputs can an integrated circuit comparator have?

**Three**

Which of the following is not the correct method of grouping?

**Diagonally**

The output of the expression  $F=A.B.C$  will be logic \_\_\_\_\_ when  $A=1, B=0, C=1$ .

**Zero**

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.

**AND, OR**

In the 32-bit Single Precision Floating point format, the exponent value \_\_\_\_\_ is reserved infinity exponent.

**99**

The Boolean expression  $(AB'CS')$  is used

**A product term**

The product of an XOR gate is zero(0), when \_\_\_\_\_ All the inputs are zero

**I and IV only**

\_\_\_\_\_ methods are used to Convert Decimal fractions to Binary.

2

To display the number\_\_\_\_ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

2

A SOP expression is equal to I \_\_\_\_\_

When one or more product terms in the expression are equal to 1

The output A B is set to I when the input combinations is

A=01, B=10

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

True

High level Noise Margins (V<sub>NH</sub>) of CMOS 5 volt series circuits is

\_\_\_\_\_

0.9 V

If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them into floating point representation and then multiplying them, the value of mantissa of result will be \_\_\_\_\_

24.582 (But not sure)

The output of the expression  $FA+B+C$  will be Logic \_\_\_\_\_ represents OR Gate.

10(binary)

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes too, the latch will be

**SET**

3.3 y CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5 y CMOS sense.

**Fast switchIn2 secedes. Very low lower dissolution Date 1**

The binary value "1010110" is equivalent to decimal \_\_\_\_\_

**86 (According to Formula)**

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 10

**Flip-Flop and DIV 16**

Flip-Flop and DIV 32

DIV 16 and DIV 32

The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)

(n raise to power 2)

(n raise to power 2 and then minus 1)

**(2 raise to power n)**

(2 raise to power n and then minus 1)

A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

**1001**

1011

0011  
1100

A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is \_\_\_\_\_

0001  
**1111**  
1000  
1110

Divide-by-160 counter is acheived by using

Flip-Flop and DIV 10  
Flip-Flop and DIV 16  
DIV 16 and DIV 32  
**DIV 16 and DIV 10**

A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.

3  
7  
**8**  
15

RCO stands for \_\_\_\_\_

Reconfiguration Counter Output  
Ripple Counter Output  
Reconfiguration Clock Output  
**Ripple Clock Output**

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

**Race condition**

Clock Skew  
Ripple Effect  
None of given options

For a down counter that counts from (111 to 000), if current state is "101" the next state will be \_\_\_\_\_

111  
110  
010  
**none of given options**

A Divide-by-20 counter can be achieved by using

**Flip-Flop and DIV 10**  
Flip-Flop and DIV 16  
Flip-Flop and DIV 32  
Div 10 and DIV 16

Ripple Clock Output

The 74HC163 is a 4-bit Synchronous Counter. it has.....data output pins

2  
4  
6  
8

\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously

**Asynchronous**

Synchronous

Positive-Edge triggered

Negative-Edge triggered

Q : A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.

3  
7  
8  
15

Q : Design of state diagram is one of many steps used to design

a clock

a truncated counter

an UP/DOWN counter

**any counter**

Q : A synchronous decade counter will have \_\_\_\_\_ flip-flops

3

4

7

10

Q : Karnaugh map is used in designing

a clock

a counter

an UP/DOWN counter

All of the above

Q : \_\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

Hold and Wait

Clock Skew

Race condition

Hold delay

Q : Three cascaded modulus-10 counters have an overall modulus of

30

100

1000

10000

Q : An Astablemultivibrator is known as a(n) \_\_\_\_\_

Oscillator

Booster

One-shot

Dual-shot

Q: \_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

**Clock Skew**

Ripple Effect

None of given options

Q: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_

Gated flip-flops

Pulse triggered flip-flops

Positive-Edge triggered flip-flops

**Negative-Edge triggered flip-flops**

Q: In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together

**True**

False

Quiz: A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must J and K be?

J = 1, K = 0

**J = 1, K = X (Don't care)**

J = X (Don't care), K = 0

J = 0, K = X (Don't care)

Q: The Synchronous counters are also known as Ripple Counters: :

True  
False

Q: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True  
False

Quiz: The terminal count of a 4-bit binary counter in the DOWN mode is \_\_\_\_\_

0000  
0011  
1100  
1111

Quiz: An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_

Q output of all flip-flops to clock input of next flip-flops  
**Q' output of all flip-flops to clock input of next flip-flops**  
Q output of all flip-flops to J input of next flip-flops  
Q' output of all flip-flops to K input of next flip-flops

the terminal count of a modulus-13 binary counter is

0000  
1111  
**1101**  
1100

Quiz: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

**True**  
False

Quiz: A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

**1001**  
1011  
0011  
1100

Quiz: Design of state diagram is one of many steps used to design

a clock  
a truncated counter  
an UP/DOWN counter  
**any counter**

Quiz: An Astable multivibrator is known as a(n) \_\_\_\_\_

**Oscillator**  
Booster  
One-shot  
Dual-shot

Quiz: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_

Gated flip-flops  
Pulse triggered flip-flops  
Positive-Edge triggered flip-flops  
**Negative-Edge triggered flip-flops**

Quiz: A decade counter is \_\_\_\_\_

Mod-3 counter

Mod-5 counter

Mod-8 counter

**Mod-10 counter**

The terminal count of a 4-bit binary counter in the DOWN mode is \_\_\_\_\_

**0000**

0011

1100

1111

The Synchronous counters are also known as Ripple Counters:

True

**False**

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

**Clock Skew**

Ripple Effect

None of given options

Divide-by-160 counter is achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16  
DIV 16 and DIV 32  
**DIV 16 and DIV 10**

Design of state diagram is one of many steps used to design

a clock  
a truncated counter  
an UP/DOWN counter  
**any counter**

In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is\_\_\_\_\_

0000  
**1111**  
0001  
10000

