MCQs DLD lec 23-33

Collected by HassanMalik

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

► True (Page 221)

► False

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

► Set-up time

► Hold time (Page 242)

► Pulse Interval time

► Pulse Stability time (PST)

74HC163 has two enable input pins which are _____ and _____

► ENP, ENT (Page 285)

► ENI, ENC

► ENP, ENC

► ENT, ENI

_____ is said to occur when multiple internal variables change due to change in one input variable

► Clock Skew

► Race condition (Page 267)

► Hold delay

► Hold and Wait

A decade counter is _____.

► Mod-3 counter

► Mod-5 counter

► Mod-8 counter

► Mod-10 counter (Page 274)

_____ is one of the examples of synchronous inputs.

► J-K input (Page 235)

► EN input

► Preset input (PRE)

► Clear Input (CLR)

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition

► Clock Skew (Page 226)

► Ripple Effect

► None of given options

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

► Doesn't have an invalid state (Page 232)

► Sets to clear when both J = 0 and K = 0

► It does not show transition on change in pulse

► It does not accept asynchronous inputs

A positive edge-triggered flip-flop changes its state when _____

► Low-to-high transition of clock (Page 228)

► High-to-low transition of clock

► Enable input (EN) is set

► Preset input (PRE) is set

A frequency counter _____

► Counts pulse width

► Counts no. of clock pulses in 1 second (Page 301)

► Counts high and low range of given clock pulse

► None of given options

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► Mod-6, Mod-10 (Page 229) rep

► Mod-50, Mod-10

► Mod-10, Mod-50

► Mod-50, Mod-6

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

► True (Page 221) rep

► False

Flip flops are also called _____

► Bi-stable dualvibrators

► Bi-stable transformer

► Bi-stable multivibrators (Page 228)

► Bi-stable singlevibrators

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

► Set-up time

► Hold time (Page 242) rep

► Pulse Interval time

► Pulse Stability time (PST)

74HC163 has two enable input pins which are _____ and _____

► ENP, ENT (Page 285)

► ENI, ENC

► ENP, ENC

► ENT, ENI

_____ is said to occur when multiple internal variables change due to change in one input variable

► Clock Skew

► Race condition (Page 267)

► Hold delay

► Hold and Wait

A decade counter is _____.

► Mod-3 counter

► Mod-5 counter Fileil

► Mod-8 counter

► Mod-10 counter (Page 274

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

► AND (Page 182)

► OR

► NOT

► XOR

_____ is one of the examples of synchronous inputs.

► J-K input (Page 235) rep

► EN input

► Preset input (PRE)

► Clear Input (CLR)

_____ is one of the examples of asynchronous inputs.

► J-K input

► S-R input

► D input

► Clear Input (CLR) (Page 235)

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition

► Clock Skew (Page 226) rep

► Ripple Effect

► None of given options

In a state diagram, the transition from a current state to the next state is determined by

► Current state and the inputs (Page 232)

► Current state and outputs

► Previous state and inputs

► Previous state and outputs

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

► Doesn't have an invalid state (Page 232) rep

► Sets to clear when both J = 0 and K = 0

► It does not show transition on change in pulse

► It does not accept asynchronous inputs

A positive edge-triggered flip-flop changes its state when _____

► Low-to-high transition of clock (Page 228) rep

► High-to-low transition of clock

► Enable input (EN) is set

► Preset input (PRE) is set

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW

► 25 mW (Page 242)

► 64 mW ► 1024

_____ counters as the name indicates are not triggered simultaneously. Fileil

► Asynchronous (Page 269)

► Synchronous

► Positive-Edge triggered

► Negative-Edge triggered

74HC163 has two enable input pins which are _____ and _____

► ENP, ENT (Page 285) rep

► ENI, ENC

► ENP, ENC

► ENT, ENI Question No: 11

(Marks: 1) - Please choose one

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► Mod-6, Mod-10 (Page 299)

► Mod-50, Mod-10

► Mod-10, Mod-50

► Mod-50, Mod-6

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

► set (Page 219)

► reset

► invalid

► clear

Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

►A parallel to serial converter circuit (Page 244)

►A counter circuit ►A BCD to Decimal decoder ►A 2-to-8 bit decoder

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

►0 ►1 (Page 230) ►Invalid ►Input is invalid

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop. ►Set-up time ►Hold time (Page 242) rep ►Pulse Interval time ►Pulse Stability time (PST

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

►Using S-R Flop-Flop ►D-flipflop ►J-K flip-flop (Page 252) ►T-Flip-Flop

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status. ►3 ►7 ►8 (Page 272) ►15

Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state ►Ten ►Eight ►Three ►Two (Page 262)

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay. ►Race condition ►Clock Skew (Page 226) rep ►Ripple Effect ►None of given options

Flip flops are also called _____

► Bi-stable dualvibrators ► Bi-stable transformer ► Bi-stable multivibrators (Page 228) rep ► Bi-stable singlevibrators

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

► 0 ► 1 ► Invalid (Page 230) ► Input is invalid

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____ ► Doesn't have an invalid state (Page 232) rep ► Sets to clear when both J = 0 and K = 0 ► It does not show transition on change in pulse ► It does not accept asynchronous inputs

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

► Set-up time ► Hold time (Page 242) ► Pulse Interval time ► Pulse Stability time (PST)

Question No: 13 (Marks: 1) - Please choose one We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

► Using S-R Flop-Flop ► D-flipflop ► J-K flip-flop (Page 252) ► T-Flip-Flop

Question No: 17 (Marks: 1) - Please choose one A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW ► 25 mW (Page 242) ► 64 mW ► 1024

Question No: 18 (Marks: 1) - Please choose one _____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition ► Clock Skew (Page 226) rep ► Ripple Effect ► None of given options

Question No: 19 (Marks: 1) - Please choose one A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

► 3 ► 7 ► 8 (Page 272) rep ► 15

Question No: 20 (Marks: 1) - Please choose one A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

► 10 Hz ► 50 Hz (Page 298) ► 100 Hz ► 500 Hz

A synchronous decade counter will have _____ flip-flops

► 3 ► 4 (Page 281) rep ► 7 ► 10