CS302 Final Term 50 MCQ's

Part # 01

1- The minimum time for which the Input signal has to be maintained at the Input of flip-flop is called ____. Pg 254

(a) set-up time
(b) hold time ✓
(c) pulse Interval time
(d) Pulse stability time (PST)

2- 74HC163 has two enable input pins which are ____ and ____. Pg 278

(a) ENP, ENT ✓
(b) ENI, ENC
(c) ENP, ENC
(d) ENT, ENI

(a) set-up time
(b) hold time
(c) pulse Interval time
(d) Pulse stability time (PST)

2- 74HC163 has two enable input pins which are ____ and ____. Pg 278

(a) ENP, ENT
(b) ENI, ENC
(c) ENP, ENC
(d) ENT, ENI

3- ____ is said to occur when multiple internal variables change due to change in one input variable. Pg 260

(a) clock strew
(b) Race condition
(c) Hold delay
(d) Hold and wait

4- The ____ and ____ input overrides the ____ input. Pg 362

(a) Asynchronous, synchronous
(b) Synchronous, asynchronous
(c) Preset input (PRE), clear input (CLR)
(d) clear input (CLR), Preset input (PRE)

change due to change in one input variable. Pg 260

ⓐ clock strew ⓒ Hold delay

ⓑ Race condition ⓓ Hold and wait

4- The ___ and ___ input overrides the ___ input. Pg 362

ⓐ Asynchronous, synchronous ⓒ Preset input (PRE), clear input (CLR)

ⓑ Synchronous, asynchronous ⓓ clear input (CLR), Preset input (PRE)

5- A decade counter is _____. Pg 267

ⓐ Mod-3 counter ⓒ Mod-8 counter

ⓑ Mod-5 counter ⓓ Mod-10 counter

Q2:

6- In asynchronous transmission when the Serial transmission line is idle, ___ no data is being transmitted (349 Pg)

ⓐ It is set to logic low ⓒ Remain in previous state

ⓑ It is set to logic high ⓓ Is not used to start transmission.

7- A 8-bit serial in/parallel out shift register contains the value

ⓑ Synchronous, asynchronous ⓓ clear input (CLR), Preset input (PRE)

5- A decade counter is _____. Pg 267

ⓐ Mod-3 counter ⓒ Mod-8 counter

ⓑ Mod-5 counter ⓓ Mod-10 counter

Q2:

6- In asynchronous transmission when the Serial transmission line is idle, _____ no data is being transmitted (349 pg)

ⓐ It is set to logic low ⓒ Remain in previous state

ⓑ It is set to logic high ⓓ Is not used to start transmission.

7- A 8-bit serial in/parallel out shift register contains the value "8" _____ clock signal(s) will be required to shift the value completely out of the register. not Sure

ⓐ 1 one ⓒ 4 four Read Page 341, 342, 343

ⓑ 2 two ⓓ 8 eight

8- In a sequential circuit the next state is determined by ____ and ____. 298

(a) state variable, current state (c) current state and external Input

(b) current state, flip-flop output (d) Input and clock signal applied

9- The divide-by-60 counter in digital clock is implemented by using two cascading counters:

(a) Mod-6, Mod-10 (c) Mod-10, Mod-50 292

(b) Mod-50, Mod-10 (d) Mod-50, Mod-6

10- Nibble consists of ___ bits.

(a) 2 (b) 4 (c) 8 (d) 16

10- Nibble consists of ___ bits. 387

(a) 2 (b) 4 (c) 8 (d) 16

11- Excess-8 code assign ___ to "-8"

(a) 1110 (b) 1100 (c) 1000 (d) 0000 Pg 34

12- The voltage gain of the Inverting Amplifier is given by the relation ___. Pg 439

(a) Vout/Vin = -Rf/Ri (c) Rf/Vin = -Ri/Vout

(b) Vout/Rf = -Vin/Ri (d) Rf/Vin = Ri/Vout

13- LUT is acronym for ___ 432

(a) Look Up Table (c) Least Upper Time Period

(b) Local User Terminal (d) None of the given

(a) Look Up Table
(b) Local User Terminal
(c) Least Upper Time Period
(d) None of the given

14- The three fundamental gates are _____.

(a) AND, NAND, XOR
(b) OR, AND, NAND
(c) NOT, NOR, XOR
(d) NOT, OR, AND

15- The total amount of memory that is supported by any digital system depends upon _____.

(a) The organization of memory
(b) The structure of memory
(c) The size of decoding unit
(d) The size of the address bus of the microprocessor or the micro-controller.

* The normal data inputs to flip-flop (D, S and R, or J and k) are reffered to as synchronous inputs.

* Because they have an effect on the outputs (Q and $\overline{Q}$) only in step...

Internet

16- _____ is one of the examples of synchronous in

ⓐ J-k input

ⓑ EN input

ⓒ Preset Input (PRE)

ⓓ Clear Input (CLR)

17- _____ occur when the sa clock signal arrives

16- _____ is one of the examples of synchronous inputs.

(a) J-k input
(b) EN input
(c) Preset Input (PRE)
(d) Clear Input (CLR)

17- _____ occur when the same clock signal arrives at different times at different clock inputs due to propagation delay.

(a) Race Condition
(b) Ripple Effect
(c) Clock Strew
(d) None of the given

18- _____ is used to simplify the circuit that determines the next state.

(a) State diagram
(b) Next state table
(c) State reduction
(d) State assignment

the next state.

(a) State diagram
(b) Next state table
(c) State reduction
(d) State assignment

19- The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop ——.

(a) Doesn't have an ~~indivi~~ invalid state
(b) Sets to clear when both J=0 and K=0
(c) It does not show transition on change in pulse
(d) It does not accept asynchronous inputs.

20- A multiplexer with a register circuit converts ——

(a) Serial data to parallel
(b) Parallel data to Serial
(c) Serial data to serial
(d) Parallel data to Parallel

ⓓ It does not accept asynchronous inputs.

20- A multiplexer with a register circuit converts ____

ⓐ Serial data to parallel ⓒ Serial data to serial

ⓑ Parallel data to Serial ⓓ Parallel data to Parallel

21- GAL is essentially a ____.

ⓐ Non-reprogrammable PAL ⓒ Reprogrammable PAL

ⓑ Very large PAL ⓓ PAL that is programmed only by manufacturer

22- In ____, all the columns in the same row are either read or written.

ⓐ Sequential Access ⓒ Fast Mode Page Access

ⓑ MOS Access ⓓ None of the given

23- A flip-flop changes its state when _____.

(a) Low-to-high transition of clock (c) Enable Input (EN) is set

(b) High-to-low transition of clock (d) Preset Input (PRE) is set

24- A frequency counter _____.

(a) counts pulse width (d) none of the given

(b) counts no. of clock pulses in 1 sec 294

(c) counts high and low range of given clock pulse

25- In a sequential circuit the next state is determined by _____ and _____.

(a) state variable, current state (c) Current state and external Input

(b) counts no. of clock pulses in 1 sec

(c) counts high and low range of given clock pulse

25- In a sequential circuit the next state is determined by ____ and ____.

(a) state variable, current state
(b) current state, flip-flop output
(c) Current state and external Input
(d) Input and clock signal applied

26- Flip-flop are also called ____.

(a) Bi-stable dualvibrators
(b) Bi-stable transformer
(c) Bi-stable multivibrators
(d) Bi-stable singlevibrators

(a) I (b) O (c) A (d) A

28- DRAM stands for _____.

(a) Dynamic RAM (c) Demoduler RAM

(b) Data RAM (d) None of the given

29- _____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

(a) Resolution (c) Quantization

(b) Accuracy (d) Missing Code

30- A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is _____.

(a) 10 mW (b) 25 mW (c) 64 mW (d) 1024

2.55

31- _____ counters are as the name indicates are not triggered simultaneously.

31- ____ counters are as the name indicates are not triggered simultaneously.

ⓐ Asynchronous ⓒ Positive-Edge triggered

ⓑ Synchronous ⓓ Negative-Edge triggered

32- For a positive edge-triggered J-K flip-flop with both J and K High, the outputs will ____ if clock goes High.

ⓐ toggle ⓑ set ⓒ reset ⓓ not change

33- If an S-R latch has a 1 on the S input and a 0 on the R input and then S input goes to 0, the latch will:

ⓐ set ⓑ reset ⓒ Invalid ⓓ clear

34- If S=1 and R=0, then Q(t+1) = ____ for +ve edge triggered flip-flop.

(a)

(b) 1

(d) Input is Invalid

35- Implementation of Latch is required almost ____ transistor

(a) Six

(b) Seven

(c) two 417

(d)

36- When both the Inputs of edge-triggered J-K flip-flop are set to logic zero ____ Pg 337

(a) The flip-flop is triggered

(b) $Q=0$ and $Q'=1$

(c) $Q=1$ and $Q'=0$

(d) The output of flip-flop remains unchanged.

37- If the FIFO memory output is already filled with data then _____. Reading Pg (418) — (420)

(a) It is locked ; no data is allowed to enter.

(b) It is not locked ; the new data overwrites the previous data.

(c) Previous data is swapped out of memory and new data enters

(d) None of the given options.

38- In _____ (a) output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

(a) moore machine

(b) mealy machine

(c) Johnson counter

(d) Ring counter

flip-flop of the shift register.

(a) moore machine
(b) mealy machine
(c) Johnson counter
(d) Ring counter

39- A multiplexer with a register circuit converts ____.

(a) serial data to parallel
(b) Parallel data to serial
(c) Serial data to serial
(d) Parallel data to parallel

40- In ____ outputs depend only on the current state.

(a) Mealy machine
(b) moore machine
(c) state reduction table
(d) state assignment table

41- The design and Implementation of synchronous ...ter starts from ____.

(a) Truth table
(b) K-map
(c) state table
(d) state diagram.

41- The design and Implementation of synchronous counter starts from ____. pg 312

(a) Truth table
(b) K-map
(c) state table
(d) state diagram.

42- The Glitches due to race condition can be avoided by using a ____. 260

(a) Gated flip-flop
(b) +ve-edge triggered flip-flop
(c) Pulse triggered flip-flop
(d) -ve-edge triggered flip-flop

43- A positive edge triggered flip-flop changes its state when ____.

(a) Low-to-high transition of clock
(b) High-to-low transition of clock
(c) Enable Input (EN) is set
(d) Preset Input (PRE) is

44- A particular half adder has _____.

(a) 2 inputs and 1 output (c) 3 inputs and 1 output

(b) 2 inputs and 2 outputs (d) 3 inputs and 2 outputs

45- NOR gate is formed by connecting _____.

(a) OR gate and then NOT gate (c) AND gate and then OR gate

(b) NOT gate and then OR gate (d) AND gate and then NOR gate

46- The sequence of states that are implemented by a n-bit Johnson counter is _____.

(a) n+2 (c) n 2

(b) 2n (n multiplied by 2) (d) 2^n

47- FIFO is an acronym for _____.

47- FIFO is an abbreviation for

(a) First In, First Out
(b) Fly In, Fly Out
(c) Fast In, Fast Out
(d) None of the given

48- The smallest unit of binary data is a ____

(a) Nibble
(b) Byte
(c) Bit
(d) Word

49- In asynchronous digital system all the circuits change their state with respect to a common clock.

(a) True
(b) False

50- ____ is one of the examples of asynchronous inputs.

(a) J-K Inputs
(b) S-R Inputs
(c) D inputs
(d) Clear Inputs (CLR)

Best of luck for your exams

387
288
238, 292, 309, 362, 365

(a) True (b) False 288

50- ____ is one of the examples of asynchronous inputs.

(a) J-K Inputs (c) D inputs 238, 292, 309, 342, 3

(b) S-R Inputs (d) Clear Inputs (CLR)

CS302 Final term

Preparation ; Part # 02

51- Bi-Stable devices remain in either of their ___ states unless the Inputs force the device to switch its state.

(a) Ten (b) Eight (c) Three (d) Two Pg 255

52- RCO stands for _____. Pg 278

(a) Reconfiguration counter output
(b) Reconfiguration clock output
(c) Ripple counter output
(d) ✓ Ripple clock output

53- The ___ Encoder is used as a keypad encoder

(a) 2-to-8 encoder
(b) 4-to-816 encoder
(c) BCD-to-Decimal
(d) ✓ Decimal-to-BCD Priority

Pg 166

(a) 2-to-8 encoder
(b) 4-to-8|16 encoder
(c) BCD-to-Decimal
(d) Decimal-to-BCD Priority

Pg 16

54- 3-to-8 Decoder can be used to Implement Standard SOP and POS Boolean expression.

(a) True
(b) False

Pg 161

55- The process of converting the analogue signal into a digital representation (code) is known as

(a) Strobing
(b) Amplification
(c) Quantization
(d) Digitization

Pg 438

56- The high density FLASH memory cell is implemented using _____. Pg 412

(a) 1 floating-gate MOS transistor (c) 4 floating-gate MOS tran
(b) 2 floating-gate MOS transistor (d) 6 floating-gate MOS tran

57- The ___ input overrides the ___ input Pg 362

(a) Asynchronous, synchronous
(b) Synchronous, asynchronou
(c) Preset Input, Clear Input
(d) Clear Input, Preset Inpu

58- Z Pin 20 ISTYPE "reg.invert"; The keyword "reg.invert" indicates _____. Pg 353

(a) An Inverted registor input
(b) An Inverted registor Input at pin 20
(c) Actice high registor Mode output
(d) ✓ Active-Low Registor Mode output.

59- The ABEL symbol for "OR" operation is _____.

(a) ! (b) ✓ # (c) $ (d) + Pg 203

60- The capability that allows the PLDs to be

59- The ABEL symbol for "OR" operation is ——.

(a) ! (b) # (c) $ (d) + Pg 203

60- The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called ——. Pg 194

(a) In-System Programming (b) In-Chip Programming (ICP)

61- The —— of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input

lines.)

Pg 410

(a) Write time (b) Recycle time (c) Refresh time (d) Access time

62- A divide-by-50 counter divides the Input ____ signal to a 1 Hz signal.

Pg 291

(a) 10 Hz (b) 50 Hz (c) 100 Hz (d) 500 Hz

63- A counter is implemented using three (3) flip-flop, possibly it will have ____ maximum output status.

(a) 3
(b) 7
(c) 8
(d) 15

$2^3 = 8$

Pg 265

64- Demultiplexer converts ___ data to ___ data.

(a) parallel data, serial data

(b) serial data, parallel data

(c) encoded data, decoded data

(d) All of the given options.

Pg 178

65- When the control line in tri-state buffer is high the buffer operates like a ___ gate.

(a) AND (b) OR (c) NOT (d) XOR

Pg 196

66- NOR Gate can be used to perform the operation of AND, OR and NOT Gate.

(a) True (b) False Pg 50

67- If an S-R latch has a 1 on the S input and then the S input goes to 0, then latch will be ---

(a) set (b) reset (c) Invalid (d) Clear # not Sure #

68- a positive edge-triggered

68- For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will ____ if the clock goes HIGH. Pg 227

(a) toggle (b) set (c) reset (d) not change

69- ____ is used to minimize the possible no. of states of a circuit. Pg 330

(a) state assignment (b) state reduction

(c) next state table (d) state diagram

* Reading must (Exam day) * Read every line like a Question.

70- A negative edge-triggered flip-flop changes its state when ------.

Pg 221

(a) Preset input (PRE) is set

(b) ✓ High-to-low transition of clock

(c) Enable input (EN) is set

(d) Low-to-high transition of cloc

71- For a down counter that counts from (111 to 000). If current state is "101" the next state will ___

(a) 010 (b) 111 (c) 110 (d) none of these Pg 302

72- In mealy machine the output depends on ___

(a) the input (c) the current state Pg 311

(b) current state and input (d) none of these

73- T... terminal count of a 4-bit binary counter in

(a) the input
(b) current state and input
(c) the current state Pg 311
(d) none of these

73- The terminal count of a 4-bit binary counter in the up mode is _____. Internet

(a) 0011 (b) 0000 (c) 1100 (d) 1111 ✓

74- Two states are said to be equal if they have exactly same _____. Pg 325

(a) next state
(b) none of these
(c) inputs ✓
(d) outputs

75- In case of cascading integrated circuit counters the enable inputs and RCO of the integrated circuit counters allow cascading of multiple counters together.)

Pg 279

(a) True (b) False

76- When the transmission line is idle in an asynchronous transmission. Pg 349

(a) It is set to logic low

(b) It is set to logic high

(c) ✓ state of transmission line is not used to state transmission

(d) It remains in previous states.

77- A synchronous decade counter will have ___ flip-flops.

(a) 7 (b) 4 (c) 10 (d) 3 Pg 267

78- To Implement the counter using S-R flip-flops instead of J-K flip-flops the ___ transition table is used. Pg 316

(a) S-R (c) none of these

(b) next state (d) J-K

78- To Implement the counter using S-R flip-flops instead of J-K flip-flops the _____ transition table is used. Pg 316

(a) S-R
(b) next state
(c) none of these
(d) J-K

79- The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop. Pg 254

(a) Pulse stability time (PST)
(b) Hold time
(c) Setup time
(d) Pulse interval time

80- In Asynchronous digital systems all the circuits change their state with respect to common clock.

(a) True (b) False Pg 238

81- In gated SR latch, what is the value of the output if EN = 1 , S = 0 , R = 1 ? Pg 219

(a) 1 (b) Q_t (c) invalid (d) 0

Input		output
EN	S	$Q_t + 1$
0	x	Q_t
1	0	Q_t

81- In gated SR latch, what is the value of the output if EN = 1 , S = 0 , R = 1 ? Pg 219

ⓐ 1 ⓑ Q_t ⓒ invalid ✓ ⓓ 0

	Input			output
	EN	S	R	$Q_t + 1$
	0	x	x	Q_t
	1	0	0	Q_t
	1	0	1	0 ✓
	1	1	0	1
	1	1	1	Invalid

82- Demultiplexer is also called Data distributor Pg 178

83- Stack is an ~~an~~ acronym for _____ Internet

(a) FIFO memory (c) Flash memory

(b) ✓ LIFO memory (d) Bust Flash memory

84- _____ is said to be occur when multiple interva variables change due to change in one input variable

(a) clock skew (c) Hold delay Pg 260

(b) ✓ Race condition (d) Hold and wait

85- LUT is an acronym for _____.

(a) ✓ Look Up Table (c) Least Upper Time Period

(a) Look Up Table (c) Least Upper Time Period

(b) Local User Terminal (d) None of these

86- A declaration section of ABEL generally includes the device declaration, ___ declaration and set declarations.

(a) model (c) system Pg 207

(b) pin (d) cell

87- The power consumed by a flip-flop is defined by —

(a) $P = M_{cc} \times V_{cc}$

(c) $P = V_{cc} \times I_{cc}$ Pg 235

(b) $P = I_{cc} \times R_{cc}$

(d) $P = V_{cc} \times R_{cc}$

88- Flip-Flop are also called _____. Pg 221

(a) Bi-stable multivibrator

(b) Bi-stable dualvibrator

(c) Bi-stable singlvibrator (d) Bi-stable transformer

89 A decade counter is _____.

(a) Mod-10 counter (b) Mod-5 counter

(c) Mod-3 counter (d) Mod-8 counter

90- A ____ can not operate without memory element.

(a) cell (b) unit (c) clock (d) counter Pg 387

* Sequential Circuit *

91- A mono-stable device only has a single stable state.

(a) False (b) True Pg 255

91- A mono-stable device only has a single stable state.

(a) False (b) True

Pg 255

92- A PLA consists of a ___ AND array and a ___ OR array.

Pg 182

(a) Fixed, Fixed (c) Programmable, Programmable

(b) Fixed, Programmable (d) Programmable, Fixed

(a) Fixed, Fixed
(b) Fixed, Programmable (d) Programmable, Fixed

93- The decimal-to-BCD encoder has _____ outputs.
(a) 10 (b) 16 (c) 4 (d) 2 Pg 166

94- GAL is an acronym for _____. Pg 183
(a) Gaint array logic (b) General array logic (c) Generic array logic

CS302 FT Preparation

95- Data is also handled in a 4-bit unit called
(a) nibble (b) memory (c) none of these. Pg 387

96- Sequential circuits can not operate without a _____ element. Pg 387
(a) memory element (b) Nibble element (c) None

97- Each storage element of a memory can either store a logic 0 or logic 1 and is called ____ Pg 387

(a) register (b) cell (c) flip-flop (d) all of these

98- The memory array can be organized in several ways depending on the ___ of data. Pg 387

(a) size (b) unit (c) reference (d) place

99- The 64-cell array organized as ___ cell array is considered as an 8-byte memory.

(a) 60+4 (b) 8x8 (c) 2x32 (d) all are allowed

100- The CONSTATE.CLK = Clock is used to indicate tha the ___ state variables change on a clock transition.

(a) CONSTATE (b) OPEN (c) MOTION (d) FLOOR Pg 373

101
92- The combinational digital circuits have ? storage element therefore combinational circuits handle only instantaneous inputs.

Pg 210

(a) two (c) one

(b) no (d) three

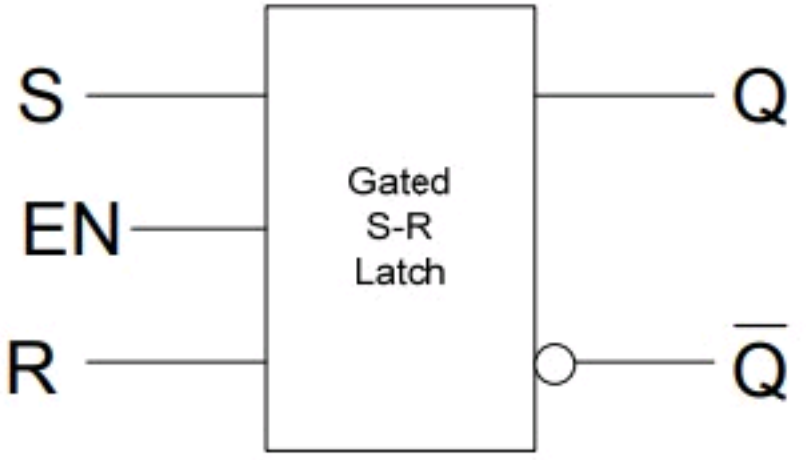


Figure 23.3 Logic Symbol of a Gated S-R Latch

Input			Output
EN	S	R	Q_{t+1}
0	x	x	Q_t
1	0	0	Q_t
1	0	1	0
1	1	0	1
1	1	1	invalid

Table 23.1 Truth-Table of a gated S-R Latch

CS302 - Digital Logic Design (Semester Quiz # 03 – (Graded))

Question # 2 of 10 (Start time: 10:06:45 AM, 26 June 2024)

In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

Select the correct option

- ○ Qt
- ◉ 0
- ○ 1
- ○ Invalid

Figure 31.1 Implementation of the Sequential Circuit

The 3-bit up counter can be implemented using S-R flip-flops and D flip-flops. Implementation of the counter using S-R flip-flop requires the use of S-R flip-flop transition table in step 3. The remaining steps follow step 3.

S-R flip-flop based Implementation

Flip-Flop Transition Table

To implement the counter using S-R flip-flops instead of J-K flip-flops, the S-R transition table is used. The S-R flip-flop does not allow S and R inputs to be set to logic 1 and 1 respectively and is considered to be an invalid state. Based on the three set of valid inputs the S-R transition table is shown. Table 31.5

Flip-flop Inputs		Output Transitions	
S	R	Q_t	Q_{t+1}
0	x	0	0
1	0	0	1
0	1	1	0
x	0	1	1

Table 31.5 S-R flip-flop Transition table

CS302 - Digital Logic Design (Semester Quiz # 03 – (Graded))

Question # 3 of 10 (Start time: 10:07:19 AM, 26 June 2024)

To implement the counter using S-R flip-flops instead of J-K flip-flops, the _____ transition table is used.

Select the correct option

- ○ None of above
- ○ Next State
- ◉ S-R
- ○ J-K

Lesson No. 31

2. NEXT-STATE TABLE

Once the state diagram of the sequential circuit is defined, a Next-State Table is derived which lists each present state and the corresponding next state. The next state is the state to which the sequential circuit switches when a clock transition occurs. Table 31.1

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Table 31.1 Next-State Table for a 3-bit Up-Counter

CS302 - Digital Logic Design (Semester Quiz # 03 – (Graded))

Question # 4 of 10 (Start time: 10:07:48 AM, 26 June 2024)

Once the state diagram is drawn for any sequential circuit the next step is to draw

Select the correct option

- ○ Logic expression
- ○ Karnaugh map
- ◉ Next-state table
- ○ Transiation table

One-Shot Mono-stable multi-vibrator

Bi-stable devices remain in either of their two states unless the inputs force the device to switch its state. The device remains in its alternate state unless the inputs are changed again to force the device back to its original state. A mono-stable device only has a single stable state and it remains in its stable state. It temporarily changes to its unstable state when it is triggered. It remains in its unstable state for a predetermined length of time and then it automatically switches back to its stable state. The length of time for which the device remains in the unstable state is determined by the time constant determined by the Resistor and Capacitor connected externally to the mon-stable device. The output of the device is a pulse having a time duration determined by R and C. These mono-stable devices are also known as One-Shots. Figure 25.9. One-Shots are of two types, the nonretriggerable and retriggerable.

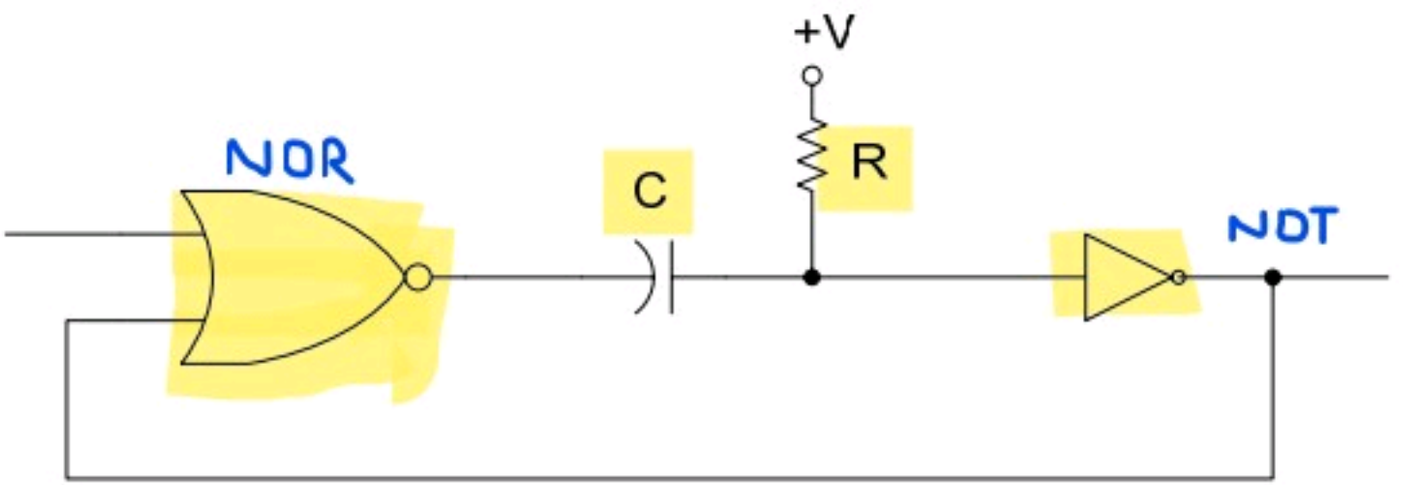


Figure 25.9a Circuit diagram of a One-Shot

CS302 - Digital Logic Design (Semester Quiz # 03 – (Graded))

Question # 5 of 10 (Start time: 10:08:12 AM, 26 June 2024)

A one-shot mono-stable device contains _____

Select the correct option

- ○ XNOR gate, Resistor, Capacitor and NOT Gate
- ○ AND gate, Resistor, Capacitor and NOT Gate
- ◉ NOR gate, Resistor, Capacitor and NOT Gate ✓
- ○ NAND gate, Resistor, Capacitor and NOT Gate

Sequential Circuits

The combinational digital circuits have no storage element; therefore combinational circuits handle only instantaneous inputs. The outputs of the combinational circuits also can not be stored. The absence of a memory element restricts the use of digital combinational circuits to certain application areas. The use of a memory element which is capable of storing digital inputs and outputs is an important part of all practical digital circuits.

Consider an ALU which performs Arithmetic and Logical operations. An ALU can not perform its operations unless it is connected to memory elements that store the inputs applied at the inputs of the ALU and outputs from the ALU. Consider an ALU that performs addition operation on a set of numbers, 2, 3, 4 and 5. The ALU can add two numbers at a time;

CS302 - Digital Logic Design (Semester Quiz # 03 – (Graded))

Question # 10 of 10 (Start time: 10:10:27 AM, 26 June 2024)

The combinational digital circuits have _____ storage element; therefore combinational circuits handle only instantaneous inputs.

Select the correct option

- ○ two
- ○ one
- ○ no
- ○ three

CS302 - Digital Logic Design (Semester Quiz # 03 – (Graded))

Question # 8 of 10 (Start time: 10:09:43 AM, 26 June 2024)

the terminal count of a modulus-13 binary counter is

Select the correct option

- 0000
- 1100
- 1101
- 1111

4. Propagtaion Delay t_{PHL} measured with respect to the leading edge of the clear input to the high-to-low transition of the output. Figure 23.16. On a high-to-low transition of the clear signal the flip-flop changes its output state to logic low. The Propagation Delay is measured at 50% transition mark on the triggering edge of the clear signal and the 50% mark on the high-to-low transition of the output that occurs due to the preset signal.

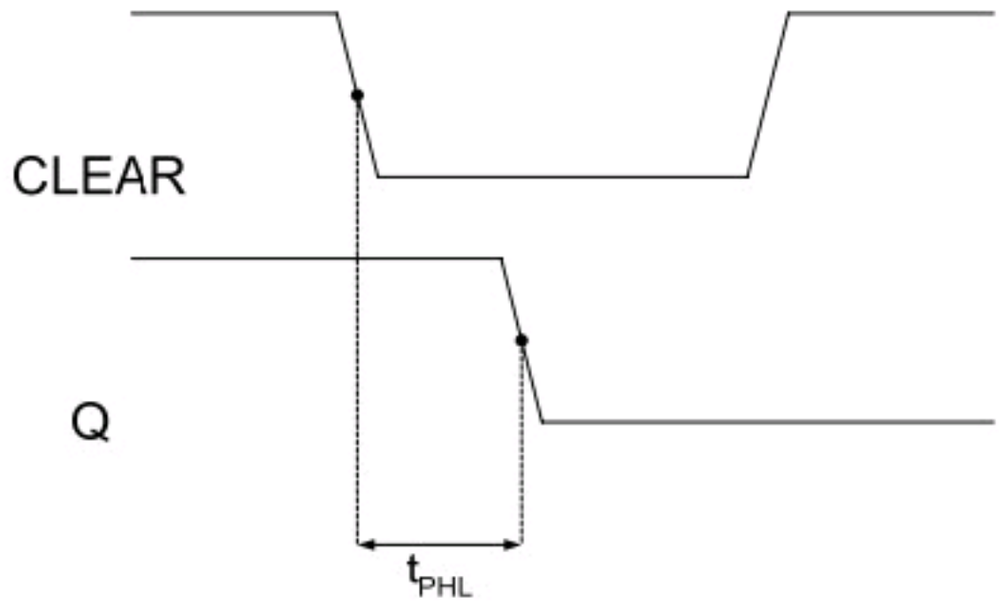


Figure 23.16 Propagation Delay, clear to high-to-low transition of the output

Set-up Time

When a clock transition occurs at the clock input of a flip-flop the output of the flip-flop is set to a new state based on the inputs. For the flip-flop to change its output to a new state at the clock transition, the input should be stable. The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the Set-up time. Figure 23.17.

CS302 - Digital Logic Design (Semester Quiz # 03 – (Graded))

Question # 9 of 10 (Start time: 10:10:05 AM, 26 June 2024)

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _____

Select the correct option

- ○ Pulse Interval time
- ○ Set-up time
- ○ Hold time
- ○ Pulse Stability time (PST)

Traffic Signal Controller Inputs and Outputs

The State Machine which controls the Traffic Signal has several inputs and outputs. The inputs are the

- NSSR: The NSSR is activated when a car is over either of the four sensors on the North-South section of the road
- EWSR: The EWSR is activated when a car is over either of the four sensors on the East-West section of the road

  A Timer is used to count the 5 minute and 1 minute traffic signal cycle during the day and night. Two signals LTIME and STIME provide the timing inputs to the State Machine.
- LTIME: The LTIME signal is activated if 5 minutes have elapsed; the signal remains active unless the timer is reset.
- STIME: The STIME signal is activated if 1 minute has elapsed; the signal remains active unless the timer is reset.

The outputs of the State Machine are

- NSGrn: The Green signal controlling the traffic on the North-South section
- NSYel: The Yellow signal controlling the traffic on the North-South section

- NSRed: The Red signal controlling the traffic on the North-South section
- EWGrn: The Green signal controlling the traffic on the East-West section
- EWYel: The Yellow signal controlling the traffic on the East-West section
- EWRed: The Red signal controlling the traffic on the East-West section
- TMRST: The Reset signal which resets the timer after the LTIME or the STIME signals are activated to indicate a time interval of 5 and 1 minutes respectively.

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 1 of 10 (Start time: 11:47:56 PM, 03 July 2024)

_____ Yellow signal controlling the traffic on the East-West section.

Select the correct option

- EWYel
- NSYel
- EWRed
- NSGrn

Mealy Machine
State Diagram

The sequential circuit represented earlier as a Moore Machine is described as a Mealy Machine. Figure 33.3. The output of a Mealy machine depends upon the present state at the inputs. The state diagram shows the six states. When the input is 1, the machine switches from its present state to the next. If the input is 0, the machine remains in its present state. The outputs of the machine when it switches to the next state or it remains the present state are shown with the directed arrows. For, example at state 'a', when the input is 1 the machine changes to the next state and the output is set to 111. When the input is set at 0, the machine remains in its current state with outputs 011.

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 2 of 10 (Start time: 11:48:32 PM, 03 July 2024)

According to Moore circuit, the output of synchronous sequential circuit depend/s on _____ of flip flop.

Select the correct option

- ○ Present State
- ○ External Inputs
- ◉ Next State
- ○ Previous State

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 3 of 10 (Start time: 11:48:58 PM, 03 July 2024)

Once the state diagram is drawn for any sequential circuit the next step is to draw

Select the correct option

- ○ Karnaugh map
- ◉ Next-state table
- ○ Logic expression
- ○ Transiation table

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 4 of 10 (Start time: 11:49:17 PM, 03 July 2024)

The n flip-flops store _____ states.

Select the correct option

○	0
○	2^(n+1)
◉	2^n
○	1

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 5 of 10 (Start time: 11:49:34 PM, 03 July 2024)

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and K be?

Select the correct option

- ○ J = X(Don't care), K = 0
- ○ J = 1, K = X(Don't care)
- ○ J = 0, K = X(Don't care)
- ○ J = 1, K = 0 ✓

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 6 of 10 (Start time: 11:50:16 PM, 03 July 2024)

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

Select the correct option

- ○ 80 mili seconds
- ● 80 micro seconds
- ○ 8 micro seconds
- ○ 10 micro seconds

The Transition table is very similar to the State table. The state table can be derived from the Transition table by assigning State Names to each State and including the output of the State Machine. The output of the State Machine is determined by the Output Equation

$$MAX = Q_0 Q_1 EN$$

The State Table for a Mealy Machine is given. Table 38.8. The Transition Table represents the function of the Mealy State Machine which is a 2-bit Counter. The Counter doesn't count when the input ENABLE=0 and increments when input ENABLE=1. The output MAX of the State Machine is dependent upon the current state and the Input ENABLE. The State Diagrams for the Mealy State machine derived from the State Table is shown. Figure 38.4.

Present State	Next State ENABLE=0	Next State ENABLE=1	Output MAX ENABLE=0	Output MAX ENABLE=1
A	A	B	0	0
B	B	C	0	0
C	C	D	0	0
D	D	A	0	1

Table 38.8 State table of a Mealy Machine

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 7 of 10 (Start time: 11:50:57 PM, 03 July 2024)

Which of the following Output Equations determines the output of the State Machine?

Select the correct option

- MAX = Q0Q1EN
- MIN = Q0Q1
- MIN = Q0Q1EN
- MAX = Q1EN

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 8 of 10 (Start time: 11:52:11 PM, 03 July 2024)

The characteristic equation of D-flip-flop implies that _____.

Select the correct option

- ◯ The next state is independent of present state ✓
- ◯ The next state is dependent on previous state
- ◯ The next state is independent of inputs

The ABEL Input file for Elevator State Machine

The main declaration and definition sections of the ABEL input file for the Elevator State Machine are described. Table 36.4.

The SR1, SR1_, SR2, SR2_ variables are the S-R latch Q and $\overline{Q}$ outputs for latches SR1 and SR2. These latches are implemented using the AND-OR gates of the PLD device, there outputs are available at the output pins 16, 17, 18 and 19 of the GAL16V8 device. These outputs are generated by combinational circuits therefore these outputs are defined as ISTYPE 'com.buffer'. These outputs are feed back to the AND gate array for connection to the D flip-flops. The outputs from the three D flip-flops, DOOR, MOTION and DIR are declared as ISTYPE 'reg.buffer' as these three outputs are the outputs of the sequential circuit D flip-flops in the OLMC modules. Table 36.4a.

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 9 of 10 (Start time: 11:52:36 PM, 03 July 2024)

The outputs of SR latches in elevator state machine are generated by combinational circuits therefore, these outputs are defined as ISTYPE '_____'.

Select the correct option

- reg.buffer
- com.org
- com.reg
- com.buffer

CS302 - Digital Logic Design (Semester Quiz # 04 – (Graded))

Question # 10 of 10 (Start time: 11:53:00 PM, 03 July 2024)

A divide-by-10 Johnson counter requires

Select the correct option

○	twelve flip-flops
✗	four flip-flops
○	five flip-flops
✓	ten flip-flops

CS302 - Digital Logic Design (Semester Quiz # 03 – (Graded))

Question # 7 of 10 (Start time: 10:09:22 AM, 26 June 2024)

A divide-by-10 ring counter requires a minimum of

Select the correct option

- four flip-flops
- ten flip-flops
- twelve flip-flops
- five flip-flops ✓

Shift Register Counters

Shift register counters are basically, shift registers connected to perform rotate left and rotate right operations. When data is rotated through a register counter a specific sequence of states is repeated. Two commonly used register counters in digital logic are the Johnson Counter and the Ring Counter.

1. Johnson Counter

In a Johnson counter, the $\overline{Q}$ output of the last flip-flop of the shift register is connected to the data input of the first flip-flop. The circuit of a 4-bit, D flip-flop based Johnson Counter is shown in figure 34.16. The sequence of states that are implemented by a n-bit Johnson counter are 2n. Thus a 4-bit Johnson counter sequences through 8 states and a 5-bit Johnson counter sequences through 10 states. Table 34.1

2. Ring Counter

The Ring Counter is similar to the Johnson counter, except that the Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register. All the flip-flops of the counter are cleared to logic low except for the first flip-flop which is preset to logic high. Figure 34.17.

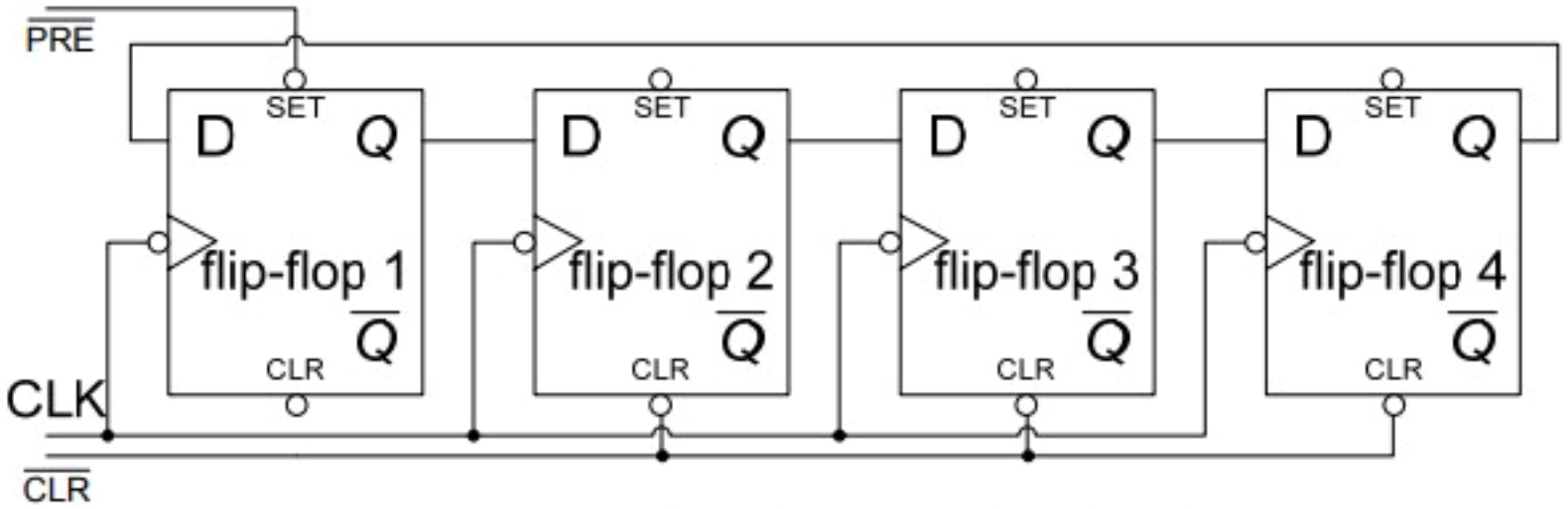


Figure 34.17 4-bit Ring Counter

After the initialization of the counter, the logic high set at the output of the first flip-flop is shifted right at each clock transition. Table 34.2. With a Ring Counter circuit no decoding gates are required. Each state of the ring counter has a unique output.

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

Table 34.2 Sequence of states of a 4-bit Ring Counter

The 74HC164 is an MSI 8-bit Serial In/Parallel Out Shift Register. The Shift register has 8 parallel Outputs, an Asynchronous Active-low CLR input which clears the shift register. The shift register is triggered on the positive clock transition. The Serial data is applied through inputs A and B. Input pins A and B are internally connected through an internal NAND gate. The two pins act as a data input and shift register enable inputs. Serial data is applied at either input A or B. The other input when set to logic high enables the shift operation. The Figure 34.6

SIPO

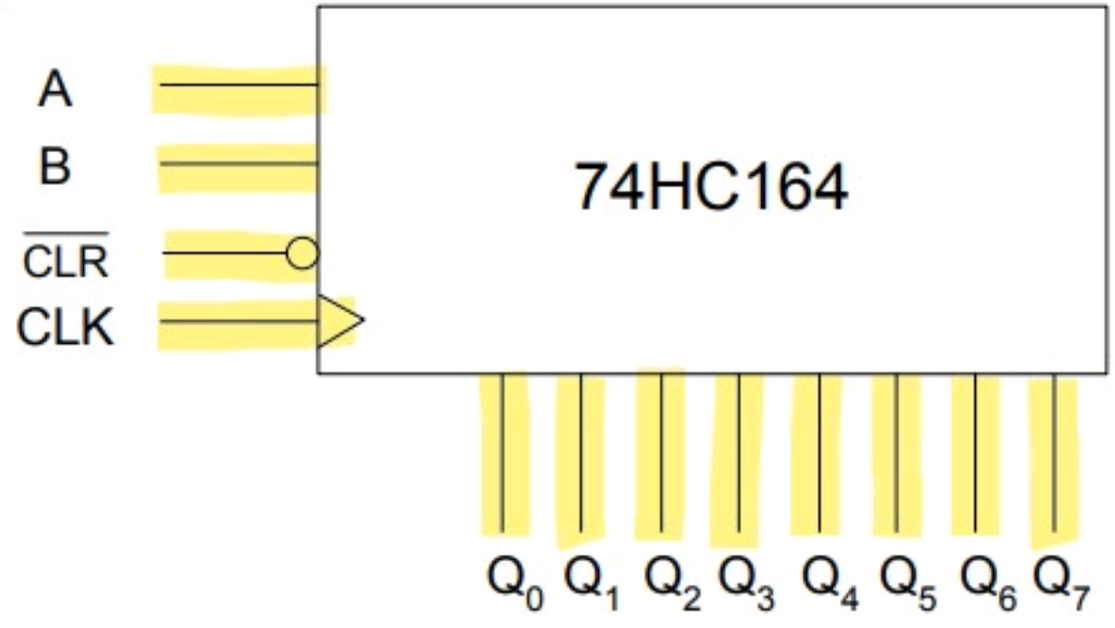


Figure 34.6a 74HC164, 8-bit Serial In/Parallel Out Shift Register

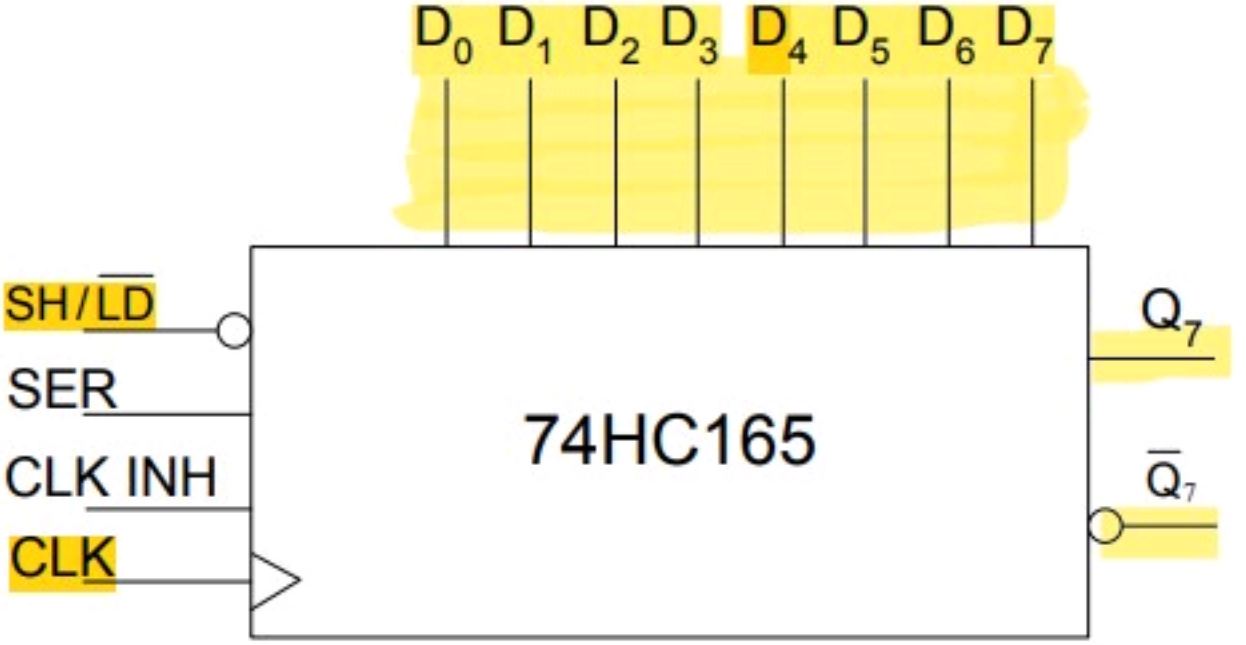


Figure 34.9 74HC165, 8-bit Parallel In/Serial Out Shift Register

344, 345

6. Rotate Right Operation

The serial output of the register is connected to the serial input of the register. By applying clock pulses data is shifted right. The data shifted out of the serial out pin at the right hand side is re-circulated back into the shift register input at the left hand side. Thus the data is rotated right within the register. Figure 34.14

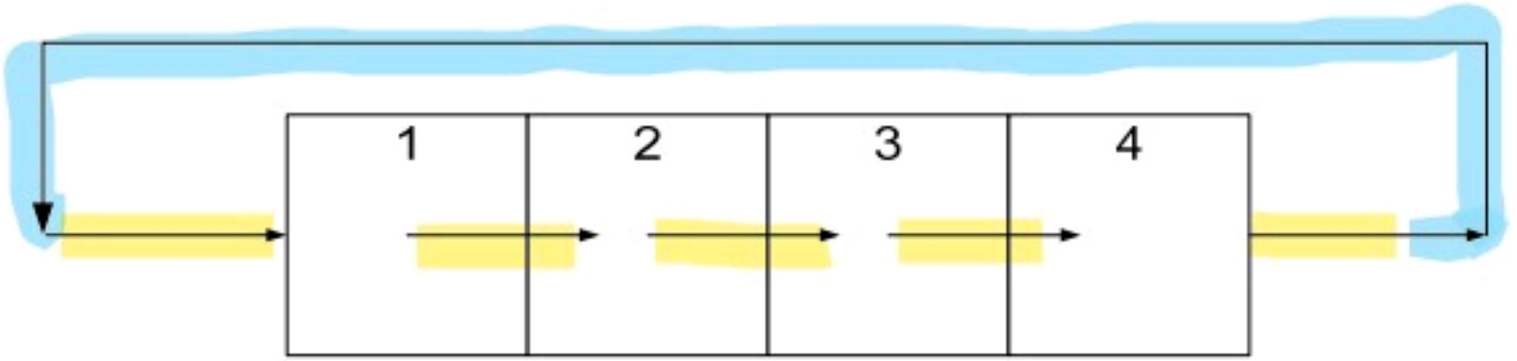
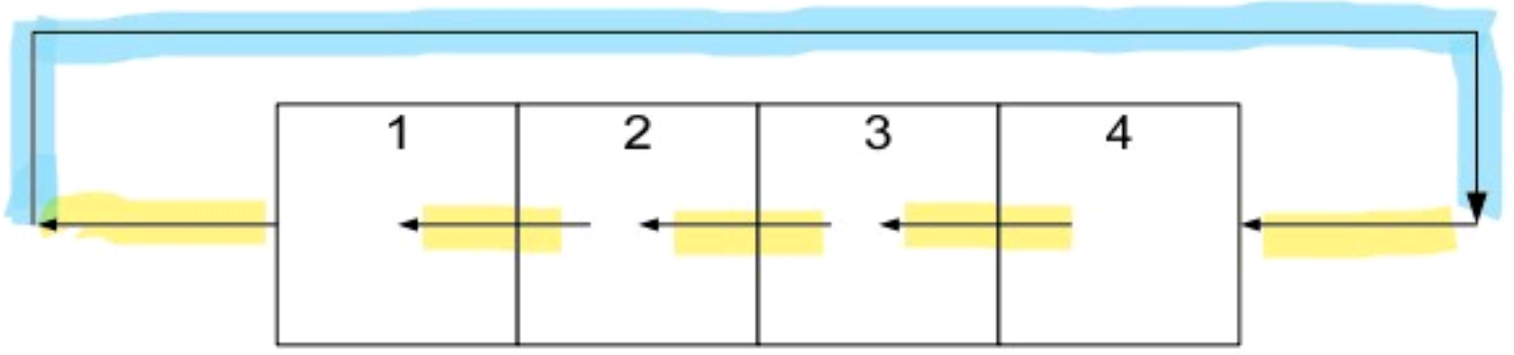


Figure 34.14 Rotate Right Operation

7. Rotate Left Operation

The serial output of the register is connected to the serial input of the register. By applying clock pulses data is shifted left. The data shifted out of the serial out pin at the left hand side is re-circulated back into the shift register input at the right hand side. Thus the data is rotated left within the register. Figure 34.15



7) To Parallel load a byte of data into a shift registor, there must be _____.

a) one clock pulse

8) Implementation of the FIFO buffer in ____ is usually takes the form of a circul buffer.

a) RAM

9) When the Op-Amp is used as an inverting amplifier, the input signal is applied at its Inverted input through a _____.

a) series resistance

10) A memory organized to store nibble data values requires a 4 bit wide data bus.

a) 1, 4 and 8

4) Four 4K Byte chips can be connected together to implemented _ 8K _ word memory.

5) FLASH memory cell is implemented using a single floating-gate ____ transistor.

a) MOS

6) Two states are said to be equal if they have exactly same _____.

a) Next state

1) Implementation of latch is required almost _____ transistor.

a) 4 b) 8 c) 2 **d) 6**

2) In moore machine the output depends upon ____.

a) the current state

3) Memories are implemented in ____ bit data unit series.

a) 1, 4 and 8

CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Start Time: 12:01 AM, 12 September 2022

Question # 9 of 10 (Start time: 12:12:35 AM, 12 September 2022) Total Marks: 1

An 8-bit converter requires_____weighted resistors which have exact values otherwise the output of the converter is not accurate.

Select the correct option

- Ten
- Seven
- Nine
- Eight ✓

CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Start Time: 12:01 AM, 12 September 2022

Question # 7 of 10 (Start time: 12:09:22 AM, 12 September 2022) **Total Marks:** 1

In elevator circuit, the floor display circuit is a combinational circuit which uses the _____ and _____ inputs two determine the floor number and the direction of the display arrow.

Select the correct option

- MOTION, FB
- ✓ MOTION, DIR
- CONSTATE, FB
- OPEN, DIR

CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Start Time: 12:01 AM, 12 September 2022

Question # 6 of 10 (Start time: 12:08:15 AM, 12 September 2022) Total Marks: 1

Memory is arranged in

Select the correct option

- [ ] randome fashion
- [x] two-dimensional manner
- [ ] three-dimensional manner
- [ ] linear fashion

CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Start Time: 12:01 AM, 12 September 2022

Question # 5 of 10 (Start time: 12:07:21 AM, 12 September 2022) Total Marks:

In moore machine the output depends on

Select the correct option

- the current state
- the current state and inputs
- the current state and the output of previous flip flop
- only inputs

CS302 - Digital Logic Design (Semester Quiz # 04) Quiz Start Time: 12:01 AM, 12 September 2022

Question # 4 of 10 (Start time: 12:06:01 AM, 12 September 2022) Total Marks: 1

A complete unit of information is sometimes called a _____

Select the correct option

- Byte
- Word (Correct)
- Bit
- Nibble