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Aslam U Alaikum!

Dear Students,

In this post we are providing you CS302 Quiz-2 Solution Fall 2022 (21 to 41) 100% correct or right solution.

Semester Quiz # 02

Dear Students,

It is to inform that **Semester Quiz # 02** has been opened today and it will remain open for **48 hours** only. You are strongly advised to take this activity seriously and make sure to submit the quiz within the given date. No quiz submission requests will be entertained later in any case due to any reason.

CS302 Quiz File

To write data to the memory the memory the write cycle is initiated by

Applying the address signals

The counter states or the range of the number of a counter is determined by the formula(“n” represented the total number of flip-flops)

2 raise to power n

THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____ GATE

OR

A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BYTHE MANUFACTURER.

TRUE

in sequential circuits memory elements are connected with_____.

common clock

A synchronous decade counter will have _____ flip-flops

4

the terminal count of a modulus -13 binary counter is

1101

The alternate solution for a multiplexer and a register circuit is _____

Parallel in / Serial out shift register

A 8-bit serial in / parallel out shift register contains the value “8”, _____ clock signal(s) will be required to shift the value completely out of the register.

8

Which of the following output equations determines the output of the state machine?

Max-Q0Q1EN

The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

CONSTATE

Memory is arranged in _____.

two-dimensional manner

The n flip-flops store _____ states.

2^n

PALs tend to execute _____ logic.

SOP

In DRAM read cycle R /W^- signal is activated to read data which is made available on the _____ data line.

D(OUT)

A SOP expression can be implemented by an _____ combination of gates.

AND-OR

Why demultiplexer is called a data distributor?

Single input to Single Output

If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

Same

The AND Gate performs a logical _____ function.

Division

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.

REQ1

_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

Combinational Input

The 64-cell array organized as 8 x 8 cell array is considered

as an 8 byte memory

A 3-variable karnaugh map has

eight cells

_____ Counters as the name indicates are not triggered simultaneously.

Synchronous

The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

Truth Table

The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

XOR, NAND

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

Flash memory Operation are classified into _____ different operation.

Two

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1111

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.

AND

The domain of the expression AB'CD + AB' + C'D + B is

A, B, C and D

The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacents 1s are detected in the input, the output is set to high.

1

Which of the following Output Equations determines the output of the State Machine?

MAX = Q0Q1EN

When the transmission line is idle in an asynchronous transmission

It is set to logic high

In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

NAND, NAND

PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

PLDs

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

The terminal count of a 4-bit binary counter in the UP mode is _____.

1100

Select the mode of programming in which GAL16V8 can be programmed:

All of the given

Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

256

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.

1001

In memory write cycle, the time for which the WE signal remains active is known as the _____.

Write pulse width

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

row, column

The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

four

The Transition table is very similar to the _____ table.

State

A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

NOR, NAND

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.

Shift Registers

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.

None of the given

The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

NAND

The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.

Small

Canonical form is a unique way of representing _____.

SOP

UVERPROM is stands for

Ultra-Voilet

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

1

Cin is part of _____ Adder.

Full

Which one flip-flop has an invalid output state?

SR

Which of the following is a volatile memory?

DRAM

The maximum value, represented by a single hexadecimal digit is _____.

"F"

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.

Top

8-bit parallel data can be converted into serial data by using _____ multiplexer.

8-to-1

You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);

NSY2 or EWY2

The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

Adding two octal numbers "36" and "71" result in _____.

127

The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

High

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

True

Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

Negative-OR, Negative-AND

A multiplexer with a register circuit converts

Parallel data to serial

Implementation of Latch is required almost _____ transistor.

Six

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

Synchronous

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.

Four

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

One

The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

4

The _____ input overrides the _____ input.

Asynchronous, synchronous

The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.

Three

Subtractors also have output to check if 1 has been _____.

Primed

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.

Q output of all flip-flops to clock input of next flip-flops

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 32

For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1

Two signals _____ and _____ provide the timing inputs to the State Machine.

PTIME and QTIME

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

$\overline{WE}$

Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.

RAM

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

7.8 microsec

The output of a NAND gate is _____ when all the inputs are one.

Zero

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.

8 AND

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -------

THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED

The terminal count of a 4-bit binary counter in the UP mode is .

1111

For a down counter that counts from (111 to 000). If current state is “101” the next state will be

110

The n flip-flops store states.

2^n

An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting

Q output of all flip-flops to clock input of next flip-flops

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated. Circuit counters allow cascading of multiple counters together.

True

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

False

The 74HC163 is a 4-bit Synchronous Counter, it has data output pins.

4

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 16

The synchronous counters are also known as Ripple Counters:

False

Each stage of Master-slave flip-flop works at of the clock signal

One half

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

80 micro seconds

Number of states in an 8-bit Johnson counter sequence are:

16

In moore machine the output depends on

The current state

Asynchronous mean that

Each flip-flop after the first one is enabled by the output of the preceding flip-flop

According to moore circuit, the output of synchronous sequential circuit depend/s on of flip flop.

Present state

In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

0

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

A one-shot mono-stable device contains _

NOR gate, Resistor, Capacitor and NOT Gate

The inputs can be directly mapped to karnaugh maps.

J-K

A mono-stable device only has a single stable state

True

When the Hz sampling interval is selected, the signal at the output of the J-K flipflop has a time period of seconds.

1, 2

The _____ Encoder is used as a keypad encoder.

Decimal-to-BCD Priority

3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

1

NOR gate is formed by connecting _____

OR Gate and then NOT Gate

A particular half adder has

2 INPUTS AND 2 OUTPUT

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to .

Toggle

A stage in the shift register consists of

A flip flop

If a circuit suffers “Clock Skew” problem, the output of circuit can’t be guarantied.

True

A modulus-14 counter has fourteen states requiring

4 flip flops

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using gate.

NOT

flip-flops are obsolete now.

Master-Slave

The glitches due to “Race Condition” can be avoided by using a .

Negative-Edge triggered flipflops

For a gated D-Latch if EN=1 and D=1 then Q(t+1)=

1

occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Clock skew

An Astable multivibrator is known as a (n) .

Oscillator

In Master-Slave flip-flop setup, the master flip-flop operators at

Both Master-Slave operator simultaneously

The power consumed by a flip-flop is defined by _

c.P = Vcc x Icc

The 3-bit up counter can be implemented using flip-flop(s).

S-R flip-flops and D-flip-flops

The terminal count of a 4-bit binary counter in the DOWN mode is

0000

If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

NOT

The low to high or high to low transition of the clock is considered to be a(n) _____

Edge

RCO Stands for _____

Ripple Clock Output

A transparent mode means _____

The changes in the data at the inputs of the latch are seen at the output

In _____ outputs depend only on the current state.

Moore Machine

Smallest unit of binary data is a _____

Bit

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

State assignment

State of flip-flop can be switched by changing its

Input signal

Once the state diagram is drawn for any sequential circuit the next step is to draw

Next-state table

Design of state diagram is one of many steps used to design

A truncated counter

Flip flops are also called_____.

Bi-stable multivibrators

Three cascaded modulus-10 counters have an overall modulus of

1000

The term hold always means .

No change

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?

J=X(Don’tcare),K=0

To parallel load a byte of data into a shift register, there must be

One clock pulse

Invalid state of NOR based SR latch occurs when _____.

S=1, R=1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

Hold time

74HC163 has two enable input pins which are _____ and _____

ENP, ENT

_____ is said to occur when multiple internal variables change due to change in one input variable

Race condition

The _____ input overrides the _____ input

Asynchronous, synchronous

A decade counter is _____.

Mod-10 counter

In asynchronous transmission when the transmission line is idle, _____

It is set to logic high

A 8-bit serial in / parallel out shift register contains the value “8”, _____ clock signal(s) will be required to shift the value completely out of the register.

8

In a sequential circuit the next state is determined by _____ and _____

Current state and external input

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

Mod-6, Mod-10

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

True

A Nibble consists of _____ bits

4

Excess-8 code assigns _____ to “-8”

0000

The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

LUT is acronym for _____

Look Up Table

The three fundamental gates are _____

NOT, OR, AND

The total amount of memory that is supported by any digital system depends upon _____

The size of the address bus of the microprocessor

Stack is an acronym for _____

LIFO memory

Addition of two octal numbers “36” and “71” results in _____

127

_____ is one of the examples of synchronous inputs.

J-K input

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Clock Skew

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

_____ is used to simplify the circuit that determines the next state.

State assignment

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

0000

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

Doesn't have an invalid state

A multiplexer with a register circuit converts _____

Parallel data to serial

GAL is essentially a _____.

Reprogrammable PAL

in _____, all the columns in the same row are either read or written.

FAST Mode Page Access

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Fist In First Out Memory

A flip-flop changes its state when _____

Low-to-high transition of clock

A frequency counter _____

Counts no. of clock pulses in 1 second

In a sequential circuit the next state is determined by _____ and _____

Input and clock signal applied

Flip flops are also called _____

Bi-stable multivibrators

Given the state diagram of an up/down counter, we can find _____

The next state of a given present state

A Nibble consists of _____ bits

4

The output of this circuit is always _____.

1

A logic circuit with an output X ABC AB consists of _____.

two AND gates, one OR gate, two inverters

The diagram given below represents _____

Sum of product form

The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

DRAM stands for _____

Dynamic RAM

The three fundamental gates are _____

NOT, OR, AND

Which of the following statement is true regarding above block diagram?

Triggering can take place anytime during the HIGH level of the CLK waveform

The expression F=A+B+C describes the operation of three bits _____ Gate.

OR

Addition of two octal numbers “36” and “71” results in _____

127

The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.

32-bit

The decimal “17” in BCD will be represented as _____

10111

The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

Zero

_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

12

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

AND

_____ is one of the examples of asynchronous inputs. ?

J-K input

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the countercounts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be_____.

1101 (not sure)

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

_____ is used to minimize the possible no. of states of a circuit.

State assignment

The best state assignment tends to _____.

Maximizes the number of state variables that don't change in a group of related states

5-bit Johnson counter sequences through ____ states

10

The address from which the data is read, is provided by _____

Microprocessor

FIFO is an acronym for _____

First In, First Out

The voltage gain of the Inverting Amplifier is given by the relation _____

Vout / Vin = - Rf / Ri

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

Accuracy

Above is the circuit diagram of _____.

Asynchronous up-counter

The sequence of states that are implemented by a n-bit Johnson counter is

2n (n multiplied by 2)

"A + B = B + A" is _____

Commutative Law

Following is standard POS expression

True

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

Using Iterative Circuit based Comparators

DE multiplexer is also called

Data distributor

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

_____ Counters as the name indicates are not triggered simultaneously.

Asynchronous

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

A synchronous decade counter will have _____ flip-flops

4

The alternate solution for a demultiplexer-register combination circuit is _____

Serial in / Parallel out shift register

The 4-bit 2"s complement representation of “+5” is _____

0101

The storage cell in SRAM is

a capacitor

What is the difference between a D latch and a D flip-flop?

The D flip-flop has a clock input.

For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs Will _____ if the clock goes HIGH.

toggle

The OR gate performs Boolean _____.

addition

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

set

The power dissipation, PD, of a logic gate is the product of the

dc supply voltage and the peak current

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

True

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

True

Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

A parallel to serial converter circuit

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

8

In designing any counter the transition from a current state to the next sate is determined by

Current state and inputs

Sum term (Max term) is implemented using _____ gates

OR

AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS “1”. WHAT WILL

BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

8 (not sure)

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

1

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

Invalid

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

J-K flip-flop

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop of the shift register.

Ring counter

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

Access Time

Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state

Two

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

8

A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry(Cout) when A = 1 and B = 1?

= 0, Cout = 1

THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

NEGATIVE-EDGE TRIGGERED FLIP-FLOPS

The design and implementation of synchronous counters start from _____

state diagram

THE HOURS COUNTER IS IMPLEMENTED USING _____

A SINGLE DECADE COUNTER AND A FLIP-FLOP

The high density FLASH memory cell is implemented using _____

1 floating-gate MOS transistor

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

Q2:= Q1 # X # Q3

When the control line in tri-state buffer is high the buffer operates like a _____gate

NOT

The output of an AND gate is one when _____

All of the inputs are one

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

A > B = 1, A < B = 0, A = B = 0

The diagram above shows the general implementation of _____ form

POS

The device shown here is most likely a

Multiplexer

DE multiplexer converts _____ data to _____data

Serial data, parallel data

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

1

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

Invalid

In asynchronous digital systems all the circuits change their state with respect to a common clock

False

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

50 Hz

The design and implementation of synchronous counters start from _____

state diagram

The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called_____

In-System Programming (ISP)

Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.

XNOR

In _____ outputs depend only on the combination of current state and inputs.

Mealy machine

In the following statement Z PIN 20 ISTYPE „reg.invert";

Active-low Registered Mode output

A Nibble consists of _____ bits

4

A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.

1001

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Fist In First Out Memory

If the FIFO Memory output is already filled with data then _____

None of given options

The process of converting the analogue signal into a digital representation (code) is known as _____

Quantization

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

Q2:= Q1 # X # Q3

The simplest and most commonly used Decoders are the _____ Decoders

n to 2n

In _____ the output of the last flip-flop of the shift register is connected to the data input of the first flipflop. ?

Johnson counter

Which is not characteristic of a shift register?

Serial in/parallel in

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

TRUE

The output of an XNOR gate is 1 when _____ I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one

II and III only

NAND gate is formed by connecting _____

AND Gate and then NOT Gate

Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

One

CS302 quiz 2

#mcqsfinalterm

Question # 2 of 10 (Start time: 09:43:24 PM) Total Marks: 1
A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:
Select correct option:
0001
1000
1110
1111

Question # 3 of 10 (Start time: 09:43:53 PM) Total Marks: 1
In moore machine the output depends on
Select correct option:
the current state and the output of previous flip flop
only inputs
the current state
the current state and inputs

Question # 4 of 10 (Start time: 09:44:05 PM) Total Marks: 1
In designing any counter the transition from a current state to the next sate is determined by
Select correct option:
Current state and inputs
Only inputs
Only current state
current state and outputs

Question # 5 of 10 (Start time: 09:44:33 PM) Total Marks: 1
A divide-by-10 Johnson counter requires
Select correct option:
ten flip-flops
four flip-flops
five flip-flops
twelve flip-flops

Question # 6 of 10 (Start time: 09:44:46 PM) Total Marks: 1
Number of states in an 8-bit Johnson counter sequence are:
Select correct option:
8
12
14
16

Question # 7 of 10 (Start time: 09:45:20 PM) Total Marks: 1
In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is _____
Select correct option:
0000
1111
0001
10000

Question # 8 of 10 (Start time: 09:45:44 PM) Total Marks: 1
Divide-by-32 counter can be acheived by using
Select correct option:

Flip-Flop and DIV 10
Flip-Flop and DIV 16
Flip-Flop and DIV 32
DIV 16 and DIV 32

Question # 9 of 10 (Start time: 09:46:53 PM) Total Marks: 1
A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is
Select correct option:
0001
1000
1110
1111

Question # 10 of 10 (Start time: 09:47:16 PM) Total Marks: 1
Three cascaded modulus-10 counters have an overall modulus of
Select correct option:
30
100
1000
10000

1. **The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.**

    1. NOT
    2. **AND**
    3. OR
    4. XOR

2. The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

1. AND
2. **NAND**
3. OR
4. NOT

3. The AND Gate performs a logical _____ function.

1. Addition
2. Substraction
3. Multiplication
4. **Division**

4. The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

1. **CONSTATE**
2. FLOOR
3. MOTION
4. OPEN

5. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

1. $\overline{CS}$
2. **$\overline{WE}$**
3. W
4. OE

6. The terminal count of a 4-bit binary counter in the UP mode is _____.

1. **1100**
2. 0011
3. 1111
4. 0000

7. **The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.**

    1. REQ0
    2. OPEN
    3. **REQ1**
    4. FLOOR1

8. **Why demultiplexer is called a data distributor?**

    1. The input will be distributed to one of the outputs
    2. The input will be selected for the output
    3. The output will be distributed to one of the inputs
    4. **Single input to Single Output**

9. **A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:**

    1. 0001
    2. 1000
    3. 1110
    4. **1111**

10. **For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.**

    1. 111
    2. 110
    3. 010
    4. **None of the given**

11. **PALs tend to execute _____ logic.**

    1. SPD
    2. **SOP**

3. SAC
4. SAP

12. The domain of the expression AB'CD + AB' + C'D + B is

1. A and D
2. B only
3. **A, B, C and D**
4. None of the given

13. If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.

1. **1001**
2. 0110
3. 1111
4. 1100

14. _____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

1. Combinational Input/Output
2. Combinational Output
3. **Combinational Input**
4. Programmable polarity

15. In the keyboard encoder, how many times per second does the ring counter scan the key board?

1. 600 scans/second
2. 625 scans/second
3. **650 scans/second**
4. 700 scans/second

16. Which of the following is a volatile memory?

1. PROM
2. **DRAM**
3. EPROM

4. EEPROM

17. Subtractors also have output to check if 1 has been _____.

1. Primed
2. Shifted
3. Complemented
4. Borrowed

18. Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

1. Negative-OR, Negative-AND
2. Negative-AND, Positive-OR
3. Positive-OR, Negative-AND
4. Positive-OR, Positive-AND

19. Which of the following Output Equations determines the output of the State Machine?

1. MIN = Q0Q1
2. MAX = Q0Q1EN
3. MIN = Q0Q1EN
4. MAX = Q1EN

20. The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

1. two
2. four
3. eight
4. sixteen

21. The output of a NAND gate is _____ when all the inputs are one.

1. Zero
2. One

3. Available
4. Not available

22. A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

1. XOR, NAND
2. NOR, XOR
3. **NOR, NAND**
4. OR, XOR

23. The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.

1. One
2. Two
3. **Three**
4. Four

24. The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

1. Sequential
2. Asynchronous
3. **Synchronous**
4. Combinational

25. The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

1. Slow
2. **Faster**
3. Medium
4. Modern

26. UVERPROM is stands for

1. Ultra-Variant
2. Ultra-Vibrant

3. Ultra-Voilet

4. Ultra-Visible

27. Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

1. Zero
2. **One**
3. Undefined
4. No output as input is invalid

28. Two signals _____ and _____ provide the timing inputs to the State Machine.

1. NSSR and EWSR
2. LTIME and STIME
3. **PTIME and QTIME**
4. NSGrn and NSYel

29. An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.

1. **Q output of all flip-flops to clock input of next flip-flops**
2. Q' output of all flip-flops to clock input of next flip-flops
3. Q output of all flip-flops to J input of next flip-flops
4. Q' output of all flip-flops to K input of next flip-flops

30. PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

1. PLAs
2. PALs
3. **PLDs**
4. EPROM

31. The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to

allow Complemented or Un-Complemented B input to be connected to the Adder input.

1. AND, NOR
2. AND, NOT
3. AND, OR
4. **XOR, NAND**

32. In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

1. **True**
2. False

33. You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);

1. **NSY2 or EWY2**
2. NSSR or TMRST
3. EWSR or NSRED
4. EWRed or EWYel

34. The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

1. 2
2. **4**
3. 6
4. 8

35. When the transmission line is idle in an asynchronous transmission

1. It is set to logic low
2. **It is set to logic high**
3. It remains in previous state
4. State of transmission line is not used to start transmission

36. For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1. 0
2. **1**
3. x (don't care condition)
4. Any of given option depending on SOP term

37. The Transition table is very similar to the _____ table.

1. Truth
2. **State**
3. Transition
4. None of the given

38. Select the mode of programming in which GAL16V8 can be programmed:

1. Simple Mode
2. Complex Mode
3. Registered Mode
4. **All of the given**

39. The _____ input overrides the _____ input.

1. **Asynchronous, synchronous**
2. Synchronous, asynchronous
3. Preset input (PRE), Clear input (CLR)
4. Clear input (CLR), Preset input (PRE)

40. Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.

1. 8 OR
2. **8 AND**

41. Flash memory Operation are classified into _____ different operation.

1. **Two**
2. Three
3. Four
4. Five

42. _____ Counters as the name indicates are not triggered simultaneously.

1. Asynchronous
2. **Synchronous**
3. Positive-Edge triggered
4. Negative-Edge triggered

43. Memory is arranged in _____.

1. linear fashion
2. **two-dimensional manner**
3. three-dimensional manner
4. random fashion

44. Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.

1. **Shift Registers**
2. Circular Buffers
3. Ring Buffers
4. Reduce Registers

45. Divide-by-32 counter can be achieved by using

1. Flip-Flop and DIV 10
2. Flip-Flop and DIV 16
3. **Flip-Flop and DIV 32**
4. DIV 16 and DIV 32

46. The n flip-flops store _____ states.

1. 1
2. **2^n**
3. 0

4. 2^(n+1)

47. In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

1. 4.8 microsec
2. 5.9 microsec
3. **7.8 microsec**
4. 5.5 microsec

48. The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

1. Low
2. **High**
3. Medium
4. Hot

49. A SOP expression can be implemented by an _____ combination of gates.

1. OR-XOR
2. AND-NAND
3. **AND-OR**
4. XOR-NOR

50. In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

1. NOR, NAND
2. NAND, NOR
3. NOR, NOR
4. **NAND, NAND**

51. The 64-cell array organized as 8 x 8 cell array is considered

1. as an 64 byte memory

2. as a 16 byte memory
3. as an 8 byte memory
4. as an 4 byte memory

52. Cin is part of _____ Adder.

1. Half
2. Full
3. Single
4. Double

53. In DRAM read cycle R /W^- signal is activated to read data which is made available on the _____ data line.

1. D(IN)
2. D(OUT)
3. D(AB)
4. D(INT)

54. The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.

1. Small
2. Large
3. Heavy
4. High

55. The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

1. Truth Table
2. State Diagram
3. Karnaugh Map
4. Logic Circuit

56. The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.

1. One

2. Two
3. Three
4. Four

57. A 3-variable karnaugh map has

1. eight cells
2. three cells
3. sixteen cells
4. four cells

58. The maximum value, represented by a single hexadecimal digit is _____.

1. "E"
2. "F"
3. "G"
4. "H"

59. The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacents 1s are detected in the input, the output is set to high.

1. 2
2. 4
3. 1
4. 0

60. Canonical form is a unique way of representing _____.

1. SOP
2. Minterm
3. Boolean Expression
4. POS

61. Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

1. 64

2. 128
3. 256
4. 512

62. GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

1. column, row
2. row, column
3. column, column
4. row, row

63. Which one flip-flop has an invalid output state?

1. T
2. JK
3. SR
4. D

64. As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.

1. Bottom
2. Top
3. Down
4. Vertex

65. Adding two octal numbers "36" and "71" result in _____.

1. 213
2. 123
3. 127
4. 345

66. If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

1. 0
2. 1

67. A multiplexer with a register circuit converts

1. Serial data to parallel
2. Parallel data to serial
3. Serial data to serial
4. Parallel data to parallel

68. Implementation of Latch is required almost _____ transistor.

1. Two
2. Four
3. Six
4. Eight

69. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

1. True
2. False

70. Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.

1. RAM
2. ROM
3. PPROM
4. Flash Memory

71. 8-bit parallel data can be converted into serial data by using _____ multiplexer.

1. 4-to-2
2. 8-to-1
3. 4-to-4
4. 8-to-4

72. In memory write cycle, the time for which the WE signal remains active is known as the _____.

1. Write address setup
2. **Write pulse width**
3. Write delay width
4. Write data time

73. If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

1. Different
2. **Same**
3. Equal
4. Opposite

Divide-by-32 counter can be acheived by using
Select correct option:

Flip-Flop and DIV 10
Flip-Flop and DIV 16
Flip-Flop and DIV 32
DIV 16 and DIV 32

Question # 2 of 10 (Start time: 03:05:20 PM) Total Marks: 1
The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)
Select correct option:

(n raise to power 2)
(n raise to power 2 and then minus 1)
(2 raise to power n)
(2 raise to power n and then minus 1)

Question # 3 of 10 (Start time: 03:06:36 PM) Total Marks: 1

A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?
Select correct option:

1001
1011
0011
1100

Question # 4 of 10 (Start time: 03:07:37 PM) Total Marks: 1

A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is_____
Select correct option:

0001
1111
1000
1110

Question # 5 of 10 (Start time: 03:09:04 PM) Total Marks: 1

Divide-by-160 counter is acheived by using
Select correct option:

Flip-Flop and DIV 10
Flip-Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

Question # 6 of 10 (Start time: 03:10:01 PM) Total Marks: 1

A counter is implemented using three (3) flip-flops, possibly it will

have _____ maximum output status.
Select correct option:

3
7
8
15

Question # 7 of 10 (Start time: 03:10:49 PM) Total Marks: 1
RCO stands for _____
Select correct option:

Reconfiguration Counter Output
Ripple Counter Output
Reconfiguration Clock Output
Ripple Clock Output

Question # 8 of 10 (Start time: 03:11:38 PM) Total Marks: 1
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
Select correct option:

Race condition
Clock Skew
Ripple Effect
None of given options

Question # 9 of 10 (Start time: 03:12:20 PM) Total Marks: 1
For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____
Select correct option:

111
110
010
none of given options

Question # 10 of 10 (Start time: 03:13:03 PM) Total Marks: 1
A Divide-by-20 counter can be acheived by using
Select correct option:

Flip-Flop and DIV 10
Flip-Flop and DIV 16
Flip-Flop and DIV 32
Div 10 and DIV 16

Q : Ripple Clock Output

The 74HC163 is a 4-bit Synchronous Counter.it has……data output pins
Select correct option:

2
4
6
8

Q : _____ Counters as the name indicates are not triggered simultaneously.
Select correct option:

Asynchronous
Synchronous
Positive-Edge triggered

Negative-Edge triggered

Q : A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.
Select correct option:

3
7
8
15

Q : Design of state diagram is one of many steps used to design
Select correct option:

a clock
a truncated counter
an UP/DOWN counter
any counter

Q : A synchronous decade counter will have _____ flip-flops.
Select correct option:

3
4
7
10

Q : Karnaugh map is used in designing.
Select correct option:

a clock
a counter
an UP/DOWN counter
All of the above

Q : _____ is said to occur when multiple internal variables change due to change in one input variable
Select correct option:

Hold and Wait
Clock Skew
Race condition
Hold delay

Q : An Astable multivibrator is known as a(n) _____
Select correct option:

Oscillator
Booster
One-shot
Dual-shot

Q: _____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
Select correct option:

Race condition
Clock Skew
Ripple Effect
None of given options

Q:The glitches due to "Race Condition" can be avoided by using a _____
Select correct option:

Gated flip-flops

Pulse triggered flip-flops
Positive-Edge triggered flip-flops
Negative-Edge triggered flip-flops

Q: In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together
Select correct option:

True
False

vuhelp.pk

Quiz: *A flip-flop is presently in SET stae and must remain SET on the next cliock pulse. What must j and K be?*
Select correct option:

J = 1, K = 0
J = 1, K = X(Don't care)
J = X(Don't care), K = 0
J = 0, K = X(Don't care)

Q: The *Synchronous counters are also known as Ripple Counters:*
Select correct option:

True
False

Q: *A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.*
Select correct option:

True
False

Quiz: *The terminal count of a 4-bit binary counter in the DOWN mode is_____*
Select correct option:

0000
0011
1100
1111

Quiz: *An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting_____*
Select correct option:

Q output of all flip-flops to clock input of next flip-flops
Q' output of all flip-flops to clock input of next flip-flops
Q output of all flip-flops to J input of next flip-flops
Q' output of all flip-flops to K input of next flip-flops

the terminal count of a modulus-13 binary counter is
Select correct option:

0000
1111
1101
1100

Quiz: *A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.*
Select correct option:

True
False

Quiz: *A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?*
Select correct option:

1001
1011
0011
1100

Quiz: *Design of state diagram is one of many steps used to design*
Select correct option:

a clock
a truncated counter
an UP/DOWN counter
any counter

Quiz: *An Astable multivibrator is known as a(n) _____*
Select correct option:

Oscillator
Booster
One-shot
Dual-shot

Quiz: *The glitches due to "Race Condition" can be avoided by using a _____*
Select correct option:

Gated flip-flops
Pulse triggered flip-flops
Positive-Edge triggered flip-flops
Negative-Edge triggered flip-flops

Quiz: *A decade counter is _____*
Select correct option:

Mod-3 counter
Mod-5 counter
Mod-8 counter
Mod-10 counter

Question # 1 of 10 (Start time: 03:40:29 PM) Total Marks: 1
The terminal count of a 4-bit binary counter in the DOWN mode is_____
Select correct option:
0000
0011
1100
1111

Question # 2 of 10 (Start time: 03:40:50 PM) Total Marks: 1
The Synchronous counters are also known as Ripple Counters:
Select correct option:
True
False

Question # 3 of 10 (Start time: 03:41:08 PM) Total Marks: 1
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
Select correct option:
Race condition
Clock Skew
Ripple Effect
None of given options

Question # 4 of 10 (Start time: 03:41:27 PM) Total Marks: 1
Divide-by-160 counter is acheived by using

Select correct option:

Flip-Flop and DIV 10
Flip-Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

Question # 5 of 10 (Start time: 03:41:44 PM) Total Marks: 1
Design of state diagram is one of many steps used to design
Select correct option:

a clock
a truncated counter
an UP/DOWN counter
any counter

Question # 6 of 10 (Start time: 03:42:01 PM) Total Marks: 1
In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is_____
Select correct option:

0000
1111
0001
10000

The 74HC163 is a 4-bit
Synchronous Counter.it has……data output pins
Select correct option:

2
4
6
8

Q : _____ Counters as the name indicates are not triggered simultaneously.
Select correct option:

Asynchronous
Synchronous
Positive-Edge triggered

Negative-Edge triggered

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Q : A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.
Select correct option:

3
7
8
15

Q : Design of state diagram is one of many steps used to design
Select correct option:

a clock
a truncated counter
an UP/DOWN counter
any counter

Q : A synchronous decade counter will have _____ flip-flops.
Select correct option:

3

4
7
10

Q : Karnaugh map is used in designing.
Select correct option:

a clock
a counter
an UP/DOWN counter
All of the above

Q : _____ is said to occur when multiple internal variables change due to change in one input variable
Select correct option:

Hold and Wait
Clock Skew
Race condition
Hold delay

Q : Three cascaded modulus-10 counters have an overall modulus of
Select correct option:

30
100
1000
10000

Q : An Astable multivibrator is known as a(n) _____
Select correct option:

Oscillator

Booster
One-shot
Dual-shot

Q: _____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
Select correct option:

Race condition
Clock Skew
Ripple Effect
None of given options

Q:The glitches due to "Race Condition" can be avoided by using a _____
Select correct option:

Gated flip-flops
Pulse triggered flip-flops
Positive-Edge triggered flip-flops
Negative-Edge triggered flip-flops

Q: In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together
Select correct option:

True
False

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Quiz: *A flip-flop is presently in SET stae and must remain SET on the next cliock pulse. What must j and K be?*
Select correct option:

J = 1, K = 0
J = 1, K = X(Don't care)
J = X(Don't care), K = 0
J = 0, K = X(Don't care)

***Q: The** Synchronous counters are also known as Ripple Counters:*
Select correct option:

True
False

***Q:** A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.*
Select correct option:

True
False

***Quiz:** The terminal count of a 4-bit binary counter in the DOWN mode is_____*
Select correct option:

0000
0011
1100
1111

***Quiz:** An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting_____*
Select correct option:

Q output of all flip-flops to clock input of next flip-flops
Q' output of all flip-flops to clock input of next flip-flops

Q output of all flip-flops to J input of next flip-flops
Q' output of all flip-flops to K input of next flip-flops

the terminal count of a modulus-13 binary counter is
Select correct option:

0000
1111
1101
1100

Quiz: *A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.*
Select correct option:

True
False

Quiz: *A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?*
Select correct option:

1001
1011
0011
1100

Quiz: *Design of state diagram is one of many steps used to design*
Select correct option:

a clock
a truncated counter

an UP/DOWN counter
any counter

Quiz: *An Astable multivibrator is known as a(n) _____*
Select correct option:

Oscillator
Booster
One-shot
Dual-shot

Quiz: *The glitches due to "Race Condition" can be avoided by using a _____*
Select correct option:

Gated flip-flops
Pulse triggered flip-flops
Positive-Edge triggered flip-flops
Negative-Edge triggered flip-flops

Quiz: *A decade counter is _____*
Select correct option:

Mod-3 counter
Mod-5 counter
Mod-8 counter
Mod-10 counter

Question # 1 of 10 (Start time: 03:40:29 PM) Total Marks: 1
The terminal count of a 4-bit binary counter in the DOWN mode is_____
Select correct option:
0000
0011

1100
1111

Question # 2 of 10 (Start time: 03:40:50 PM) Total Marks: 1
The Synchronous counters are also known as Ripple Counters:
Select correct option:
True
False

Question # 3 of 10 (Start time: 03:41:08 PM) Total Marks: 1
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
Select correct option:
Race condition
Clock Skew
Ripple Effect
None of given options

Question # 4 of 10 (Start time: 03:41:27 PM) Total Marks: 1
Divide-by-160 counter is acheived by using
Select correct option:
Flip-Flop and DIV 10
Flip-Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

Question # 5 of 10 (Start time: 03:41:44 PM) Total Marks: 1
Design of state diagram is one of many steps used to design
Select correct option:
a clock
a truncated counter
an UP/DOWN counter
any counter

Question # 6 of 10 (Start time: 03:42:01 PM) Total Marks: 1

In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is_____

Select correct option:

0000

1111

0001

10000

Which of the number is not a representative of hexadecimal system

Select correct option :

1234

ABCD

1001

DEFH

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together

Select correct option :

True
False

High level Noise Margins (VNH) of CMOS 5 volt series circuits is _____
Select correct option :
0 . 3 V
0 . 5 V
0 . 9 V
3 . 3 V

To get the answer " 1 " in Boolean addition of three variables , _____
Select correct option :
All three variables must be 1
One of the variables must be 1
All three variables must be 0
Any two variables must be 1

The 3 - variable Karnaugh Map (K- Map) has _____ cells for min or max terms
Select correct option :
4
8
12
16

_____ is invalid number of cells in a single group formed by the adjacent cells in K - map
Select correct option :
2
8
12
16

The boolean expression A + B' + C is
a sum term

a literal term
a product term
a complemented term

The Binary number 1011 .101 has an Integer part represented by _____ and a fraction part _____ separated by a decimal point .
Select correct option :
1011, 101
101, 1011
101, 1101
10111, 11

Adding two octal numbers " 36 " and " 71 " result in _____
Select correct option :
213
123
127
345

Adding two octal numbers " 36 " and " 71 " result in _____
Select correct option :
213
123
127
345

If we multiply " 723 " and " 34 " by representing them in floating point notation i .e . by first , converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____

Select correct option :
24 .582
2 . 4582
24582 not sure
0 . 24582

NOR Gate can be used to perform the operation of AND, OR and NOT Gate
Select correct option :
TRUE
FALSE

The three fundamental gates are _____
Select correct option :
AND, NAND, XOR
OR , AND, NAND
NOT, NOR , XOR
NOT, OR , AND

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result
Select correct option :
1001
0110
1111
1100

A SOP expression having a domain of 3 variables will have a truth table having _____ combinations of inputs and corresponding output values .
Select correct option :
2
4

8
16

In designing any counter the transition from a current state to the next sate is determined by
Select correct option :
Current state and inputs
Only inputs
Only current state
current state and outputs

The 4 - variable K - Map has _____ rows and _____ columns of cells .
Select correct option :
2 , 2
2 , 4
4 , 2
4 , 4

A standard SOP form has _____ terms that have all the variables in the domain of the expression.
Sum

A synchronous decade counter will have _____ flip - flops
Select correct option :
3
4
7
10

.Which one of the following is not a valid rule of Boolean algebra?
(a) A + 1 = 1
(b) A = $\bar{A}$

(c) A. A = A
(d) A + 0 = A

How many data select lines are
required for selecting eight inputs ?
1
2
3
4

If two adjacent 1 s are detected in the
input , the output is set to high .
input combinations will be
0011
0101
1100
1010

The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1. ▶ Undefined ▶ One ▶ Zero ▶ No Output as input is invalid.

CS302 Question No: 5 (M - 1) **_____ is invalid number of cells in a single group formed by the adjacent cells in K-map.**

▶ 2 ▶ 8
▶ 12 ▶ 16

CS302 Question No: 6 (M - 1) **The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.** ▶ AND ▶ OR ▶ NOT ▶ XOR

CS302 Question No: 7 (M - 1) **_____ is one of the examples of synchronous inputs.**

▶ J-K input
▶ EN input
▶ Preset input (PRE)
▶ Clear Input (CLR)

The 4 - variable Karnaugh Map (K - Map)
has _____ rows and _____colums
2 , 2
4 , 4
4 , 2
2 , 4

the boolean expression AB 'CD 'is
a sumterm
a product term
a literal term
always 1

Don’ t care conditions are marked as
_____ in the output column of
the function table
0
1
X
None of the given options

An example of SOP expression is
A + B (C + D)
A' B + AC ' + AB ' C
(A ' + B + C)(A + B ' + C)
both (a) and (b)

In a 4 - bit binary counter , the next
state after the terminal count in the
DOWN mode is _____
Select correct option :
0000
1111

0001
10000

A SOP expression having a domain of 3 variables will have a truth table having _____ combinations of inputs and corresponding output values .
Select correct option :
2
4
8
16

The OR Gate performs a Boolean _____ function
Select correct option :
Addition
Subtraction
Multiplication
Division

Sum term (Max term) is implemented using _____ gates
Select correct option :
OR
AND
NOT
OR - AND

Above is the circuit diagram of _____.

- Asynchronous up-counter
- Asynchronous down-counter
- Synchronous up-counter
- Synchronous down-counter

CS302 Question No: 26 (M - 1) **The sequence of states that are implemented by a n-bit Johnson counter is**

► n+2 (n plus 2) ► 2n (n multiplied by 2) ► 2n (2 raise to power n) ► n2 (n raise to power 2)

The number " 1259" may belong to _____ number system .
Select correct option :
Binary number system
Octal or Decimal system .
Decimal or Hexadecimal system
Binary or Hexadecimal system

" 1101 " in signed representation is equivalent to _____
Select correct option :
10
13
- 10
- 5

TTL based devices work with a dc supply of _____ Volts
Select correct option :
+ 10
+ 5
+ 3
3 . 3

In decimal value " 275 " the weight of the digit " 7 " is _____
Select correct option :
0
1
10

100

The decimal " 10 " will have an octal equivalent _____
Select correct option :
9
10
11
12

Caveman number system is Base _____ number system
Select correct option :
2
5
10
16

The terminal count of a 4 - bit binary counter in the DOWN mode is_ _____
Select correct option :
0000
0011
1100
1111

A divide- by- 10 ring counter requires a minimum of
Select correct option :
ten flip - flops
five flip - flops
four flip - flops
twelve flip - flops

In moore machine the output depends on
Select correct option :
the current state and the output of previous flip flop
only inputs
the current state

When an eight bit serial in / serial out shift register is used for a 24 micro seconds time delay , the clock frequenct must be
Select correct option :
41 .67 KHz
333 KHz
125 KHz
8 MHz

To parallel load a byte of data into a shift register , there must be
Select correct option :
one clock pulse
one clock pulse for each 1 in the data
eight clock pulse
one clock pulse for each 0 in the data

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

With a 100 KHz clock frequency , eight bits can be serially entered into a shift register in

Select correct option :
80 micro seconds
8 micro seconds
80 mili seconds
10 micro seconds

1011+ 101 = _____
Select correct option :
10000
00001
10011
11001

Once the state diagram is drawn for any sequential circuit the next step is to draw
Select correct option :
Transiation table
Karnaugh map
Next- state table
Logic expression

When an eight bit serial in / serial out shift register is used for a 24 micro seconds time delay , the clock frequenct must be
Select correct option :
41 .67 KHz
333 KHz Not Confirm
125 KHz
8 MHz

A 4 - bit binary up / down counter is in the binary state of zero . The next state in the DOWN mode is :
Select correct option :
0001
1000
1110

1111

In moore machine the output depends on
Select correct option :
the current state and the output of previous flip flop
only inputs
the current state
the current state and inputs

A divide- by- 10 Johnson counter requires
Select correct option :
ten flip - flops
four flip - flops
five flip - flops
twelve flip - flops

Number of states in an 8 - bit Johnson counter sequence are :
Select correct option :
8
12
14
16

In a 4 - bit binary counter , the next state after the terminal count in the DOWN mode is _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Select correct option :
0000
1111
0001
10000

Divide - by- 32 counter can be acheived

by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
Flip - Flop and DIV 32
DIV 16 and DIV 32

A 4 - bit binary up / down counter is in the binary state of zero . The next state in the UP mode is
Select correct option :
0001
1000
1110
1111

Three cascaded modulus - 10 counters have an overall modulus of
Select correct option :
30
100
1000
10000

A stage in the shift register consists of
Select correct option :
a latch
a flip flop
a byte of storage
four bits of storage

When an eight bit serial in / serial out shift register is used for a 24 micro seconds time delay , the clock frequenct must be
Select correct option :
41 .67 KHz
333 KHz not confirm

125 KHz
8 MHz

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

A 4 - bit UP / DOWN counter is in DOWN mode and in the 1010 state . on the next clock pulse , to what state does the counter go ?
Select correct option :
1001
1011
0011
1100

In moore machine the output depends on
Select correct option :
the current state and the output of previous flip flop
only inputs
the current state
the current state and inputs

A divide- by- 10 Johnson counter requires
Select correct option :
ten flip - flops
four flip - flops
five flip - flops
twelve flip - flops

Three cascaded modulus - 10 counters have an overall modulus of
Select correct option :
30
100
1000
10000

A divide- by- 10 ring counter requires a minimum of
Select correct option :
ten flip - flops
five flip - flops
four flip - flops
twelve flip - flops

Number of states in an 8 - bit Johnson counter sequence are :
Select correct option :
8
12
14
16

the terminal count of a modulus - 13 binary counter is
Select correct option :
0000
1111
1101
1100

A Divide - by- 20 counter can be acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16

Flip - Flop and DIV 32
Div 10 and DIV 16

To serially shift a byte of data into a shift register , there must be
Select correct option :
one clock pulse
one load pulse
eight clock pulses
one clock pulse for each 1 in the data

In moore machine the output depends on
Select correct option :
the current state and the output of previous flip flop
only inputs
the current state
the current state and inputs
1
A divide- by- 10 Johnson counter requires
Select correct option :
ten flip - flops
four flip - flops
five flip - flops
twelve flip - flops

A 4 - bit binary up / down counter is in the binary state of zero . The next state in the DOWN mode is :
Select correct option :
0001
1000
1110
1111

A divide- by- 10 ring counter requires a

minimum of
Select correct option :
ten flip - flops
five flip - flops
four flip - flops
twelve flip - flops

A multiplexer with a register circuit converts
Select correct option :
Serial data to parallel
Parallel data to serial
Serial data to serial
Parallel data to parallel

In designing any counter the transition from a current state to the next sate is determined by
Select correct option :
Current state and inputs
Only inputs
Only current state
current state and outputs

A decade counter can be implemented by truncating the counting sequence of a MOD - 20 counter .
Select correct option :
True
False

The terminal count of a 4 - bit binary counter in the DOWN mode is_ _____
Select correct option :
0000
0011
1100

1111

An Asynchronous Down - counter is implemented (Using J - K flip - flop) by connecting _____
Select correct option :
output of all flip - flops to clock input of next flip - flops
output of all flip - flops to clock input of next flip - flops
output of all flip - flops to J input of next flip - flops
output of all flip - flops to K input of next flip - flops

the terminal count of a modulus - 13 binary counter is
Select correct option :
0000
1111
1101
1100

A decade counter can be implemented by truncating the counting sequence of a MOD - 20 counter .
Select correct option :
True
False

A 4 - bit UP / DOWN counter is in DOWN mode and in the 1010 state . on the next clock pulse , to what state does the counter go ?
Select correct option :
1001

1011
0011
1100

Design of state diagram is one of many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

An Astable multivibrator is known as a (n) _____
Select correct option :
Oscillator
Booster
One - shot
Dual- shot

The glitches due to " Race Condition" can be avoided by using a _____
Select correct option :
Gated flip - flops
Pulse triggered flip - flops
Positive - Edge triggered flip - flops
Negative - Edge triggered flip - flops

Karnaugh map is used in designing
Select correct option :
a clock
a counter
an UP /DOWN counter
All of the above

_____ is said to occur when multiple internal variables change due to change in one input variable
Select correct option :
Hold and Wait
Clock Skew
Race condition
Hold delay

Three cascaded modulus - 10 counters have an overall modulus of
Select correct option :
30
100
1000
10000

An Astable multivibrator is known as a (n) _____
Select correct option :
Oscillator
Booster
One - shot
Dual- shot

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay .
Select correct option :
Race condition
Clock Skew
Ripple Effect
None of given options

The glitches due to " Race Condition" can be avoided by using a _____
Select correct option :

Gated flip - flops
Pulse triggered flip - flops
Positive - Edge triggered flip - flops
Negative - Edge triggered flip - flops

A flip - flop is presently in SET stae and must remain SET on the next cliock pulse . What must j and K be ?
Select correct option :
J = 1 , K = 0
J = 1 , K = X (Don't care)
J = X(Don't care), K = 0
J = 0 , K = X (Don't care)

The Synchronous counters are also known as Ripple Counters :
Select correct option :
True
False

The Synchronous counters are also known as Ripple Counters :
Select correct option :
True
False

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay .
Select correct option :
Race condition

Clock Skew
Ripple Effect
None of given options

Divide - by- 160 counter is acheived by
using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

Design of state diagram is one of
many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

_____ Counters as the name
indicates are not triggered
simultaneously
Select correct option
Asynchronous
Synchronous
Positive - Edge triggered
Negative- Edge triggered

Ripple Clock Output
The 74 HC 163 is a 4 - bit Synchronous
Counter .it has . ...data output pins
Select correct option :
2
4
6

8

A counter is implemented using three (3) flip - flops , possibly it will have _____ maximum output status .
Select correct option :
3
7
8
15

Sum term (Max term) is implemented using _____ gates
Select correct option :
OR
AND
NOT
OR - AND

Design of state diagram is one of many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

Divide - by- 32 counter can be acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
Flip - Flop and DIV 32
DIV 16 and DIV 32

The counter states or the range of numbers of a counter is determined by

the formula . (“n ” represents the total number of flip - flops)
Select correct option :
(n raise to power 2)
(n raise to power 2 and then minus 1)
(2 raise to power n)
(2 raise to power n and then minus 1)

A 4 - bit UP / DOWN counter is in DOWN mode and in the 1010 state . on the next clock pulse , to what state does the counter go ?
Select correct option :
1001
1011
0011
1100

A 4 - bit binary UP / DOWN counter is in the binary state zero . the next state in the DOWN mode is_ _____
Select correct option :
0001
1111
1000
1110

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

A counter is implemented using three (3) flip - flops , possibly it will have _____ maximum output status .
Select correct option :

3
7
8
15

RCO stands for _____
Select correct option :
Reconfiguration Counter Output
Ripple Counter Output
Reconfiguration Clock Output
Ripple Clock Output

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay .
Select correct option :
Race condition
Clock Skew
Ripple Effect
None of given options

For a down counter that counts from (111 to 000), if current state is " 101 " the next state will be _____
Select correct option :
111
110
010
none of given options

A Divide - by- 20 counter can be acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
Flip - Flop and DIV 32
Div 10 and DIV 16

Design of state diagram is one of many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

An Astable multivibrator is known as a (n) _____
Select correct option :
Oscillator
Booster
One - shot
Dual- shot

_____ is one of the examples of asynchronous inputs.

- ▶ J-K input
- ▶ S-R input
- ▶ D input
- ▶ Clear Input (CLR)

CS302 Question No: 9 (M - 1) **The _____ input overrides the _____ input.** ▶ Asynchronous, synchronous ▶ Synchronous, asynchronous ▶ Preset input (PRE), Clear input (CLR) ▶ Clear input (CLR), Preset input (PRE)

CS302 Question No: 10 (M - 1) **_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.** ▶ Race condition ▶ Clock Skew ▶ Ripple Effect ▶ None of given options

CS302 Question No: 11 (M - 1) **Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and**

X=1, the next state of the counter will be _____

- ▶ 0000
- ▶ 1101
- ▶ 1011
- ▶ 1111

CS302 Question No: 12 (M - 1) **In a state diagram, the transition from a current state to the next state is determined by** ▶ Current state and the inputs ▶ Current state and outputs ▶ Previous state and inputs ▶ Previous state and outputs

CS302 Question No: 13 (M - 1) **_____ is used to minimize the possible no. of states of a circuit.** ▶ State assignment ▶ State reduction ▶ Next state table ▶ State diagram

The glitches due to " Race Condition"
can be avoided by using a _____
Select correct option :
Gated flip - flops
Pulse triggered flip - flops
Positive - Edge triggered flip - flops
Negative- Edge triggered flip - flops

A decade counter is _____
Select correct option :
Mod - 3 counter
Mod - 5 counter
Mod - 8 counter
Mod - 10 counter

The terminal count of a 4 - bit binary
counter in the DOWN mode
is_ _____
Select correct option :
0000
0011
1100
1111

The Synchronous counters are also known as Ripple Counters :
Select correct option :
True
False

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay .
Select correct option :
Race condition
Clock Skew
Ripple Effect
None of given options

Divide - by- 160 counter is acheived by using
Select correct option :
Flip - Flop and DIV 10
Flip - Flop and DIV 16
DIV 16 and DIV 32
DIV 16 and DIV 10

Design of state diagram is one of many steps used to design
Select correct option :
a clock
a truncated counter
an UP /DOWN counter
any counter

12. 3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions
►**True (Page 160)**
►False

13. The device shown here is most likely a _____

►Comparator
►Multiplexer
►**Demultiplexer click here for detail**
►Parity generator

14. The GAL22V10 has _____ inputs

►**22 (Page 195)**
►10
►44
►20

15. A latch retains the state unless

►Power is turned off
►**Input is changed (page 218)**
►Output is changed
►Clock pulse is changed

16. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

►**SET (Page 220)**

►RESET
►Clear
►Invalid

17. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS 5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (VoH) will be in the range of _____ volts.

►4 to 4.5
►**4.5 to 5**

►0 to 4.5
►0 to 3.5

18. A.(B.C) = (A.B).C is an expression of _____
►Demorgan"s Law
►Distributive Law
►Commutative Law
►**Associative Law (Page 72)**

In a 4 - bit binary counter , the next state after the terminal count in the DOWN mode is _____
Select correct option :
0000
1111
0001
10000

A 5 - variable karnaugh map has
Select correct option :
sixteen cells
thirty two cells
sixty- four cells
None of these

The bolean expression A + BC equals
Select correct option :
(A ' + B)(A' + C)
(A + B) (A + C)
(A + B) (A ' + C)
none of the above

the boolean expression AB 'CD 'is
Select correct option :
a sumterm
a product term
a literal term

always 1

The OR Gate performs a Boolean _____ function
►Addition (Page 42)
►Subtraction
►Multiplication
►Division

4. TTL based devices work with a dc supply of _____ Volts
►+10
►+5 (Page 61)
►+3
►3.3

5. A standard POS form has _____ terms that have all the variables in the domain of the expression.
►Sum (Page 85)
►Product
►Min
►Composite

6. A SOP expression having a domain of 3 variables will have a truth table having _____ combinations of inputs and corresponding output values.
►2
►4
►8 (According to rule)
►16

7. A BCD to 7-Segment decoder has
►3 inputs and 7 outputs
►4 inputs and 7 outputs (Page 103)
►7 inputs and 3 outputs
► inputs and 4 outputs

8. In the Karnaugh map shown above, which of the loops shown represents a legal grouping?
►A
►
►**C click here for detail**
►D
9. The binary value of 1010 is converted to the product term
►True
►**False**

Which one of the following is NOT a valid rule of Boolean algebra?
Select correct option :
A + 1 = 1
A = A '
AA = A
A + 0 = A

In a 4 - variable K - map , a 2 - variable product term is produced by
Select correct option :
a 2 - cell group of 1 s
a 8 - cell group of 1 s
a 4 - cell group of 1 s
a 4 - cell group of 0 s

On a Karnaugh map , grouping the 0 s produces
Select correct option :
a POS expression
a SOP expression
a " don ' t care " condition
AND- OR logic

A 3 - variable karnaugh map has

Select correct option :
eight cells
three cells
sixteen cells
four cells

which of the following rules states that if one input of an AND gate is always 1 , the output is equal to the other input ?
Select correct option :
A + 1 = 1
A + A = A
A. A = A
A. 1 = A

2 ' s complement of 5 is
Select correct option :
1101
1011
0101
1100

An example of SOP expression is
Select correct option :
A + B (C + D)
A' B + AC ' + AB ' C
(A ' + B + C)(A + B ' + C)
both (a) nad (b)

2's complement of any binary number can be calculated by
► adding 1's complement twice
► adding 1 to 1's complement (Page 144)
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.
► AND
► OR
► NOT
► **XOR (Page 186)**

1. The binary value "11011" is equivalent to _____
►**1B (According to rule)**
►1C
►1D
►1E

2. An important application of AND Gate is its use in counter circuit
►**True (Page 281)**
►False

Adjacent 1 s detector circuit will have
active low output for the input
Select correct option :
1101
1010 (Not Confirm)
0110
1011

The complement of a variable is always
Select correct option :
0

1
equal to the variable
the inverse of the variable

Adjacent 1 s detector circuit will have active high output for the input
Select correct option :
0101
1010
0011
0001

The domain of the expression AB 'CD + AB ' + C 'D + B is
Select correct option :
A and D
B only
A, B, C and D
none of these

the boolean expression A + B ' + C is
Select correct option :
a sum term
a literal term
a product term
a complemented term

The boolean expression (A + C) (AB ' + AC) (A 'C ' + B ') can be simplified to
Select correct option :
AB '
AB + A' C
A' B + BC
AB + BC

The boolean expression X = AB + CD represents
Select correct option :
two ORs ANDed together

a 4 - input AND gate
two ANDs ORed together
an exclusive - Or

Which one of the following is NOT a
valid rule of Boolean algebra?
Select correct option :
A + 1 = 1
A = A '
AA = A
A + 0 = A
The function to be performed by the processor is selected by set of inputs known as _____
► Function Select Inputs (Page 147)
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?
► 2 (Page 160)
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.
► Giant Array Logic
► General Array Logic (Page 183)
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs
► 4 (Page 216)
► 8

► 12
► 16

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____
► Demorgan"s Law
► Distributive Law
► Commutative Law
► **Associative Law (Page 72)**

How many data select lines are
required for selecting eight inputs ?
Select correct option :
4
3
2
1

the boolean expression AB 'CD 'is
a sumterm
a product term
a literal term
always 1

The boolean expression (A + C) (AB'
+AC) (A 'C ' + B ') can be simplified to
AB '
AB + A 'C
A' B + BC
AB + BC

which of the following rules states
that if one input of an AND gate is
always 1 , the output is equal to the
other input ?

A + 1 =1
A + A = A
A. A = A
A .1 = A

The range of Excess-8 code is from _____ to _____
► +7 to -8 (Page 34)
► +8 to -7
► +9 to -8
► -9 to +8

Question No: 5 (Marks: 1) - Please choose one
A non-standard POS is converted into a standard POS by using the rule _____
►
►
AA □□0 **(Page 85)**
►
► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
► 4
► 8 (Page 89)
► 12
► 16

FINALTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design

Time: 90 min
Marks: 58

Question No: 1 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► 8

Question No: 2 (Marks: 1) - Please choose one

A frequency counter _____

- ► Counts pulse width
- ► Counts no. of clock pulses in 1 second
- ► Counts high and low range of given clock pulse
- ► None of given options

Question No: 3 (Marks: 1) - Please choose one

In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► Current state and external input
- ► Input and clock signal applied

Question No: 4 (Marks: 1) - Please choose one

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► Mod-6, Mod-10
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 5 (Marks: 1) - Please choose one

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► True
- ► False

Question No: 6 (Marks: 1) - Please choose one

Flip flops are also called _____

- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► Bi-stable multivibrators
- ► Bi-stable singlevibrators

Question No: 7 (Marks: 1) - Please choose one

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► Hold time
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 8 (Marks: 1) - Please choose one

74HC163 has two enable input pins which are _____ and _____

- ► ENP, ENT
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Question No: 9 (Marks: 1) - Please choose one

_____ is said to occur when multiple internal variables change due to change in one input variable

- ► Clock Skew
- ► Race condition
- ► Hold delay
- ► Hold and Wait

Question No: 10 (Marks: 1) - Please choose one

Given the state diagram of an up/down counter, we can find _____

- ► The next state of a given present state
- ► The previous state of a given present state
- ► Both the next and previous states of a given state
- ► The state diagram shows only the inputs/outputs of a given states

Question No: 11 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

- ► Asynchronous, synchronous
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 12 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

- ► two AND gates, two OR gates, two inverters
- ► three AND gates, two OR gates, one inverter
- ► two AND gates, one OR gate, two inverters
- ► two AND gates, one OR gate

Question No: 13 (Marks: 1) - Please choose one

A decade counter is _____.

- ► Mod-3 counter
- ► Mod-5 counter
- ► Mod-8 counter

► Mod-10 counter

Question No: 14 (Marks: 1) - Please choose one

In asynchronous transmission when the transmission line is idle, _____

► It is set to logic low
► It is set to logic high
► Remains in previous state
► State of transmission line is not used to start transmission

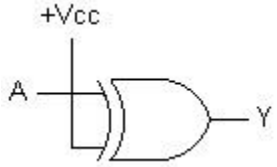
Question No: 15 (Marks: 1) - Please choose one

A Nibble consists of _____ bits

► 2
► 4
► 8
► 16

Question No: 16 (Marks: 1) - Please choose one

The output of this circuit is always _____.



► 1
► 0
► A
► $\overline{A}$

Question No: 17 (Marks: 1) - Please choose one

Excess-8 code assigns _____ to "-8"

► 1110
► 1100
► 1000
► 0000

Question No: 18 (Marks: 1) - Please choose one

The voltage gain of the Inverting Amplifier is given by the relation _____

► $V_{out} / V_{in} = - R_f / R_i$
► $V_{out} / R_f = - V_{in} / R_i$
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / V_{out}$

Question No: 19 (Marks: 1) - Please choose one

LUT is acronym for _____

► Look Up Table
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 20 (Marks: 1) - Please choose one

DRAM stands for _____

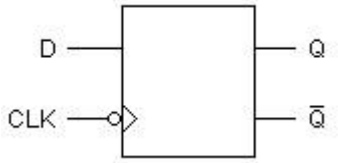
- ▶ Dynamic RAM
- ▶ Data RAM
- ▶ Demoduler RAM
- ▶ None of given options

Question No: 21 (Marks: 1) - Please choose one

The three fundamental gates are _____

- ▶ AND, NAND, XOR
- ▶ OR, AND, NAND
- ▶ NOT, NOR, XOR
- ▶ NOT, OR, AND

Question No: 22 (Marks: 1) - Please choose one



Which of the following statement is true regarding above block diagram ?

- ▶ Triggering takes place on the negative-going edge of the CLK pulse
- ▶ Triggering takes place on the positive-going edge of the CLK pulse
- ▶ Triggering can take place anytime during the HIGH level of the CLK waveform
- ▶ Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 23 (Marks: 1) - Please choose one

The total amount of memory that is supported by any digital system depends upon _____

- ▶ The organization of memory
- ▶ The structure of memory
- ▶ The size of decoding unit
- ▶ The size of the address bus of the microprocessor

Question No: 24 (Marks: 1) - Please choose one

The expression F=A+B+C describes the operation of three bits _____ Gate.

- ▶ OR
- ▶ AND
- ▶ NOT
- ▶ NAND

Question No: 25 (Marks: 1) - Please choose one

Stack is an acronym for_____

- ▶ FIFO memory
- ▶ LIFO memory
- ▶ Flash Memory
- ▶ Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one

Addition of two octal numbers “36” and “71” results in _____

► 213
► 123
► 127
► 345

Question No: 27 (Marks: 2)
Define quantization process.

Question No: 28 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer and 2-to-4 Binary Decoder?

Question No: 29 (Marks: 2)

A general Sequential circuit consists of a combinational circuit and a memory element. How this memory element is implemented

Question No: 30 (Marks: 2)

Suppose a 2 bit up-counter, having states "A, B, C, D". Write down GOTO statements to show how present states change to next states.

Question No: 31 (Marks: 3)

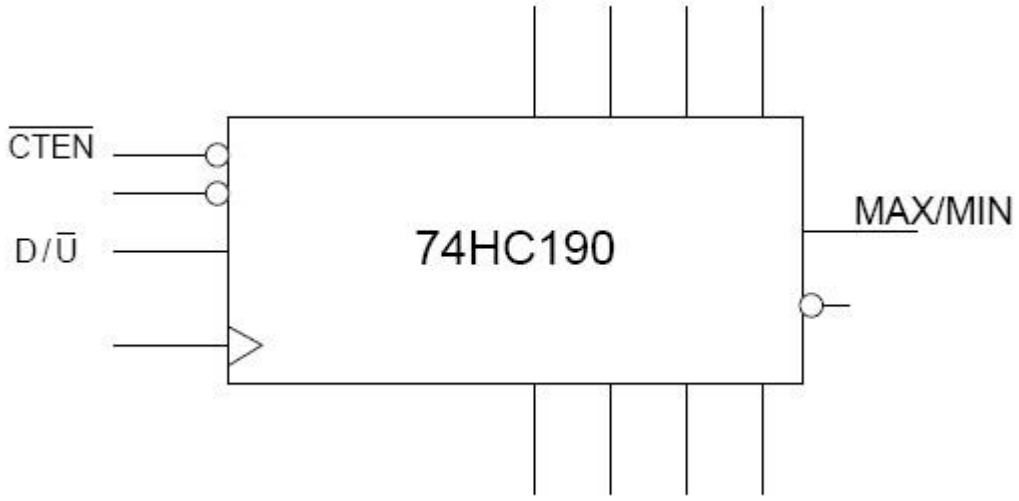
Name three Operations that can be performed on FLASH Memory

Question No: 32 (Marks: 3)

Explain Rotate Right Operation of shift register with the help of diagram.

Question No: 33 (Marks: 3)

You are given the block diagram of 74HC190 integrated circuit up/down counter, explain the function of labeled inputs/outputs.



Question No: 34 (Marks: 5)

Draw the state diagram of 3-bit up-down counter, use an external input X, when X sets to logic 1, the counter counts downwards, otherwise upward.

Question No: 35 (Marks: 5)

Differentiate between synchronous and asynchronous RAM.

Question No: 36 (Marks: 5)

Explain Memory Select or Enable Signals

FINALTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design (Session - 4)

Time: 90 min
Marks: 58

Question No: 1 (Marks: 1) - Please choose one
The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.

- ► 8-bit
- ► 16-bit
- ► **32-bit**
- ► 64-bit

Question No: 2 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____

- ► 11101
- ► 11011
- ► **10111**
- ► 11110

Question No: 3 (Marks: 1) - Please choose one
The basic building block for a logical circuit is _____

- ► A Flip-Flop
- ► **A Logical Gate**
- ► An Adder
- ► None of given options

Question No: 4 (Marks: 1) - Please choose one
The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

- ► Undefined
- ► One
- ► **Zero**
- ► No Output as input is invalid.

Question No: 5 (Marks: 1) - Please choose one
_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

- ► 2
- ► 8
- ► **12**
- ► 16

Question No: 6 (Marks: 1) - Please choose one
The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

- ► **AND**

► OR
► NOT
► XOR

Question No: 7 (Marks: 1) - Please choose one

_____ is one of the examples of synchronous inputs.

► **J-K input**
► EN input
► Preset input (PRE)
► Clear Input (CLR)

Question No: 8 (Marks: 1) - Please choose one

_____ is one of the examples of asynchronous inputs.

► J-K input
► S-R input
► **D input**
► Clear Input (CLR)

Question No: 9 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

► **Asynchronous, synchronous**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 10 (Marks: 1) - Please choose one

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew**
► Ripple Effect
► None of given options

Question No: 11 (Marks: 1) - Please choose one

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

► 0000
► **1101**
► 1011
► 1111

Question No: 12 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one

_____ is used to minimize the possible no. of states of a circuit.

► **State assignment**

► State reduction

► Next state table

► State diagram

Question No: 14 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

► **State diagram**

► Next state table

► State reduction

► State assignment

Question No: 15 (Marks: 1) - Please choose one

The best state assignment tends to _____.

► Maximizes the number of state variables that don't change in a group of related states

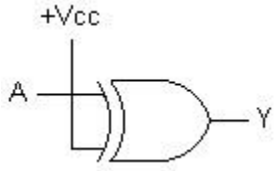
► **Minimizes the number of state variables that don't change in a group of related states**

► Minimize the equivalent states

► None of given options

Question No: 16 (Marks: 1) - Please choose one

The output of this circuit is always _____.



► **1**

► 0

► A

►

Question No: 17 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1

► 2

► 4

► **8**

Question No: 18 (Marks: 1) - Please choose one

5-bit Johnson counter sequences through ____ states

► 7

► 10

► 32

► **25**

Question No: 19 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- ► 1100
- ► 0011
- ► **0000**
- ► 1111

Question No: 20 (Marks: 1) - Please choose one

The address from which the data is read, is provided by _____

- ► Depends on circuitry
- ► None of given options
- ► RAM
- ► **Microprocessor**

Question No: 21 (Marks: 1) - Please choose one

FIFO is an acronym for _____

- ► **First In, First Out**
- ► Fly in, Fly Out
- ► Fast in, Fast Out
- ► None of given options

Question No: 22 (Marks: 1) - Please choose one

LUT is acronym for _____

- ► **Look Up Table**
- ► Local User Terminal
- ► Least Upper Time Period
- ► None of given options

Question No: 23 (Marks: 1) - Please choose one

The voltage gain of the Inverting Amplifier is given by the relation _____

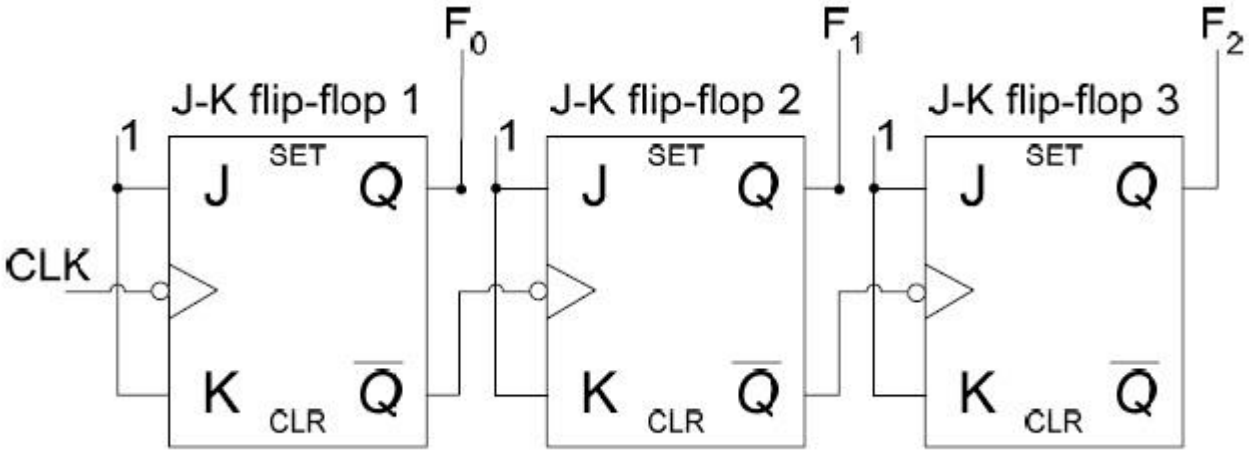
- ► **$V_{out} / V_{in} = - R_f / R_i$**
- ► $V_{out} / R_f = - V_{in} / R_i$
- ► $R_f / V_{in} = - R_i / V_{out}$
- ► $R_f / V_{in} = R_i / V_{out}$

Question No: 24 (Marks: 1) - Please choose one

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

- ► Resolution
- ► **Accuracy**
- ► Quantization
- ► Missing Code

Question No: 25 (Marks: 1) - Please choose one



Above is the circuit diagram of _____.

- ► Asynchronous up-counter
- ► Asynchronous down-counter
- ► **Synchronous up-counter**
- ► Synchronous down-counter

Question No: 26 (Marks: 1) - Please choose one

The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► **2n (n multiplied by 2)**
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

Question No: 27 (Marks: 2)

Draw the Truth-Table of NOR based S-R Latch

input		output
S	**R**	**Q_{T+1}**
0	**0**	**Q_T**
0	**1**	**0**
1	**0**	**1**
1	**1**	**INVALID**

Question No: 28 (Marks: 2)

Two state assignments are given in the table below. Identify which state assignment is best and why?

States	State assignment 1	State assignment 2
A	**00**	**00**

B	**01**	**01**
C	**11**	**10**
D	**10**	**11**

Ans:
State assignment 2 is best assignment… it Minimizes the number of state variables that don't change in a group of related states

. **Question No: 29 (Marks: 2)**

Write down at least two functions of a register.

Ans:

1. **Registers are operating as a coherent unit to hold and generate data.**
2. **registers functions also include configuration and start-up of certain features, especially during initialization, bufferstorage e.g. video memory for graphics cards, input/output (I/O) of different kinds,**

Question No: 30 (Marks: 2)

Define quantization process.

Ans:
The process by which we can convert an analogue signal into digital signal (code) is known as quantization process.

Question No: 31 (Marks: 3)

How can we calculate the frequency of an unknown signal?

Ans:
The frequency of a particular event is accomplished by counting the number of times that event occurs within a specific time interval, then dividing the count by the length of the time interval.

Question No: 32 (Marks: 3)

Given the following statement used in PLD programming:
Y PIN 23 ISTYPE 'com';
Explain what does this statement mean?

Ans:
The Y variable is a 'Combinational' output available directly from the AND-OR gate array output. The active-low or active-high output of the Registered Mode can also be

specified in the declaration statement

Question No: 33 (Marks: 3)

Explain dynamic RAM in your own words.

Ans:

Dram use latch to store a single bit of information. The main drawback of it id the discharge of capacitor over a period of time. Here four gates are used in making a single latch. In terms of transistors, 4 to 6 transistors are required to implement a single storage cell. In order to build memories with higher densities, a single transistor is used to store a binary value. A single transistor can not store a binary value however it is used to charge and discharge a capacitor. The capacitor can not retain the charge, therefore it has to be periodically charged

Through a refresh cycle.

Question No: 34 (Marks: 5)

You are given the Next-state table of a moor machine, using this information draw the state diagram of the machine.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	1	1	1	1	1
1	1	1	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	1	0
1	1	0	0	1	1

Question No: 35 (Marks: 5)

Explain Memory Select or Enable Signals

Memory Select or Enable Signal:

There are more than one memory chips to store program

Information in daily use computers. read or write operation is carried out on a single addressable location instantaneously .

The unique location is accessed in one of the several memory chips, so single memory chips is selected before a read or write operation can be carried out. All memory chips have a chip enable or chip select signal which has to be activated before the memory can be accessed.

Question No: 36 (Marks: 5)

Performance characteristics of D/A converters are determined by five parameters. Name them.

Ans:

Performances characteristics of D/A converters are determined by five parameters

are as follow:

1. **Accuracy**
2. **Setting time**
3. **Monotonicity**
4. **Linearity**
5. **Resolution**

FINALTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design (Session - 1)

Time: 90 min
arks: 58

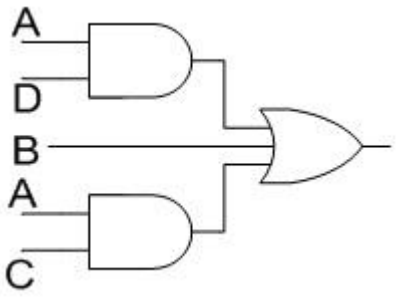
Question No: 1 (Marks: 1) - Please choose one

"A + B = B + A" is _____

- ► Demorgan's Law
- ► Distributive Law
- ► Commutative Law
- ► Associative Law

Question No: 2 (Marks: 1) - Please choose one

The diagram given below represents _____



- ► Demorgans law
- ► Associative law
- ► Product of sum form
- ► Sum of product form

Question No: 3 (Marks: 1) - Please choose one

Following is standard POS expression

$(A+\bar{B}+C+\bar{D})(A+\bar{B}+C+D)(A+B+\bar{C}+\bar{D})(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+D)$

- ► True
- ► False

Question No: 4 (Marks: 1) - Please choose one

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

- ► Using a single comparator
- ► Using Iterative Circuit based Comparators
- ► Connecting comparators in vertical hierarchy
- ► Extra logic gates are always required.

Question No: 5 (Marks: 1) - Please choose one

Demultiplexer is also called

- ► Data selector
- ► Data router
- ► Data distributor
- ► Data encoder

Question No: 6 (Marks: 1) - Please choose one

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► Doesn't have an invalid state
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 7 (Marks: 1) - Please choose one

A positive edge-triggered flip-flop changes its state when _____

- ► Low-to-high transition of clock
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 8 (Marks: 1) - Please choose one

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

- ► 10 mW
- ► 25 mW
- ► 64 mW
- ► 1024

Question No: 9 (Marks: 1) - Please choose one

_____ counters as the name indicates are not triggered simultaneously.

- ► Asynchronous
- ► Synchronous
- ► Positive-Edge triggered
- ► Negative-Edge triggered

Question No: 10 (Marks: 1) - Please choose one

74HC163 has two enable input pins which are _____ and _____

- ► ENP, ENT
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Question No: 11 (Marks: 1) - Please choose one

The divide-by-60 counter in digital clock is implemented by using two cascading

counters:

- ► Mod-6, Mod-10
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 12 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

- ► Current state and the inputs
- ► Current state and outputs
- ► Previous state and inputs
- ► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one

A synchronous decade counter will have _____ flip-flops

- ► 3
- ► 4
- ► 7
- ► 10

Question No: 14 (Marks: 1) - Please choose one

_____ is used to minimize the possible no. of states of a circuit.

- ► State assignment
- ► State reduction
- ► Next state table
- ► State diagram

Question No: 15 (Marks: 1) - Please choose one

A multiplexer with a register circuit converts _____

- ► Serial data to parallel
- ► Parallel data to serial
- ► Serial data to serial
- ► Parallel data to parallel

Question No: 16 (Marks: 1) - Please choose one

The alternate solution for a demultiplexer-register combination circuit is _____

- ► Parallel in / Serial out shift register
- ► Serial in / Parallel out shift register
- ► Parallel in / Parallel out shift register
- ► Serial in / Serial Out shift register

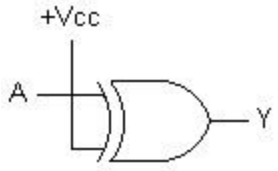
Question No: 17 (Marks: 1) - Please choose one

A GAL is essentially a _____.

- ► Non-reprogrammable PAL
- ► PAL that is programmed only by the manufacturer
- ► Very large PAL
- ► Reprogrammable PAL

Question No: 18 (Marks: 1) - Please choose one

The output of this circuit is always _____.



- ► 1
- ► 0
- ► A
- ►

Question No: 19 (Marks: 1) - Please choose one
DRAM stands for _____

- ► **Dynamic RAM**
- ► **Data RAM**
- ► **Demoduler RAM**
- ► **None of given options**

Question No: 20 (Marks: 1) - Please choose one
in _____, all the columns in the same row are either read or written.

- ► Sequential Access
- ► MOS Access
- ► FAST Mode Page Access
- ► None of given options

Question No: 21 (Marks: 1) - Please choose one
FIFO is an acronym for _____

- ► First In, First Out
- ► Fly in, Fly Out
- ► Fast in, Fast Out
- ► None of given options

Question No: 22 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► Fist In First Out Memory
- ► Flash Memory
- ► Fast Page Access Mode Memory

Question No: 23 (Marks: 1) - Please choose one
A frequency counter _____

- ► Counts pulse width

- ► Counts no. of clock pulses in 1 second
- ► Counts high and low range of given clock pulse
- ► None of given options

Question No: 24 (Marks: 1) - Please choose one

The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► 2n (n multiplied by 2)
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

Question No: 25 (Marks: 1) - Please choose one

Stack is an acronym for _____

- ► FIFO memory
- ► LIFO memory
- ► Flash Memory
- ► Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one

The 4-bit 2's complement representation of "+5" is _____

- ► 1010
- ► 1110
- ► 1011
- ► 0101

Question No: 27 (Marks: 2)

Explain the erase operation in context of Flash Memory.

Question No: 28 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer and 2-to-4 Binary Decoder?

Question No: 29 (Marks: 2)

Some of the counters (e.g. 74HC163) are called pre-set counters. why?

Question No: 30 (Marks: 2)

How many bytes will be there in 32 K x 8 memory?

Question No: 31 (Marks: 3)
Differentiate between truth table and next-state table

Question No: 32 (Marks: 3)
Name the three types of errors Analogue to Digital converters exhibit during their conversion operation.

Question No: 33 (Marks: 3)
How can a serial in/parallel out register be used as a serial in/serial out register?

Question No: 34 (Marks: 5)
Explain the implementation of First In First Out (FIFO) Memory by using RAM.

Question No: 35 (Marks: 5)
Explain memory read operation with the help of an example

Question No: 36 (Marks: 5)
Explain the next-state table with the help of a table for any sequential circuit

CS302-Digital Logic & Design

FINAL TERM Solved MCQS

Prepared by: JUNAID MALIK

AL-JUNAID TECH INSTITUTE

Question No: 1
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.
► Set-up time
► Hold time (Page 242)
► Pulse Interval time
► Pulse Stability time (PST)

Question No: 2
74HC163 has two enable input pins which are _____ and _____
► ENP, ENT (Page 285)
► ENI, ENC
► ENP, ENC
► ENT, ENI

Question No: 3
_____ is said to occur when multiple internal variables change due to change in one input variable
► Clock Skew
► Race condition (Page 267)
► Hold delay
► Hold and Wait

Question No: 4
The _____ input overrides the _____ input
► Asynchronous, synchronous (Page 369)
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 5
A decade counter is _____.
► Mod-3 counter
► Mod-5 counter
► Mod-8 counter
► Mod-10 counter (Page 274)

Question No: 6
In asynchronous transmission when the transmission line is idle, _____
► It is set to logic low
► It is set to logic high (Page 356)
► Remains in previous state
► State of transmission line is not used to start transmission

Question No: 7 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356)**

Question No: 8

In a sequential circuit the next state is determined by _____ and _____

► State variable, current state
► Current state, flip-flop output
► **Current state and external input (Page 318)**
► Input and clock signal applied

Question No: 9

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► **Mod-6, Mod-10 (Page 299)**
► Mod-50, Mod-10
► Mod-10, Mod-50
► Mod-50, Mod-6

Question No: 10

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

► **True (Page 221)**
► False

Question No: 11

A Nibble consists of _____ bits

► 2
► **4 (Page 394)**
► 8
► 16

Question No: 12

Excess-8 code assigns _____ to "-8"

► 1110
► 1100
► 1000
► **0000 (Page 34)**

Question No: 13

The voltage gain of the Inverting Amplifier is given by the relation _____

► **Vout / Vin = - Rf / Ri (Page 446)**
► Vout / Rf = - Vin / Ri
► Rf / Vin = - Ri / Vout
► Rf / Vin = Ri / Vout

Question No: 14
LUT is acronym for _____
► **Look Up Table (Page 439)**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 15
The three fundamental gates are _____
► AND, NAND, XOR
► OR, AND, NAND
► NOT, NOR, XOR
► **NOT, OR, AND (Page 40)**

Question No: 16
The total amount of memory that is supported by any digital system depends upon _____
► The organization of memory
► The structure of memory
► The size of decoding unit
► **The size of the address bus of the microprocessor (Page 430)**

Question No: 17
Stack is an acronym for _____
► FIFO memory
► **LIFO memory (Page 429)**
► Flash Memory
► Bust Flash Memory

Question No: 18
Addition of two octal numbers "36" and "71" results in _____
► 213
► 123
► **127**
► 345

Question No: 19
_____ is one of the examples of synchronous inputs.
► **J-K input (Page 235)**
► EN input
► Preset input (PRE)
► Clear Input (CLR)

Question No: 20
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
► Race condition
► **Clock Skew (Page 226)**

► Ripple Effect
► None of given options

Question No: 22
In a state diagram, the transition from a current state to the next state is determined by
► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 23
_____ is used to simplify the circuit that determines the next state.
► State diagram
► Next state table
► State reduction
► **State assignment (Page 335)**

Question No: 24
Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. Wha will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)
► 1100
► 0011
► 0000
► 1111

Question No: 25
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____
► **Doesn't have an invalid state (Page 232)**
► Sets to clear when both J = 0 and K = 0
► It does not show transition on change in pulse
► It does not accept asynchronous inputs

Question No: 26
A multiplexer with a register circuit converts _____
► Serial data to parallel
► **Parallel data to serial (Page 356)**
► Serial data to serial
► Parallel data to parallel

Question No: 27
GAL is essentially a _____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183)**

Question No: 28
in _____, all the columns in the same row are either read or written.
► Sequential Access
► MOS Access
► **FAST Mode Page Access (Page 413)**
► None of given options

Question No: 29
In order to synchronize two devices that consume and produce data at different rates, we can use _____
► Read Only Memory
► **Fist In First Out Memory (Page 425)**
► Flash Memory
► Fast Page Access Mode Memory

Question No: 30
A flip-flop changes its state when _____
► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 31
A frequency counter _____
► Counts pulse width
► **Counts no. of clock pulses in 1 second (Page 301)**
► Counts high and low range of given clock pulse
► None of given options

Question No: 32
In a sequential circuit the next state is determined by _____ and _____
► State variable, current state
► Current state, flip-flop output
► Current state and external input
► **Input and clock signal applied (Page 305)**

Question No: 33
Flip flops are also called _____
► Bi-stable dualvibrators
► Bi-stable transformer
► **Bi-stable multivibrators (Page 228)**
► Bi-stable singlevibrators

Question No: 36

Given the state diagram of an up/down counter, we can find _____

► **The next state of a given present state (Page 371)**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

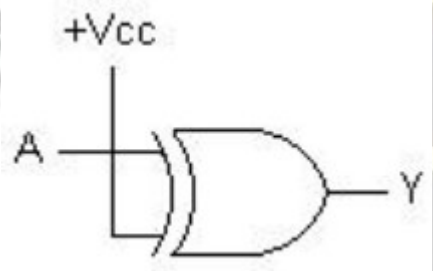
Question No: 38

A Nibble consists of _____ bits

► 2
► **4 (Page 394)**
► 8
► 16

Question No: 39

The output of this circuit is always _____.



► 1
► 0
► A
► $\overline{A}$

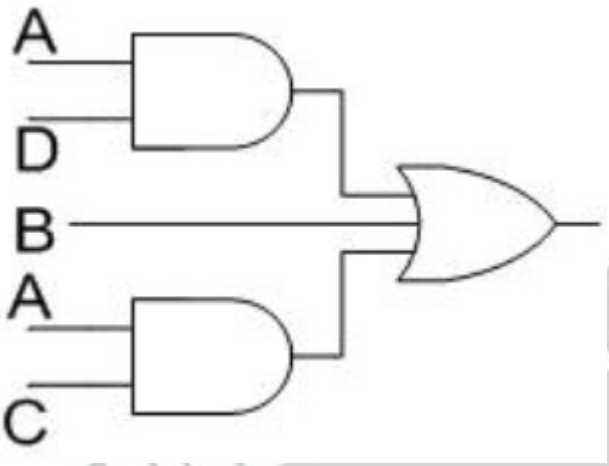
Question No: 40

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► **two AND gates, one OR gate, two inverters (Lecture 8)**
► two AND gates, one OR gate

Question No: 41

The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78)**

Question No: 42
The voltage gain of the Inverting Amplifier is given by the relation _____
► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
► $V_{out} / R_f = - V_{in} / R_i$
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / V_{out}$

Question No: 43
DRAM stands for _____
► **Dynamic RAM (Page 407)**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 44
The three fundamental gates are _____
► AND, NAND, XOR
► OR, AND, NAND
► NOT, NOR, XOR
► **NOT, OR, AND (Page 40)**

Question No: 45

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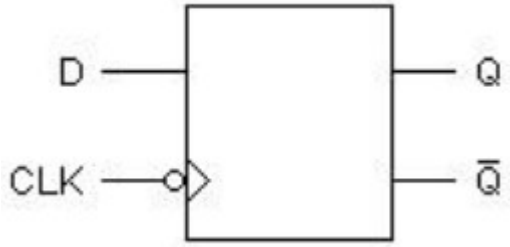


Which of the following statement is true regarding above block diagram?
► Triggering takes place on the negative-going edge of the CLK pulse
► Triggering takes place on the positive-going edge of the CLK pulse
► Triggering can take place anytime during the HIGH level of the CLK waveform
► Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 46
The expression F=A+B+C describes the operation of three bits _____ Gate.
► OR (Page 42)
► AND
► NOT
► NAND

Question No: 47
Addition of two octal numbers "36" and "71" results in _____
► 213
► 123
► 127
► 345

Question No: 48
The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.
► 8-bit
► 16-bit
► 32-bit (Page 25)
► 64-bit

Question No: 49
The decimal "17" in BCD will be represented as _____
► 11101
► 11011
► 10111 (According to rule)
► 11110

Question No: 50
The basic building block for a logical circuit is _____
► A Flip-Flop
► A Logical Gate (Page 7)
► An Adder
► None of given options

Question No: 51
The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.
► Undefined
► One
► Zero (According to rule)
► No Output as input is invalid.

Question No: 52
_____ is invalid number of cells in a single group formed by the adjacent cells in K-map
► 2
► 8
► 12 (According to rule "2^n")
► 16

Question No: 53
The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.
► AND (Page 182)
► OR
► NOT
► XOR

Question No: 54
_____ is one of the examples of asynchronous inputs. ► J-K input
► S-R input
► D input

► Clear Input (CLR) (Page 235)

Question No: 55
Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____
► 0000
► 1101 (not sure)
► 1011
► 1111

Question No: 56

In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 232)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 57

_____ is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341)**
► State reduction
► Next state table
► State diagram

Question No: 59

The best state assignment tends to _____.

► **Maximizes the number of state variables that don't change in a group of related states (Page 337)**
► Minimizes the number of state variables that don't change in a group of related states
► Minimize the equivalent states
► None of given options

Question No: 60

5-bit Johnson counter sequences through ____ states

► 7
► **10 (Page 354)**
► 32
► 25

Question No: 61

The address from which the data is read, is provided by _____

► Depends on circuitry
► None of given options
► RAM
► **Microprocessor (Page 397)**

Question No: 62

FIFO is an acronym for _____

► **First In, First Out (Page 424)**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 63

The voltage gain of the Inverting Amplifier is given by the relation _____

► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**

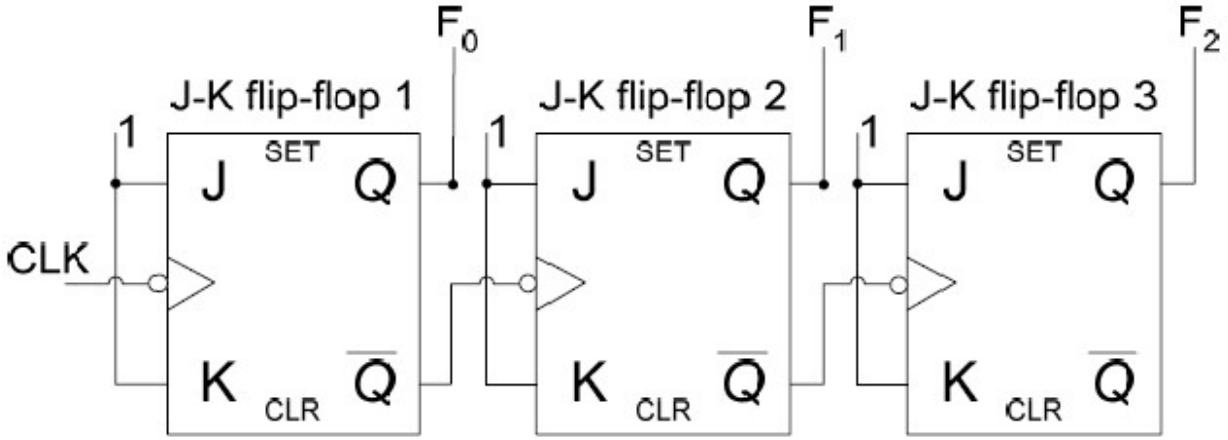
► $V_{out} / R_f = - V_{in} / R_i$
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / V_{out}$

Question No: 64

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expecte output.

► Resolution
► **Accuracy (Page 460)**
► Quantization
► Missing Code

Question No: 65



Above is the circuit diagram of _____.

► **Asynchronous up-counter (Page 270)**
► Asynchronous down-counter
► Synchronous up-counter
► Synchronous down-counter

Question No: 66

The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354)**
► 2^n (2 raise to power n)
► n^2 (n raise to power 2)

Question No: 67

"A + B = B + A" is _____

► Demorgan‟s Law
► Distributive Law
► **Commutative Law (Page 72)**
► Associative Law

Question No: 68

Following is standard POS expression

$$(A+\bar{B}+C+\bar{D})(A+\bar{B}+C+D)(A+B+\bar{C}+\bar{D})(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+D)$$

► **True (Lecture 9)**

► False

Question No: 69

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

► Using a single comparator

► **Using Iterative Circuit based Comparators (Page 155)**

► Connecting comparators in vertical hierarchy

► Extra logic gates are always required.

Question No: 70

DE multiplexer is also called

► Data selector

► Data router

► **Data distributor (Page 178)**

► Data encoder

Question No: 71

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW

► **25 mW (Page 242)**

► 64 mW

► 1024

Question No: 72

_____ Counters as the name indicates are not triggered simultaneously.

► **Asynchronous (Page 269)**

► Synchronous

► Positive-Edge triggered

► Negative-Edge triggered

Question No: 74
In a state diagram, the transition from a current state to the next state is determined by
► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 75
A synchronous decade counter will have _____ flip-flops
► 3
► **4 (Page 281)**
► 7
► 10

Question No: 76
The alternate solution for a demultiplexer-register combination circuit is _____
► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356)**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 77
The 4-bit 2‟s complement representation of “+5” is _____
► 1010
► 1110
► 1011
► **0101 (Page 22)**

Question No: 78
The storage cell in SRAM is
► a flip –flop
► **a capacitor (Page 407)**
► a fuse
► a magnetic domain

Question No: 79
What is the difference between a D latch and a D flip-flop?
► The D latch has a clock input.
► The D flip-flop has an enable input.
► The D latch is used for faster operation.
► **The D flip-flop has a clock input.**

Question No: 80

For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs Will _____ if the clock goes HIGH.

► **toggle**
► set
► reset
► not change

Question No: 81

The OR gate performs Boolean _____.

► multiplication
► subtraction
► division
► **addition (Page 42)**

Question No: 82

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

► **set (Page 219)**
► reset
► invalid
► clear

Question No: 83

Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.

► A = 1, B = 0, C = 0, D = 0
► **A = 1, B = 0, C = 1, D = 0 (Lecture 8)**
► A = 0, B = 1, C = 0, D = 0
► A = 1, B = 0, C = 1, D = 1

Question No: 84

The power dissipation, *P*D, of a logic gate is the product of the

► **dc supply voltage and the peak current**
► dc supply voltage and the average supply current
► ac supply voltage and the peak current
► ac supply voltage and the average supply current

Question No: 85

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

►**True**
►False

Question No:86

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

►**True (Page 50)**
►False

Question No: 87

Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

►A parallel to serial converter circuit (Page 244)

►A counter circuit

►A BCD to Decimal decoder

►A 2-to-8 bit decoder

Question No: 88

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

►4

►8 (Page 89)

►12

►16

Question No: 89

In designing any counter the transition from a current state to the next sate is determined by

►Current state and inputs (Page 332)

►Only inputs

►Only current state

►current state and outputs

Question No: 90

Sum term (Max term) is implemented using _____ gates

►OR (Page 78)

►AND

►NOT

►OR-AND

Question No: 91

AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

►2

►4

►6

►8 (not sure)

Question No: 93

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

►0

►1 (Page 230)

►Invalid

►Input is invalid

Question No: 94

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

► 0

► 1

► Invalid (Page 233)

► Input is invalid

Question No: 95

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help l

_____

►Using S-R Flop-Flop
►D-flipflop
►J-K flip-flop (Page 252)
►T-Flip-Flop

Question No: 96

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

►3
►7
►8 (Page 272)
►15

Question No: 97

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

►Moore machine
►Meally machine
►Johnson counter
►Ring counter (Page 355)

Question No: 98

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

►Write Time
►Recycle Time
►Refresh Time
►Access Time (Page 417)

Question No: 99

Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state

►Ten
►Eight
►Three
►Two (Page 262)

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Question No: 101

A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?

►= 0, Cout = 0

►= 0, Cout = 1 (Page 135)

►= 1, Cout = 0

►= 1, Cout = 1

Question No: 102

THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

►GATED FLIP-FLOPS

►PULSE TRIGGERED FLIP-FLOPS

►POSITIVE-EDGE TRIGGERED FLIP-FLOPS

►NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267)

Question No: 103

The design and implementation of synchronous counters start from _____

► Truth table

► k-map

► state table

► state diagram (Page 319)

Question No: 104

THE HOURS COUNTER IS IMPLEMENTED USING _____

►ONLY A SINGLE MOD-12 COUNTER IS REQUIRED

►MOD-10 AND MOD-6 COUNTERS

►MOD-10 AND MOD-2 COUNTERS

►A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299)

Question No: 105 (Marks: 1) - Please choose one

The high density FLASH memory cell is implemented using _____

►1 floating-gate MOS transistor (Page 419)

►2 floating-gate MOS transistors

►4 floating-gate MOS transistors

►6 floating-gate MOS transistors

Question No: 106 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

►Q2:= Q1 $ X $ Q3

►Q2:= Q1 # X # Q3 (Page 210)

►Q2:= Q1 & X & Q3

►Q2:= Q1 ! X ! Q3

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Question No: 107

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

►TTL (Page 65)

►CMOS 3.5 series

►CMOS 5 Series

►Power dissipation of all circuits increases with time.

Question No: 108

When the control line in tri-state buffer is high the buffer operates like a _____gate

►AND

►OR

►NOT (Page 196)

►XOR

Question No: 109

3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

►Low switching speeds, high power dissipation

►Fast switching speeds, high power dissipation

►Fast switching speeds, very low power dissipation (Page 61)

►Low switching speeds, very low power dissipation

Question No:110

The output of an AND gate is one when _____

► All of the inputs are one (Page 40)

► Any of the input is one

► Any of the input is zero

► All the inputs are zero

Question No: 111

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1

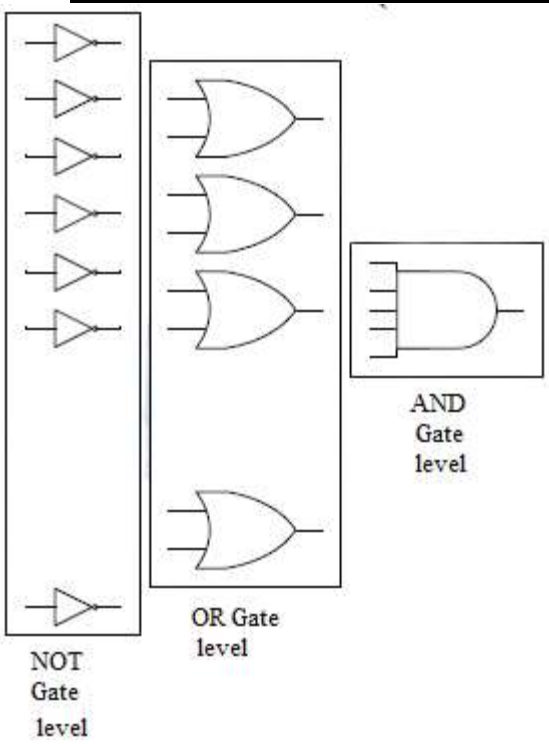
► A > B = 0, A < B = 1, A = B = 0

► A > B = 1, A < B = 0, A = B = 0 (Page 109)

► A > B = 0, A < B = 1, A = B = 1

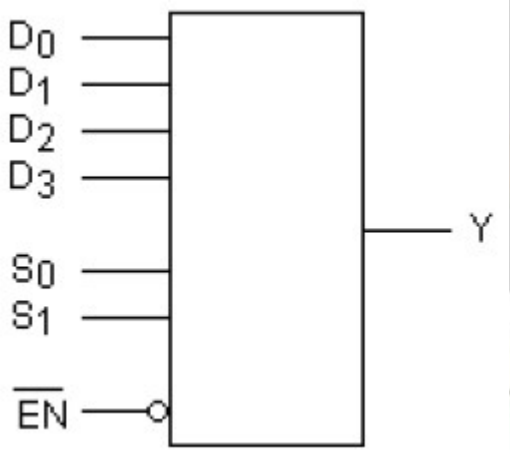
Question No:112

The diagram above shows the general implementation of _____ form



► boolean
► arbitrary
► **POS (Page 122)**
► SOP

Question No: 113
The device shown here is most likely a



► Comparator
► Multiplexer
► Demultiplexer
► Parity generator

Question No: 114

DE multiplexer converts _____ data to _____ data

► Parallel data, serial data
► **Serial data, parallel data (Page 356)**
► Encoded data, decoded data
► All of the given options.

Question No:115

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

Question No: 116

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

► 0
► 1
► **Invalid (Page 230)**
► Input is invalid

Question No: 119

In asynchronous digital systems all the circuits change their state with respect to a common clock

► True
► **False (Page 245)**

Question No: 201

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW
► **25 mW (Page 242)**
► 64 mW
► 1024

Question No: 202

A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

► 10 Hz
► **50 Hz (Page 298)**
► 100 Hz
► 500 Hz

Question No: 203
The design and implementation of synchronous counters start from _____
► Truth table
► k-map
► state table
► **state diagram (Page 319)**

Question No: 204
In _____ the output of the last flip-flop of the shift register is connected to the data input of the first flip-flop. ► Moore machine
► Meally machine
► **Johnson counter (Page 354)**
► Ring counter Q

Question No: 205
Which is not characteristic of a shift register?
► **Serial in/parallel in (Page 346)**
► Serial in/parallel out
► Parallel in/serial out
► Parallel in/parallel out

Question No:206
NOR Gate can be used to perform the operation of AND, OR and NOT Gate
► FALSE
► **TRUE (Page 250)**

Question No: 207
The output of an XNOR gate is 1 when _____ I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one
► I Only
► IV Only
► I and IV only
► **II and III only (Page 53)**

Question No: 208
NAND gate is formed by connecting _____
► **AND Gate and then NOT Gate (Page 45)**
► NOT Gate and then AND Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 209

Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

► Zero

► **One (Page 46)**

► Undefined

► No output as input is invalid

Question No: 210

The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____

► Radiation-Erase programming method (REPM)

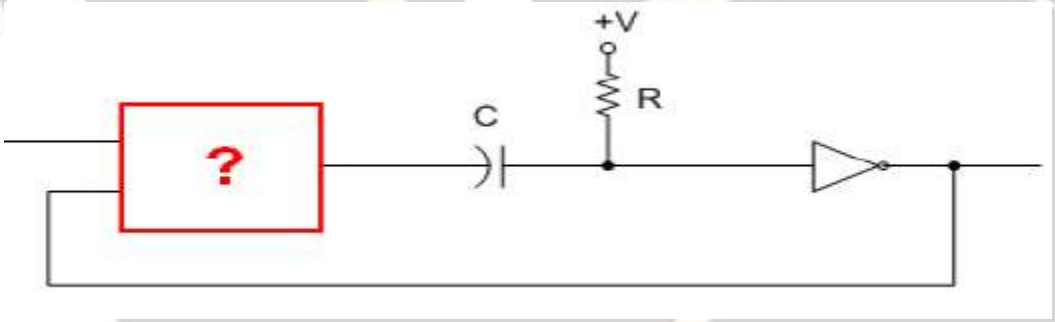
► **In-System Programming (ISP) (Page 194)**

► In-chip Programming (ICP)

► Electronically-Erase programming method(EEPM)

Question No: 211

Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.



► AND

► NAND

► NOR

► **XNOR (Page 262)**

Question No: 212

In _____ outputs depend only on the combination of current state and inputs.

► **Mealy machine (Page 332)**

► Moore Machine

► State Reduction table

► State Assignment table

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Question No: 213
In the following statement Z PIN 20 ISTYPE „reg.invert“;
The keyword “reg.invert” indicates _____
► An inverted register input
► An inverted register input at pin 20
► Active-high Registered Mode output
► **Active-low Registered Mode output (Page 360)**

Question No: 214
A Nibble consists of _____ bits
► 2
► **4 (Page 394)**
► 8
► 16

Question No: 215
A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.
► 1110
► 0111
► 1000
► **1001**

Question No: 216
In order to synchronize two devices that consume and produce data at different rates, we can use _____
► Read Only Memory
► **Fist In First Out Memory (Page 425)**
► Flash Memory
► Fast Page Access Mode Memory

Question No: 217
If the FIFO Memory output is already filled with data then _____
► It is locked; no data is allowed to enter
► It is not locked; the new data overwrites the previous data.
► Previous data is swapped out of memory and new data enters
► **None of given options**

Question No: 218
The process of converting the analogue signal into a digital representation (code) is known as _____
► Strobing
► Amplification
► **Quantization (Page 445)**
► Digitization

Question No: 219

$(A+B)(A+\overline{B}+C)(\overline{A}+C)$

is an example of _____

► **Product of sum form (Page 77)**
► Sum of product form
► Demorgans law
► Associative law

Question No: 220

Q2 :=Q1 OR X OR Q3 The above ABEL expression will be

► Q2:= Q1 $ X $ Q3
► **Q2:= Q1 # X # Q3 (Page 210)**
► Q2:= Q1 & X & Q3
► Q2:= Q1 ! X ! Q3

Question No: 221

Caveman number system is Base _____ number system ► 2

► **5 (Page 11)**
► 10
► 16

Question No: 222

The output of an XOR gate is zero (0) when _____

I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

► I Only
► IV Only
► **I and IV only (Page 53)**
► II and III only

Question No: 223

The simplest and most commonly used Decoders are the _____ Decoders

► **n to 2n (Page 158)**
► (n-1) to 2n
► (n-1) to (2n-1)
► n to 2n-1

Question No: 224
The _____ Encoder is used as a keypad encoder.
► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► Decimal-to-BCD Priority (Page 166)

Question No: 225
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions
► True (Page 161)
► False

Question No: 226
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop
► 0
► 1 (Page 230)
► Invalid
► Input is invalid

Question No: 227
If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)
► AND
► OR
► NOT (Page 226)
► XOR

Question No: 228
The low to high or high to low transition of the clock is considered to be a(n) _____
► State
► Edge (Page 228)
► Trigger
► One-shot

Question No: 230
RCO Stands for _____
► Reconfiguration Counter Output
► Reconfiguration Clock Output
► Ripple Counter Output
► Ripple Clock Output (Page 285)

Question No: 231
A transparent mode means _____
► The changes in the data at the inputs of the latch are seen at the output (Page 245)
► The changes in the data at the inputs of the latch are not seen at the output
► Propagation Delay is zero (Output is immediately changed when clock signal is applied)
► Input Hold time is zero (no need to maintain input after clock transition)

Question No: 232
In _____ outputs depend only on the current state.
► Mealy machine
► **Moore Machine (Page 332)**
► State Reduction table
► State Assignment table

Question No: 233
Smallest unit of binary data is a _____
► **Bit (Page 394)**
► Nibble
► Byte
► Word

Question No: 234
NOR gate is formed by connecting _____
► **OR Gate and then NOT Gate (Page 47)**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 235
A particular half adder has
► 2 INPUTS AND 1 OUTPUT
► **2 INPUTS AND 2 OUTPUT (Page 134)**
► 3 INPUTS AND 1 OUTPUT
► 3 INPUTS AND 2 OUTPUT

Question No: 236
THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____ GATE
► AND
► **OR (Page 171)**
► NAND
► XOR

Question No: 237
A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BY THE MANUFACTURER.
► **TRUE (Page 182)**
► FALSE

Question No: 241
A synchronous decade counter will have _____ flip-flops
► 3
► **4 (Page 281)**
► 7

► 10

Question No: 242

The alternate solution for a multiplexer and a register circuit is _____

►Parallel in / Serial out shift register (Page 356)

►Serial in / Parallel out shift register

►Parallel in / Parallel out shift register

►Serial in / Serial Out shift register

Question No: 243

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1

► 2

► 4

► 8 (Page 356)

Question No: 245

If the FIFO Memory output is already filled with data then _____

► It is locked; no data is allowed to enter

► It is not locked; the new data overwrites the previous data.

► Previous data is swapped out of memory and new data enters

► None of given options

Question No: 246

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO ------

► THE FLOP-FLOP IS TRIGGERED

► Q=0 AND Q‟=1

► Q=1 AND Q‟=0

► THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED (page 223)

Question No: 247

The terminal count of a 4-bit binary counter in the UP mode is____.

- 1100
- 0011
- 1111
- 0000

Question No: 248

For a down counter that counts from (111 to 000). If current state is "101" the next state willbe ____.

- 111
- 110
- 010
- None of given options

Question No: 249

The n flip-flops store_____states.

a. 1

b.

2^n

c. 0

d. 2^(n+1)

Question No: 250

An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting _____.

- Q output of all flip-flops to clock input of next flip-flops
- Q' output of all flip-flops to clock input of next flip-flops
- Q output of all flip-flops to J input of next flip-flops
- Q' output of all flip-flops to K input of next flip-flops

Question No: 251

In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together.

- True
- False

Question No: 251

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

a.True

b.False

Question No: 252

The 74HC163 is a 4-bit Synchronous Counter, it has_____data output pins.

b. 2

b. 4

c. 6

d. 8

Question No: 253

Divide-by-32 counter can be achieved by using

c. Flip-Flop and DIV10b. Flip-Flop and DIV 16

c. Flip-Flop and DIV 32

d. DIV 16 and DIV 32

Question No: 254

The synchronous counters are also known as Ripple Counters:

a.True

b False

Question No: 255

Each stage of Master-slave flip-flop works at_____of the clock signal

- Each stage works on complete clock signal
- One fourth
- One third
- One half

Question No: 256

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

`

a. 80 micro seconds

b. 8 micro seconds

c. 80 mili seconds

d. 10 micro seconds

Question No: 257

Number of states in an 8-bit Johnson counter sequence are:

d. 8

e. 12

f. 14

g. 16

Question No: 258

In moore machine the output depends on

- The current state and the output of previous flip flop
- Only inputs
- The current state
- The current state and inputs

Question No: 259

Asynchronous mean that _____

- Each flip-flop after the first one is enabled by the output of the preceding flip-flop
- Each flip-flop is enabled by the output of the preceding flip-flop
- Each flip-flop except the last one is enabled by the output of the preceding flip-flop
- Each alternative flip-flop after the first one is enabled by the output of the precedingflip-flop

Question No: 260

According to moore circuit, the output of synchronous sequential circuit depend/s on _____of flip flop.

h. Previous state

i. Present state

j. Next state

k. External state

Question No: 261

In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

- Q
- 0
- 1
- Invalid

Question No: 262

A Divide-by-20 counter can be achieved by using

a. Flip-Flop and DIV 10
b. Flip-Flop and DIV 16
c. Flip-Flop and DIV 32
d. DIV 10 and DIV 16

Question No: 263

A one-shot mono-stable device contains_____

- AND gate, Resistor, Capacitor and NOT Gate
- NAND gate, Resistor, Capacitor and NOT Gate
- NOR gate, Resistor, Capacitor and NOT Gate
- XNOR gate, Resistor, Capacitor and NOT Gate

Question No: 264

The_inputs can be directly mapped to karnaugh maps.

- S-R
- J-K
- Flip-Flop
- External

Question No: 265

A mono-stable device only has a single stable state

a. True
b. False

Question No: 266

When the_____Hz sampling interval is selected, the signal at the output of the J-K flip-flophas a time period of_____seconds.

a. 1, 2
b. 0, 2
c. 2, 5
d. 1, 1

Question No: 267

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to_____.

- Set
- Toggle

- Latch
- Reset

Question No: 268

A stage in the shift register consists of

- A latch
- A flip flop
- A byte of storage
- Four bits of storage

Question No: 269

If a circuit suffers "Clock Skew" problem, the output of circuit can't be guarantied.

a. True
b. False

Question No: 270

A modulus-14 counter has fourteen states requiring _____

l. 14 flip flops
m. 14 registers
c. 4 flip flops
d. 4 registers

Question No: 271

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using_____gate.

- AND
- OR
- NOT
- NAND

Question No: 272

_____flip-flops are obsolete now.

- Edge-triggered
- Master-Slave
- T-flipflop
- D-flipflop

Question No: 273

The glitches due to "Race Condition" can be avoided by using a_____.

n. Gated flip-flops
o. Pulse triggered flip-flops
p. Positive-Edge triggered flip-flops
d. Negative-Edge triggered flip-flops

Question No: 274

For a gated D-Latch if EN=1 and D=1 then Q(t+1)=_____

- 0
- Q(t)

- 1
- Invalid

Question No: 275

____occurs when the same clock signal arrives at different times at different clockinputs due to propagation delay.

q. Race condition
b. Clock skew
c. Ripple effect
d. None of given options

Question No: 276

An Astable multivibrator is known as a (n)_____.

a. Oscillator
b. Booster
c. One-shot
d. Dual-shot

Question No: 277

In Master-Slave flip-flop setup, the master flip-flop operators at _____

- Positive half cycle of pulse
- Negative half cycle of pulse
- Both Master-Slave operator simultaneously
- Master-Slave flip-flop does not operate on pulses rather it is edge triggered

Question No: 278

The power consumed by a flip-flop is defined by _____

- P = Icc x Rcc
- P=vcc x Rcc

o c.P = Vcc x Icc
o P = Mcc x Vcc

Question No: 279

The 3-bit up counter can be implemented using_____flip-flop(s).

- S-R flip-flops only
- S-R flip-flops and D-flip-flops
- S-R flip-flops or D-flip-flops
- D-flip-flop only

Question No: 280

The terminal count of a 4-bit binary counter in the DOWN mode is _____

a. 0000
b. 0011
c. 1100
d. 1111

Question No: 281

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

- State reduction
- State minimization

State assignment

- State evaluation

Question No: 282

State of flip-flop can be switched by changing its _____

a. Input signal
b. Output signal
c. Momentary signal
d. Contemporary signal

Question No: 283

Once the state diagram is drawn for any sequential circuit the next step is to draw

- Transiation table
- Karnaugh map
- Next-state table
- Logic expression

Question No: 284

Design of state diagram is one of many steps used to design

- A clock
- A truncated counter
- An UP/DOWN counter
- Any counter

Question No: 285

Flip flops are also called _____

- Bi-stable multivibrators
- Bi-stable singlevibrators
- Bi-stable dualvibrators
- Bi-stable transformer

Question No: 286

Three cascaded modulus-10 counters have an overall modulus of

- 30
- b. 100
- c. 1000
- 10000

Question No: 287

The term hold always means_____.

a. Q=0, Q'=1
b. Q=1, Q'=0
c. Q=0, Q'=0
d. No change

Question No: 288

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?

a. J=1, K=0
b. J=1,K=X(Don'tcare)
c. J=X(Don'tcare),K=0
d. J=0, K=X(Don't care)

Question No: 289

To parallel load a byte of data into a shift register, there must be

a. One clock pulse
b. One clock pulse for each 1 in the data
c. Eight clock pulse
d. One clock pulse for each 0 in the data

Question No: 290

Invalid state of NOR based SR latch occurs when _____.

r. S=0, R=0
s. S=0, R=1
t. S=1, R=0
u. S=1, R=1

FINALTERM EXAMINATION
Spring 2011

Question No: 1 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356)**

Question No: 2 (Marks: 1) - Please choose one
In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► **Current state and external input (Page 318)**
- ► Input and clock signal applied

Question No: 3 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► **Mod-6, Mod-10 (Page 299)**
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 4 (Marks: 1) - Please choose one
In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► **True (Page 221)**
- ► False

Question No: 5 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242)**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 6 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

- ► **ENP, ENT (Page 285)**
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Question No: 7 (Marks: 1) - Please choose one
_____ is said to occur when multiple internal variables change due to change in one input variable

- ► Clock Skew
- ► **Race condition (Page 267)**
- ► Hold delay
- ► Hold and Wait

Question No: 8 (Marks: 1) - Please choose one
The _____ input overrides the _____ input

- ► **Asynchronous, synchronous (Page 369)**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 9 (Marks: 1) - Please choose one
A decade counter is _____.

- ► Mod-3 counter
- ► Mod-5 counter
- ► Mod-8 counter
- ► **Mod-10 counter (Page 274)**

Question No: 10 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

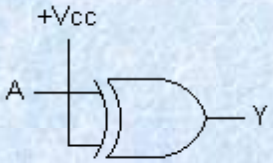
- ► It is set to logic low
- ► **It is set to logic high (Page 356)**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 11 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- ► 2
- ► **4 (Page 394)**
- ► 8
- ► 16

Question No: 12 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A** **Click here for detail**
- ► $\overline{A}$

Question No: 13 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "-8"

- ► 1110
- ► 1100
- ► 1000
- ► **0000 (Page 34)**

Question No: 14 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

- ► **Vout / Vin = - Rf / Ri (Page 446)**
- ► Vout / Rf = - Vin / Ri
- ► Rf / Vin = - Ri / Vout
- ► Rf / Vin = Ri / Vout

Question No: 15 (Marks: 1) - Please choose one
LUT is acronym for _____

- ► **Look Up Table (Page 439)**
- ► Local User Terminal
- ► Least Upper Time Period
- ► None of given options

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 16 (Marks: 1) - Please choose one
The three fundamental gates are _____

- ► AND, NAND, XOR
- ► OR, AND, NAND
- ► NOT, NOR, XOR
- ► **NOT, OR, AND (Page 40)**

Question No: 17 (Marks: 1) - Please choose one
The total amount of memory that is supported by any digital system depends upon _____

- ► The organization of memory
- ► The structure of memory
- ► The size of decoding unit
- ► **The size of the address bus of the microprocessor (Page 430)**

Question No: 18 (Marks: 1) - Please choose one
Stack is an acronym for _____

- ► FIFO memory
- ► **LIFO memory (Page 429)**
- ► Flash Memory
- ► Bust Flash Memory

Question No: 19 (Marks: 1) - Please choose one
Addition of two octal numbers "36" and "71" results in _____

- ► 213
- ► 123
- ► **127**
- ► 345

Question No: 20 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

- ► **J-K input (Page 235)**
- ► EN input
- ► Preset input (PRE)
- ► Clear Input (CLR)

Question No: 21 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

- ► Race condition
- ► **Clock Skew (Page 226)**
- ► Ripple Effect
- ► None of given options

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 22 (Marks: 1) - Please choose one

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

- ► 0000
- ► **1101 (not sure)**
- ► 1011
- ► 1111

Question No: 23 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

- ► **Current state and the inputs (Page 332)**
- ► Current state and outputs
- ► Previous state and inputs
- ► Previous state and outputs

Question No: 24 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

- ► State diagram
- ► Next state table
- ► State reduction
- ► **State assignment (Page 335)**

Question No: 25 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356) rep**

Question No: 26 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

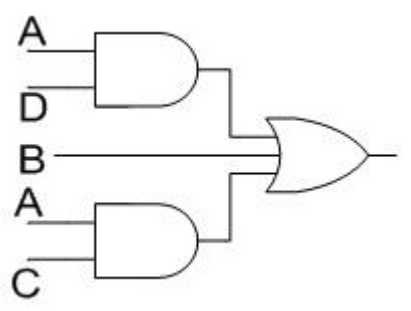
- ► 1100
- ► 0011
- ► **0000** Click here for detail
- ► 1111

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 27 (Marks: 1) - Please choose one
LUT is acronym for _____

► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

. **Question No: 28 (Marks: 1) - Please choose one**
The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78)**

Question No: 29 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

► **Doesn't have an invalid state (Page 232)**
► Sets to clear when both J = 0 and K = 0
► It does not show transition on change in pulse
► It does not accept asynchronous inputs

Question No: 30 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 31 (Marks: 1) - Please choose one
A GAL is essentially a _____.

► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183)**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 32 (Marks: 1) - Please choose one
in _____, all the columns in the same row are either read or written.

- ► Sequential Access
- ► MOS Access
- ► **FAST Mode Page Access (Page 413)**
- ► None of given options

Question No: 33 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► **Fist In First Out Memory (Page 425)**
- ► Flash Memory
- ► Fast Page Access Mode Memory

Question No: 34 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228)**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

FINALTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356) rep**

Question No: 2 (Marks: 1) - Please choose one
A frequency counter _____

- ► Counts pulse width
- ► **Counts no. of clock pulses in 1 second (Page 301)**
- ► Counts high and low range of given clock pulse
- ► None of given options

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 3 (Marks: 1) - Please choose one
In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► Current state and external input
- ► **Input and clock signal applied (Page 305)**

Question No: 4 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► **Mod-6, Mod-10 (Page 229) rep**
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 5 (Marks: 1) - Please choose one
In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► **True (Page 221) rep**
- ► False

Question No: 6 (Marks: 1) - Please choose one
Flip flops are also called _____

- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► **Bi-stable multivibrators (Page 228)**
- ► Bi-stable singlevibrators

Question No: 7 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242) rep**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 8 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

- ► **ENP, ENT (Page 285)**
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 9 (Marks: 1) - Please choose one

_____ is said to occur when multiple internal variables change due to change in one input variable

- ► Clock Skew
- ► **Race condition (Page 267)**
- ► Hold delay
- ► Hold and Wait

Question No: 10 (Marks: 1) - Please choose one

Given the state diagram of an up/down counter, we can find _____

- ► **The next state of a given present state (Page 371)**
- ► The previous state of a given present state
- ► Both the next and previous states of a given state
- ► The state diagram shows only the inputs/outputs of a given states

Question No: 11 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

- ► **Asynchronous, synchronous (Page 369) rep**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 12 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

- ► two AND gates, two OR gates, two inverters
- ► three AND gates, two OR gates, one inverter
- ► **two AND gates, one OR gate, two inverters (Lecture 8)**
- ► two AND gates, one OR gate

Question No: 13 (Marks: 1) - Please choose one

A decade counter is _____.

- ► Mod-3 counter
- ► Mod-5 counter
- ► Mod-8 counter
- ► **Mod-10 counter (Page 274)**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

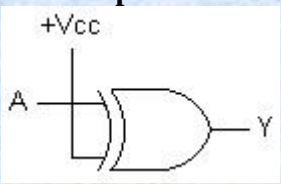
Question No: 14 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

- ► It is set to logic low
- ► **It is set to logic high (Page 356) rep**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

Question No: 15 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- ► 2
- ► **4 (Page 394)**
- ► 8
- ► 16

Question No: 16 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A** **Click here for detail** **rep**
- ► $\overline{A}$

Question No: 17 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "-8"

- ► 1110
- ► 1100
- ► 1000
- ► **0000 (Page 34) rep**

Question No: 18 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

- ► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
- ► $V_{out} / R_f = - V_{in} / R_i$
- ► $R_f / V_{in} = - R_i / V_{out}$
- ► $R_f / V_{in} = R_i / V_{out}$

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 19 (Marks: 1) - Please choose one
LUT is acronym for _____

- **Look Up Table (Page 439) rep**
- Local User Terminal
- Least Upper Time Period
- None of given options

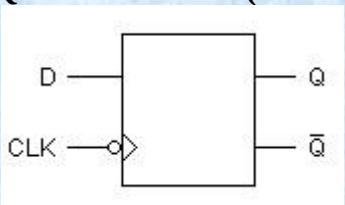
Question No: 20 (Marks: 1) - Please choose one
DRAM stands for _____

- **Dynamic RAM (Page 407)**
- Data RAM
- Demoduler RAM
- None of given options

Question No: 21 (Marks: 1) - Please choose one
The three fundamental gates are _____

- AND, NAND, XOR
- OR, AND, NAND
- NOT, NOR, XOR
- **NOT, OR, AND (Page 40)**

Question No: 22 (Marks: 1) - Please choose one



Which of the following statement is true regarding above block diagram?

- Triggering takes place on the negative-going edge of the CLK pulse
- Triggering takes place on the positive-going edge of the CLK pulse
- Triggering can take place anytime during the HIGH level of the CLK waveform
- Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 23 (Marks: 1) - Please choose one
The total amount of memory that is supported by any digital system depends upon _____

- The organization of memory
- The structure of memory
- The size of decoding unit
- **The size of the address bus of the microprocessor (Page 430) rep**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 24 (Marks: 1) - Please choose one
The expression F=A+B+C describes the operation of three bits _____ Gate.

► **OR (Page 42)**
► AND
► NOT
► NAND

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for_____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one
Addition of two octal numbers "36" and "71" results in _____

► 213
► 123
► **127**
► 345

FINALTERM EXAMINATION
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Question No: 1 (Marks: 1) - Please choose one
The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.

► 8-bit
► 16-bit
► **32-bit (Page 25)**
► 64-bit

Question No: 2 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____

► 11101
► 11011
► **10111 (According to rule)**
► 11110

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 3 (Marks: 1) - Please choose one
The basic building block for a logical circuit is _____

- ► A Flip-Flop
- ► **A Logical Gate (Page 7)**
- ► An Adder
- ► None of given options

Question No: 4 (Marks: 1) - Please choose one
The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

- ► Undefined
- ► One
- ► **Zero (According to rule)**
- ► No Output as input is invalid.

Question No: 5 (Marks: 1) - Please choose one
_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

- ► 2
- ► 8
- ► **12 (According to rule "2^n")**
- ► 16

Question No: 6 (Marks: 1) - Please choose one
The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

- ► **AND (Page 182)**
- ► OR
- ► NOT
- ► XOR

Question No: 7 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

- ► **J-K input (Page 235) rep**
- ► EN input
- ► Preset input (PRE)
- ► Clear Input (CLR)

Question No: 8 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

- ► J-K input
- ► S-R input
- ► D input
- ► **Clear Input (CLR) (Page 235)**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 9 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

► **Asynchronous, synchronous (Page 369) rep**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 10 (Marks: 1) - Please choose one

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew (Page 226) rep**
► Ripple Effect
► None of given options

Question No: 11 (Marks: 1) - Please choose one

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

► 0000
► **1101 (not sure)**
► 1011
► 1111

Question No: 12 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 232)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one

_____ is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341)**
► State reduction
► Next state table
► State diagram

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 14 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

- ► State diagram
- ► Next state table
- ► State reduction
- ► **State assignment (Page 335)**

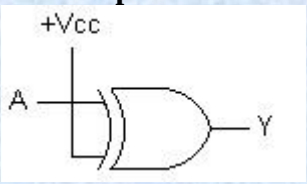
Question No: 15 (Marks: 1) - Please choose one

The best state assignment tends to _____.

- ► **Maximizes the number of state variables that don't change in a group of related states (Page 337)**
- ► Minimizes the number of state variables that don't change in a group of related states
- ► Minimize the equivalent states
- ► None of given options

Question No: 16 (Marks: 1) - Please choose one

The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A Click here for detail rep**
- ► $\overline{A}$

Question No: 17 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356) rep**

Question No: 18 (Marks: 1) - Please choose one

5-bit Johnson counter sequences through ____ states

- ► 7
- ► **10 (Page 354)**
- ► 32
- ► 25

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 19 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- ► 1100
- ► 0011
- ► **0000** **Click here for detail rep**
- ► 1111

Question No: 20 (Marks: 1) - Please choose one

The address from which the data is read, is provided by _____

- ► Depends on circuitry
- ► None of given options
- ► RAM
- ► **Microprocessor (Page 397)**

Question No: 21 (Marks: 1) - Please choose one

FIFO is an acronym for _____

- ► **First In, First Out (Page 424)**
- ► Fly in, Fly Out
- ► Fast in, Fast Out
- ► None of given options

Question No: 22 (Marks: 1) - Please choose one

LUT is acronym for _____

- ► **Look Up Table (Page 439) rep**
- ► Local User Terminal
- ► Least Upper Time Period
- ► None of given options

Question No: 23 (Marks: 1) - Please choose one

The voltage gain of the Inverting Amplifier is given by the relation _____

- ► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
- ► $V_{out} / R_f = - V_{in} / R_i$
- ► $R_f / V_{in} = - R_i / V_{out}$
- ► $R_f / V_{in} = R_i / V_{out}$

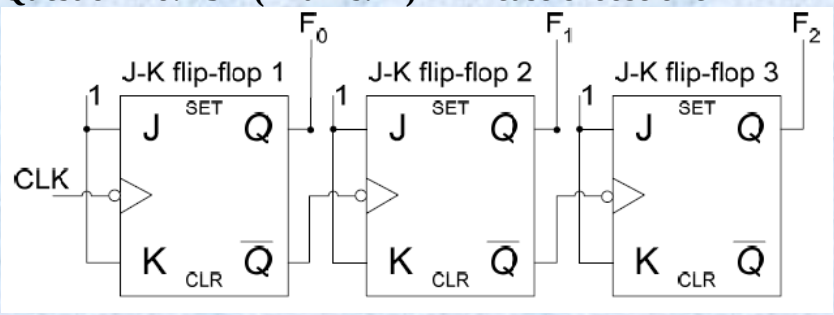
Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 24 (Marks: 1) - Please choose one

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

- ► Resolution
- ► **Accuracy (Page 460) rep**
- ► Quantization
- ► Missing Code

Question No: 25 (Marks: 1) - Please choose one



Above is the circuit diagram of _____.

- ► **Asynchronous up-counter (Page 270)**
- ► Asynchronous down-counter
- ► Synchronous up-counter
- ► Synchronous down-counter

Question No: 26 (Marks: 1) - Please choose one

The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► **2n (n multiplied by 2) (Page 354)**
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

FINALTERM EXAMINATION
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Question No: 1 (Marks: 1) - Please choose one

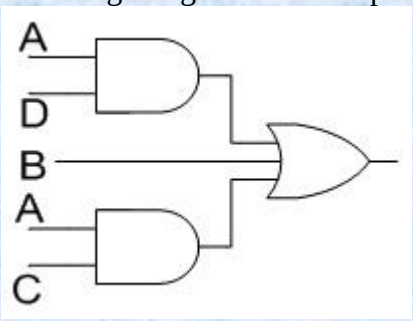
"A + B = B + A" is _____

- ► Demorgan's Law
- ► Distributive Law
- ► **Commutative Law (Page 72)**
- ► Associative Law

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 2 (Marks: 1) - Please choose one

The diagram given below represents _____



- ► Demorgans law
- ► Associative law
- ► Product of sum form
- ► **Sum of product form (Page 78) rep**

Question No: 3 (Marks: 1) - Please choose one

Following is standard POS expression

$$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$$

- ► **True (Lecture 9)**
- ► False

Question No: 4 (Marks: 1) - Please choose one

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

- ► Using a single comparator
- ► **Using Iterative Circuit based Comparators (Page 155)**
- ► Connecting comparators in vertical hierarchy
- ► Extra logic gates are always required.

Question No: 5 (Marks: 1) - Please choose one

Demultiplexer is also called

- ► Data selector
- ► Data router
- ► **Data distributor (Page 178)**
- ► Data encoder

Question No: 6 (Marks: 1) - Please choose one

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 7 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

► **Low-to-high transition of clock (Page 228) rep**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 8 (Marks: 1) - Please choose one
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

► 10 mW
► **25 mW (Page 242)**
► 64 mW
► 1024

Question No: 9 (Marks: 1) - Please choose one
_____ counters as the name indicates are not triggered simultaneously.

► **Asynchronous (Page 269)**
► Synchronous
► Positive-Edge triggered
► Negative-Edge triggered

Question No: 10 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

► **ENP, ENT (Page 285) rep**
► ENI, ENC
► ENP, ENC
► ENT, ENI

Question No: 11 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

► **Mod-6, Mod-10 (Page 299)**
► Mod-50, Mod-10
► Mod-10, Mod-50
► Mod-50, Mod-6

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 12 (Marks: 1) - Please choose one
In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs (Page 332)**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops

► 3
► **4 (Page 281)**
► 7
► 10

Question No: 14 (Marks: 1) - Please choose one
_____ is used to minimize the possible no. of states of a circuit.

► **State assignment (Page 341) rep**
► State reduction
► Next state table
► State diagram

Question No: 15 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 16 (Marks: 1) - Please choose one
The alternate solution for a demultiplexer-register combination circuit is _____

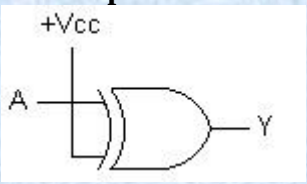
► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356)**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 17 (Marks: 1) - Please choose one
A GAL is essentially a _____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
►**Reprogrammable PAL (Page 183) rep**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 18 (Marks: 1) - Please choose one

The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A** **Click here For detail** **rep**
- ► $\overline{A}$

Question No: 20 (Marks: 1) - Please choose one

in _____, all the columns in the same row are either read or written.

- ► Sequential Access
- ► MOS Access
- ► **FAST Mode Page Access (Page 413) rep**
- ► None of given options

Question No: 21 (Marks: 1) - Please choose one

FIFO is an acronym for _____

- ► **First In, First Out (Page 424) rep**
- ► Fly in, Fly Out
- ► Fast in, Fast Out
- ► None of given options

Question No: 22 (Marks: 1) - Please choose one

In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► **Fist In First Out Memory (Page 425) rep**
- ► Flash Memory
- ► Fast Page Access Mode Memory

Question No: 23 (Marks: 1) - Please choose one

A frequency counter _____

- ► Counts pulse width
- ► **Counts no. of clock pulses in 1 second (Page 301) rep**
- ► Counts high and low range of given clock pulse
- ► None of given options

Question No: 24 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► **2n (n multiplied by 2) (Page 354) rep**
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for _____

- ► FIFO memory
- ► **LIFO memory (Page 429) rep**
- ► Flash Memory
- ► Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one
The 4-bit 2's complement representation of "+5" is _____

- ► 1010
- ► 1110
- ► 1011
- ► **0101 (Page 22)**

FINALTERM EXAMINATION
Spring 2010

Question No: 1 (Marks: 1) - Please choose one
The storage cell in SRAM is
- ► a flip –flop
- ► **a capacitor (Page 407)**
- ► a fuse
- ► a magnetic domain

Question No: 2 (Marks: 1) - Please choose one
What is the difference between a D latch and a D flip-flop?
- ► The D latch has a clock input.
- ► The D flip-flop has an enable input.
- ► The D latch is used for faster operation.
- ► **The D flip-flop has a clock input.** **Click here for detail**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 3 (Marks: 1) - Please choose one
For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will_____ if the clock goes HIGH.
►toggle Click here for detail
►set
►reset
►not change

Question No: 4 (Marks: 1) - Please choose one
The OR gate performs Boolean _____.
►multiplication
►subtraction
►division
►addition (Page 42)

Question No: 5 (Marks: 1) - Please choose one
If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be
► set (Page 219)
► reset
► invalid
► clear

5. Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.
►A = 1, B = 0, C = 0, D = 0
►A = 1, B = 0, C = 1, D = 0 (Lecture 8)
►A = 0, B = 1, C = 0, D = 0
►A = 1, B = 0, C = 1, D = 1

Question No: 6 (Marks: 1) - Please choose one
The power dissipation, *P*D, of a logic gate is the product of the
►dc supply voltage and the peak current Click here for detail
►dc supply voltage and the average supply current
►ac supply voltage and the peak current
►ac supply voltage and the average supply current

Question No: 7 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.
►True Click here for detail
►False

Question No: 8 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate
►True (Page 50)
►False

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 9 (Marks: 1) - Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer
►A parallel to serial converter circuit (Page 244)
►A counter circuit
►A BCD to Decimal decoder
►A 2-to-8 bit decoder

Question No: 10 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
►4
►8 (Page 89)
►12
►16

Question No: 11 (Marks: 1) - Please choose one
In designing any counter the transition from a current state to the next sate is determined by
►Current state and inputs (Page 332)
►Only inputs
►Only current state
►current state and outputs

Question No: 12 (Marks: 1) - Please choose one
Sum term (Max term) is implemented using _____ gates
►OR (Page 78)
►AND
►NOT
►OR-AND

Question No: 13 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____
► The next state of a given present state (Page 371) rep
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 14 (Marks: 1) - Please choose one
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?
►2
►4
►6
►8 (not sure)

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 15 (Marks: 1) - Please choose one
WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO _____

►THE FLOP-FLOP IS TRIGGERED
►Q=0 AND Q'=1
►Q=1 AND Q'=0 (Page 233)
►THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED

Question No: 16 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop
►0
►1 (Page 230)
►Invalid
►Input is invalid

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
► 0
► 1
► Invalid (Page 233)
► Input is invalid

Question No: 17 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.
►Set-up time
►Hold time (Page 242) rep
►Pulse Interval time
►Pulse Stability time (PST)

Question No: 18 (Marks: 1) - Please choose one
We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____
►Using S-R Flop-Flop
►D-flipflop
►J-K flip-flop (Page 252)
►T-Flip-Flop

Question No: 19 (Marks: 1) - Please choose one
A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.
►3
►7
►8 (Page 272)
►15

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 20 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.
►Moore machine
►Meally machine
►Johnson counter
►Ring counter (Page 355)

Question No: 21 (Marks: 1) - Please choose one
The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines
►Write Time
►Recycle Time
►Refresh Time
►Access Time (Page 417)

Question No: 22 (Marks: 1) - Please choose one
Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
►Ten
►Eight
►Three
►Two (Page 262)

Question No: 23 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
►Race condition
►Clock Skew (Page 226) rep
►Ripple Effect
►None of given options

Question No: 24 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____
►Parallel in / Serial out shift register (Page 356)
►Serial in / Parallel out shift register
►Parallel in / Parallel out shift register
►Serial in / Serial Out shift register

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for _____
► FIFO memory
► LIFO memory (Page 429) rep
► Flash Memory
► Bust Flash Memory

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 26 (Marks: 1) - Please choose one
A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?
► = 0, Cout = 0
► **= 0, Cout = 1 (Page 135)**
► = 1, Cout = 0
► = 1, Cout = 1

Question No: 27 (Marks: 1) - Please choose one
THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____
►GATED FLIP-FLOPS
►PULSE TRIGGERED FLIP-FLOPS
►POSITIVE-EDGE TRIGGERED FLIP-FLOPS
►**NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267)**

Question No: 28 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

► Truth table
► k-map
► state table
► **state diagram (Page 319)**

Question No: 29 (Marks: 1) - Please choose one
THE HOURS COUNTER IS IMPLEMENTED USING _____
►ONLY A SINGLE MOD-12 COUNTER IS REQUIRED
►MOD-10 AND MOD-6 COUNTERS
►MOD-10 AND MOD-2 COUNTERS
►**A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299)**

Question No: 30 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____
► **The next state of a given present state (Page 371) rep**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 31 (Marks: 1) - Please choose one
LUT is acronym for _____
► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 32 (Marks: 1) - Please choose one

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

► Resolution
► **Accuracy (Page 460) rep**
► Quantization
► Missing Code

Question No: 33 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

►State diagram
►**Next state table**
►State reduction
►**State assignment (Page 335) rep**

Question No: 34 (Marks: 1) - Please choose one

The high density FLASH memory cell is implemented using _____

►**1 floating-gate MOS transistor (Page 419)**
►2 floating-gate MOS transistors
►4 floating-gate MOS transistors
►6 floating-gate MOS transistors

Question No: 35 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3

The above ABEL expression will be

►Q2:= Q1 $ X $ Q3
►**Q2:= Q1 # X # Q3 (Page 210)**
►Q2:= Q1 & X & Q3
►Q2:= Q1 ! X ! Q3

Question No: 36 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

►**TTL (Page 65)**
►CMOS 3.5 series
►CMOS 5 Series
►Power dissipation of all circuits increases with time.

Question No: 37 (Marks: 1) - Please choose one

When the control line in tri-state buffer is high the buffer operates like a _____gate

►AND
►OR
►**NOT (Page 196)**
►XOR

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 38 (Marks: 1) - Please choose one
3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.
►Low switching speeds, high power dissipation
►Fast switching speeds, high power dissipation
►**Fast switching speeds, very low power dissipation (Page 61)**
►Low switching speeds, very low power dissipation

FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
The output of an AND gate is one when _____

► **All of the inputs are one (Page 40)**
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Question No: 2 (Marks: 1) - Please choose one
The OR Gate performs a Boolean _____ function

► **Addition (Page 42) rep**
► Subtraction
► Multiplication
► Division

Question No: 3 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

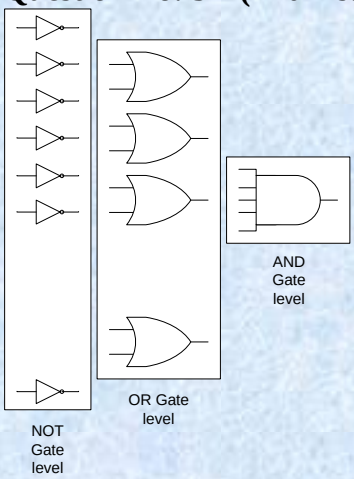
► **True rep Click here for Detail**
► False

Question No: 4 (Marks: 1) - Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► A > B = 1, A < B = 0, A < B = 1
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (Page 109)**
► **A > B = 0, A < B = 1, A = B = 1**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 5 (Marks: 1) - Please choose one

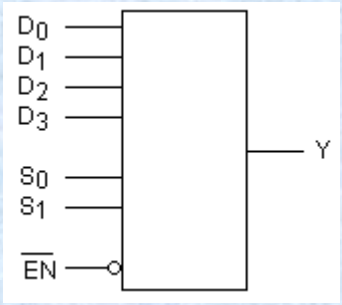


The diagram above shows the general implementation of _____ form

- ► boolean
- ► arbitrary
- ► **POS (Page 122)**
- ► SOP

Question No: 6 (Marks: 1) - Please choose one

The device shown here is most likely a



- ► Comparator
- ► **Multiplexer** **Click here for detail**
- ► Demultiplexer
- ► Parity generator

Question No: 7 (Marks: 1) - Please choose one

Demultiplexer converts _____ data to _____ data

- ► Parallel data, serial data
- ► **Serial data, parallel data (Page 356)**
- ► Encoded data, decoded data
- ► All of the given options.

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 8 (Marks: 1) - Please choose one
Flip flops are also called _____
- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► **Bi-stable multivibrators (Page 228) rep**
- ► Bi-stable singlevibrators

Question No: 9 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop
- ► 0
- ► **1 (Page 230)**
- ► Invalid
- ► Input is invalid

Question No: 10 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
- ► 0
- ► 1
- ► **Invalid (Page 230)**
- ► Input is invalid

Question No: 11 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____
- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 12 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242)**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 13 (Marks: 1) - Please choose one
We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____

- ► Using S-R Flop-Flop
- ► D-flipflop
- ► **J-K flip-flop (Page 252)**
- ► T-Flip-Flop

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 14 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

- ► True
- ► **False (Page 245)**

Question No: 15 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228) rep**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 16 (Marks: 1) - Please choose one
A negative edge-triggered flip-flop changes its state **when** _____

- ► Enable input (EN) is set
- ► Preset input (PRE) is set
- ► Low-to-high transition of clock
- ► **High-to-low transition of clock (Page 228)**

Question No: 17 (Marks: 1) - Please choose one
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

- ► 10 mW
- ► **25 mW (Page 242)**
- ► 64 mW
- ► 1024

Question No: 18 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

- ► Race condition
- ► **Clock Skew (Page 226) rep**
- ► Ripple Effect
- ► None of given options

Question No: 19 (Marks: 1) - Please choose one
A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

- ► 3
- ► 7
- ► **8 (Page 272) rep**
- ► 15

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 20 (Marks: 1) - Please choose one
A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

- ► 10 Hz
- ► **50 Hz (Page 298)**
- ► 100 Hz
- ► 500 Hz

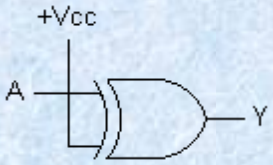
Question No: 21 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

- ► Truth table
- ► k-map
- ► state table
- ► **state diagram (Page 319)**

Question No: 22 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops

- ► 3
- ► **4 (Page 281) rep**
- ► 7
- ► 10

Question No: 23 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A Click here for Detail rep**
- ► $\overline{A}$

Question No: 24 (Marks: 1) - Please choose one
At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

- ► 2
- ► 4
- ► 6
- ► **8 (not sure) rep**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 25 (Marks: 1) - Please choose one

In _____ the $\overline{Q}$ output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.

- ► Moore machine
- ► Mealy machine
- ► **Johnson counter (Page 354)**
- ► Ring counter

Question No: 26 (Marks: 1) - Please choose one

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

- ► Moore machine
- ► Mealy machine
- ► Johnson counter
- ► **Ring counter (Page 355) rep**

Question No: 27 (Marks: 1) - Please choose one

Which is not characteristic of a shift register?

- ► **Serial in/parallel in (Page 346)**
- ► Serial in/parallel out
- ► Parallel in/serial out
- ► Parallel in/parallel out

Question No: 28 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- ► **1100**
- ► 0011
- ► **0000 Click here for detail rep**
- ► 1111

Question No: 29 (Marks: 1) - Please choose one

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

- ► Write Time
- ► Recycle Time
- ► Refresh Time
- ► **Access Time (Page 417) rep**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 30 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► **2n (n multiplied by 2) (Page 354) rep**
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

FINALTERM EXAMINATION
Fall 2009

Question No: 1 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

- ► FALSE
- ► **TRUE (Page 250)**

Question No: 2 (Marks: 1) - Please choose one
The output of an XNOR gate is 1 when _____

I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

- ► I Only
- ► IV Only
- ► I and IV only
- ► **II and III only (Page 53)**

Question No: 3 (Marks: 1) - Please choose one
NAND gate is formed by connecting _____

- ► **AND Gate and then NOT Gate (Page 45)**
- ► NOT Gate and then AND Gate
- ► AND Gate and then OR Gate
- ► OR Gate and then AND Gate

Question No: 4 (Marks: 1) - Please choose one
Consider A=1,B=0,C=1. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

- ► Zero
- ► **One (Page 46)**
- ► Undefined
- ► No output as input is invalid

Question No: 5 (Marks: 1) - Please choose one
The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____

- ► Radiation-Erase programming method (REPM)
- ► **In-System Programming (ISP) (Page 194)**
- ► In-chip Programming (ICP)
- ► Electronically-Erase programming method(EEPM)

Question No: 6 (Marks: 1) - Please choose one
The ABEL symbol for "OR" operation is

- ► !
- ► &
- ► **# (Page 201) rep**
- ► $

Question No: 7 (Marks: 1) - Please choose one
If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop

- ► 0
- ► 1
- ► **Invalid (Page 230) rep**
- ► Input is invalid

Question No: 8 (Marks: 1) - Please choose one
The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► **Doesn't have an invalid state (Page 232) rep**
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 9 (Marks: 1) - Please choose one
For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____

- ► 0
- ► **1 (Page 227) rep**
- ► Q(t)
- ► Invalid

Question No: 10 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

- ► True
- ► **False (Page 245) rep**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 11 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228) rep**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

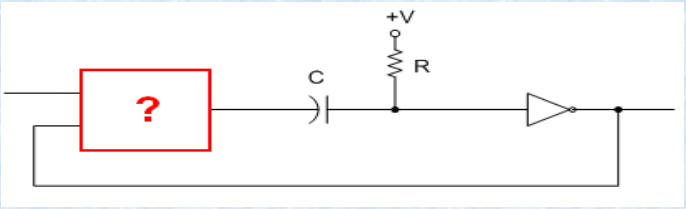
Question No: 12 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

- ► J-K input
- ► S-R input
- ► D input
- ► **Clear Input (CLR) (Page 235) rep**

Question No: 13 (Marks: 1) - Please choose one
The _____ input overrides the _____ input

- ► **Asynchronous, synchronous (Page 369) rep**
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 14 (Marks: 1) - Please choose one
Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.



- ► AND
- ► NAND
- ► NOR
- ► **XNOR (Page 262)**

Question No: 15 (Marks: 1) - Please choose one
In _____ outputs depend only on the combination of current state and inputs.

- ► **Mealy machine (Page 332)**
- ► Moore Machine
- ► State Reduction table
- ► State Assignment table

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 16 (Marks: 1) - Please choose one
_____ is used to simplify the circuit that determines the next state.

- ► State diagram
- ► Next state table
- ► State reduction
- ► **State assignment (Page 335) rep**

Question No: 17 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____

- ► Serial data to parallel
- ► **Parallel data to serial (Page 356) rep**
- ► Serial data to serial
- ► Parallel data to parallel

Question No: 18 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

- ► It is set to logic low
- ► **It is set to logic high (Page 356) rep**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

Question No: 19 (Marks: 1) - Please choose one
In the following statement
Z PIN 20 ISTYPE 'reg.invert';
The keyword "reg.invert" indicates _____

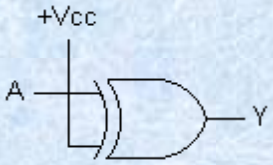
- ► An inverted register input
- ► An inverted register input at pin 20
- ► Active-high Registered Mode output
- ► **Active-low Registered Mode output (Page 360)**

Question No: 20 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- ► 2
- ► **4 (Page 394)**
- ► 8
- ► 16

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 21 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A Click here for detail rep**
- ► $\overline{A}$

Question No: 22 (Marks: 1) - Please choose one
At T0 the value stored in a 4-bit left shift was "1". What will be the value of register after three clock pulses?

- ► 2
- ► 4
- ► 6
- ► **8 (not sure) rep**

Question No: 23 (Marks: 1) - Please choose one
A bidirectional 4-bit shift register is storing the nibble 1110. Its RIGHT/$\overline{\text{LEFT}}$ input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.

- ► 1110
- ► 0111
- ► 1000
- ► **1001 Click he re for detail**

Question No: 24 (Marks: 1) - Please choose one
The high density FLASH memory cell is implemented using _____

- ► **1 floating-gate MOS transistor (Page 419) rep**
- ► 2 floating-gate MOS transistors
- ► 4 floating-gate MOS transistors
- ► 6 floating-gate MOS transistors

Question No: 25 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- ► Read Only Memory
- ► **Fist In First Out Memory (Page 425)**
- ► Flash Memory
- ► Fast Page Access Mode Memory

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 26 (Marks: 1) - Please choose one

If the FIFO Memory output is already filled with data then _____

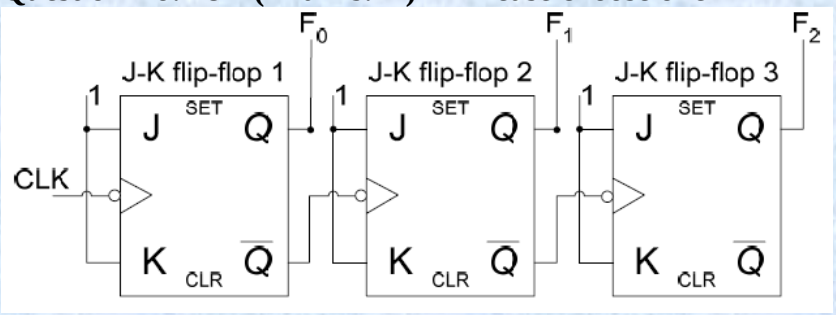
- ► It is locked; no data is allowed to enter
- ► It is not locked; the new data overwrites the previous data.
- ► Previous data is swapped out of memory and new data enters
- ► **None of given options**

Question No: 27 (Marks: 1) - Please choose one

The process of converting the analogue signal into a digital representation (code) is known as _____

- ► Strobing
- ► Amplification
- ► **Quantization (Page 445)**
- ► Digitization

Question No: 28 (Marks: 1) - Please choose one



Above is the circuit diagram of _____.

- ► **Asynchronous up-counter (Page 270) rep**
- ► Asynchronous down-counter
- ► Synchronous up-counter
- ► Synchronous down-counter

Question No: 29 (Marks: 1) - Please choose one

$(A + B)(A + \overline{B} + C)(\overline{A} + C)$ is an example of _____

- ► **Product of sum form (Page 77)**
- ► Sum of product form
- ► Demorgans law
- ► Associative law

Question No: 30 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3

The above ABEL expression will be

- ► Q2:= Q1 $ X $ Q3
- ► **Q2:= Q1 # X # Q3 (Page 210)**
- ► Q2:= Q1 & X & Q3
- ► Q2:= Q1 ! X ! Q3

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

FINALTERM EXAMINATION
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Question No: 1 (Marks: 1) - Please choose one
Caveman number system is Base _____ number system

► 2
► **5 (Page 11)**
► 10
► 16

Question No: 2 (Marks: 1) - Please choose one
The output of an XOR gate is zero (0) when _____
I) All the inputs are zero
II) Any of the inputs is zero
III) Any of the inputs is one
IV) All the inputs are one

► I Only
► IV Only
► **I and IV only (Page 53)**
► II and III only

Question No: 3 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____**10001(right opt is not given)**

► 11101
► 11011
► **10111 (According to rule) rep**
► 11110

Question No: 4 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True Click here for Detail rep**
► False

Question No: 5 (Marks: 1) - Please choose one
The simplest and most commonly used Decoders are the _____ Decoders
► **n to 2n (Page 158)**
► (n-1) to 2n
► (n-1) to (2n-1)
► n to 2n-1

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 6 (Marks: 1) - Please choose one
The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► **Decimal-to-BCD Priority (Page 166)**

Question No: 7 (Marks: 1) - Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

► **True (Page 161)**
► False

Question No: 8 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop

► 0
► **1 (Page 230)**
► Invalid
► Input is invalid

Question No: 9 (Marks: 1) - Please choose one
If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

► AND
► OR
► **NOT (Page 226)**
► XOR

Question No: 10 (Marks: 1) - Please choose one
In asynchronous digital systems all the circuits change their state with respect to a common clock

► True
► **False (Page 245) rep**

Question No: 11 (Marks: 1) - Please choose one
The low to high or high to low transition of the clock is considered to be a(n) _____

► State
► **Edge (Page 228)**
► Trigger
► One-shot

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 12 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

► **Low-to-high transition of clock (Page 228)**
► High-to-low transition of clock
► Enable input (EN) is set
► Preset input (PRE) is set

Question No: 13 (Marks: 1) - Please choose one
RCO Stands for _____
► Reconfiguration Counter Output
► Reconfiguration Clock Output
► Ripple Counter Output
► **Ripple Clock Output (Page 285)**

Question No: 14 (Marks: 1) - Please choose one
Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
► Ten
► Eight
► Three
► **Two (Page 262) rep**

Question No: 15 (Marks: 1) - Please choose one
_____ is one of the examples of asynchronous inputs.

► J-K input
► S-R input
► D input
► **Clear Input (CLR) (Page 255) rep**

Question No: 16 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew (Page 226) rep**
► Ripple Effect
► None of given options

Question No: 17 (Marks: 1) - Please choose one
A transparent mode means _____

► **The changes in the data at the inputs of the latch are seen at the output (Page 245)**
► The changes in the data at the inputs of the latch are not seen at the output
► Propagation Delay is zero (Output is immediately changed when clock signal is applied)
► Input Hold time is zero (no need to maintain input after clock transition)

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 18 (Marks: 1) - Please choose one
In _____ outputs depend only on the current state.
► Mealy machine
► **Moore Machine (Page 332)**
► State Reduction table
► State Assignment table

Question No: 19 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____

► **Parallel in / Serial out shift register (Page 356) rep**
► Serial in / Parallel out shift register
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 20 (Marks: 1) - Please choose one
The alternate solution for a demultiplexer-register combination circuit is _____

► Parallel in / Serial out shift register
► **Serial in / Parallel out shift register (Page 356) rep**
► Parallel in / Parallel out shift register
► Serial in / Serial Out shift register

Question No: 21 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

► It is set to logic low
► **It is set to logic high (Page 356) rep**
► Remains in previous state
► State of transmission line is not used to start transmission

Question No: 22 (Marks: 1) - Please choose one
Smallest unit of binary data is a _____

► **Bit (Page 394)**
► Nibble
► Byte
► Word

Question No: 23 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

► 2
► **4 (Page 394) rep**
► 8
► 16

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 24 (Marks: 1) - Please choose one
A GAL is essentially a _____.
► Non-reprogrammable PAL
► PAL that is programmed only by the manufacturer
► Very large PAL
► **Reprogrammable PAL (Page 183) rep**

Question No: 25 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8 (Page 356) rep**

Question No: 26 (Marks: 1) - Please choose one
DRAM stands for _____
► **Dynamic RAM (Page 407) rep**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 27 (Marks: 1) - Please choose one
FIFO is an acronym for _____

► **First In, First Out (Page 424) rep**
► Fly in, Fly Out
► Fast in, Fast Out
► None of given options

Question No: 28 (Marks: 1) - Please choose one **(Diagram is missing)**
In the circuit diagram of 3-bit synchronous counter shown above, The red rectangle would be replaced by which gate?
► **AND**
► OR
► NAND
► XNOR

Question No: 29 (Marks: 1) - Please choose one
The sequence of states that are implemented by a n-bit Johnson counter is

► n+2 (n plus 2)
► **2n (n multiplied by 2) (Page 354) rep**
► 2n (2 raise to power n)
► n2 (n raise to power 2)

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 30 (Marks: 1) - Please choose one
Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

FINALTERM EXAMINATION
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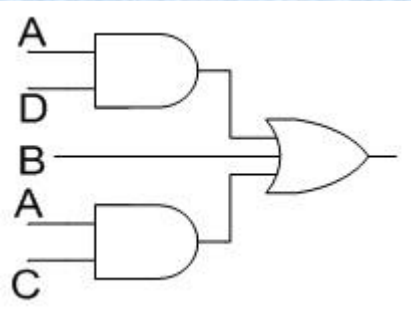
Question No: 1 (Marks: 1) - Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form (Page 78) rep**

Question No: 2 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "+7"

► **0000 (Page 34) rep**
► 1001
► 1000
► 1111

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 3 (Marks: 1) - Please choose one
NOR gate is formed by connecting _____
► **OR Gate and then NOT Gate (Page 47)**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 4 (Marks: 1) - Please choose one
A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?

► = 0, Cout = 0
► **= 0, Cout = 1 (Page 135) rep**
► = 1, Cout = 0
► = 1, Cout = 1

Question No: 5 (Marks: 1) - Please choose one
A particular half adder has
► 2 INPUTS AND 1 OUTPUT
► **2 INPUTS AND 2 OUTPUT (Page 134)**
► 3 INPUTS AND 1 OUTPUT
► 3 INPUTS AND 2 OUTPUT

Question No: 6 (Marks: 1) - Please choose one
THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____ GATE

► AND
► **OR (Page 171)**
► NAND
► XOR

Question No: 7 (Marks: 1) - Please choose one
A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BY THE MANUFACTURER.

► **TRUE (Page 182)**
► FALSE

Question No: 8 (Marks: 1) - Please choose one
Flip flops are also called _____

► Bi-stable dualvibrators
► Bi-stable transformer
► **Bi-stable multivibrators (Page 228)**
► Bi-stable singlevibrators

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 9 (Marks: 1) - Please choose one
A positive edge-triggered flip-flop changes its state when _____

- ► **Low-to-high transition of clock (Page 228)**
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 10 (Marks: 1) - Please choose one
_____ is one of the examples of synchronous inputs.

- ► **J-K input (Page 235)**
- ► EN input
- ► Preset input (PRE)
- ► Clear Input (CLR)

Question No: 11 (Marks: 1) - Please choose one
THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____

- ► GATED FLIP-FLOPS
- ► PULSE TRIGGERED FLIP-FLOPS
- ► POSITIVE-EDGE TRIGGERED FLIP-FLOPS
- ► **NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267) rep**

Question No: 12 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

- ► Truth table
- ► k-map
- ► state table
- ► **state diagram (Page 319) rep**

Question No: 13 (Marks: 1) - Please choose one
THE HOURS COUNTER IS IMPLEMENTED USING _____

- ► ONLY A SINGLE MOD-12 COUNTER IS REQUIRED
- ► MOD-10 AND MOD-6 COUNTERS
- ► MOD-10 AND MOD-2 COUNTERS
- ► **A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299) rep**

Question No: 14 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____

- ► **The next state of a given present state (Page 371) rep**
- ► The previous state of a given present state
- ► Both the next and previous states of a given state
- ► The state diagram shows only the inputs/outputs of a given states

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 15 (Marks: 1) - Please choose one
In _____ outputs depend only on the current state.

► Mealy machine
► **Moore Machine (Page 332) rep**
► State Reduction table
► State Assignment table

Question No: 16 (Marks: 1) - Please choose one
A synchronous decade counter will have _____ flip-flops
► 3
► **4 (Page 281)**
► 7
► 10

Question No: 17 (Marks: 1) - Please choose one
A multiplexer with a register circuit converts _____
► Serial data to parallel
► **Parallel data to serial (Page 356) rep**
► Serial data to serial
► Parallel data to parallel

Question No: 18 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____
►**Parallel in / Serial out shift register (Page 356)**
►Serial in / Parallel out shift register
►Parallel in / Parallel out shift register
►Serial in / Serial Out shift register

Question No: 19 (Marks: 1) - Please choose one
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

► 2
► 4
► 6
► **8 (not sure) rep**

Question No: 20 (Marks: 1) - Please choose one
A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.
► 1
► 2
► 4
► **8 (Page 356)**

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 21 (Marks: 1) - Please choose one
5-BIT JOHNSON COUNTER SEQUENCES THROUGH ____ STATES

► 7
► **10 (Page 354) rep**
► 32
► 25

Question No: 22 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.
►Moore machine
►Meally machine
►Johnson counter
►**Ring counter (Page 355)**

Question No: 23 (Marks: 1) - Please choose one
DRAM stands for _____
► **Dynamic RAM (Page 407) rep**
► Data RAM
► Demoduler RAM
► None of given options

Question No: 24 (Marks: 1) - Please choose one
If the FIFO Memory output is already filled with data then _____

► It is locked; no data is allowed to enter
► It is not locked; the new data overwrites the previous data.
► Previous data is swapped out of memory and new data enters
► **None of given options**

Question No: 25 (Marks: 1) - Please choose one
LUT is acronym for _____
► **Look Up Table (Page 439) rep**
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 26 (Marks: 1) - Please choose one
_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.
► Resolution
► **Accuracy (Page 460) rep**
► Quantization
► Missing Code

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari

Question No: 27 (Marks: 1) - Please choose one **(Diagram is missing)**

In the circuit diagram of 3-bit synchronous counterThe red rectangle, shown above would be replaced which gate?

► AND
► OR
► NAND
► XNOR

Question No: 28 (Marks: 1) - Please choose one

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -------

► THE FLOP-FLOP IS TRIGGERED
► Q=0 AND Q'=1
► Q=1 AND Q'=0
► **THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED (page 223)**

Question No: 29 (Marks: 1) - Please choose one

A frequency counter _____

► Counts pulse width
► **Counts no. of clock pulses in 1 second (Page 301) rep**
► Counts high and low range of given clock pulse
► None of given options

Question No: 30 (Marks: 1) - Please choose one

Stack is an acronym for _____

► FIFO memory
► **LIFO memory (Page 429) rep**
► Flash Memory
► Bust Flash Memory

Muhammad Moaaz Siddiq – MCS (2nd)
mc100401285@Gmail.com
Campus:- Institute of E-Learning & Modern Studies (IEMS) Samundari