

# Cs302 quiz 1 file

By

<https://vuonlinehelp.blogspot.com/p/cs302-quiz-no02-solution-fall2021.html>

Compose by ALI HASSAN

Which of the following is the octal equivalent of 28 decimal number?

34

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

$(2^{64})-1$

In a 4-variable K-map, a 2-variable product term is produced by a 4-cell group of 1s

For a Standard SOP expression, a \_\_\_\_ is placed in the cell corresponding to the product term present in the expression.

1

The \_\_\_\_\_ input select/deselects both the decoders simultaneously.

Enable

NAND and \_\_\_\_\_ gates are known as Universal Gates.

**NOR**

The declaration section of ABEL generally includes the device declaration, \_\_\_\_\_ declarations and set declarations.

**Pin**

An SOP expression having a domain of 2 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.

**4**

In the 32-bit Single Precision Floating formation, the exponent value \_\_\_\_\_ is reserved to represent 0 exponents.

**0**

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

**Slow**

The complement of a variable is always

**The inverse of the variable**

$A(B + C) = A.B + A.C$  is the expression of \_\_\_\_\_.

**Distributive Law**

If the number 2025 is represented in floating point, then exponent is \_\_\_\_\_.

**3**

Excess-8 code of -6 is \_\_\_\_\_.

0010

A 3-variable Karnaugh map has

Eight cells

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is \_\_\_\_\_ to the range of values that are to be represented.

Proportional

Suppose we want to transmit the data "10001101" and an "Even-Parity" bit scheme is used to detect errors, the parity bit added to the data will be\_\_\_\_\_.

Both "0" and "1" can be used

The carry propagation delay problem in parallel binary adder can be solved by \_\_\_\_\_.

Using two full adders

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a \_\_\_\_\_ multiplexer.

2-input, 8-bit

The octal equivalent of the following binary number is

\_\_\_\_\_.

117

A' is written in ABEL as\_\_\_\_\_.

!A

Which of the following is the hexadecimal equivalent of 28?

1C

High Level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_.

0.9 V

Adjacent 1s detector circuit will have active high output for the input.

0011

Modern information techniques are relying more on \_\_\_\_\_ transmission.

Digital

The \_\_\_\_\_ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.

Two

How many data select lines are required for selecting eight inputs?

3

Select the mode of programming in which GAL 16V8 can be programmed.

All of the given option

\_\_\_\_\_ has the fastest switching speed and low power requirement.

Advanced low power Schottky

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_.

**0.1**

The minimum time for which the input signal has to be maintained at the input of flip-flop is called \_\_\_ of the flip-flop.

**Hold time**

A Divide-by-20 counter can be achieved by using

**Flip-Flop and DIV 10**

Each stage of Master-slave flip-flop works at \_\_\_ of the clock signal.

**One half**

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using \_\_\_

**NOT**

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is \_\_\_

**1111**

\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

**Race condition**

The Synchronous counters are also known as Ripple Counters: **False**

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the \_\_\_

**Set-up time**

The n flip-flops store \_\_\_ states.

**2<sup>n</sup>**

When the \_\_\_ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of \_\_\_

**1,2**

A positive edge-triggered flip-flop changes its state when \_\_\_

**Low-to-high transition of clock**

A decade counter is \_\_\_

**Mod-10 counter**