Cs302 quiz 1 file

Update quiz

By

https://vuonlinehelp.blogspot.com/p/cs302-quiz-no02-solution-fall2021.html

Compose by ALI HASSAN

(***Note: file is website sa copy karna ka bad bani ha tu searching karty howy space ni use krni ap na phr search thk ho ga.(for example:*** whichof) ***Thanks you!)***

Which of the following is the octal equivalent of 28 decimal number?

34

The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.

(2^64)-1

In a 4-variable K-map, a 2-variable product term is produced by

a 4-cell group of 1s

For a Standard SOP expression, a ____ is placed in the cell corresponding to the product term present in the expression.

1

The _____ input select/deselects both the decoders simultaneously.

Enable

NAND and _____ gates are known as Universal Gates.

NOR

The declaration section of ABEL generally includes the device declaration, _____declarations and set declarations.

Pin

An SOP expression having a domain of 2 variables will have a truth table having _____combinations of inputs and corresponding output values.

4

In the 32-bit Single Precision Floating formation, the exponent value _____ is reserved to represent 0 exponents.

0

CMOS technology is characterized by low power dissipation with _____ switching speeds.

Slow

The complement of a variable is always

The inverse of the variable

A (B + C) = A.B + A.C is the expression of _____.

Distributive Law

If the number 2025 is represented in floating point, then exponent is _____.

3

Excess-8 code of -6 is _____.

0010

A 3-variable Karnaugh map has

Eight cells

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is _____ to the range of values that are to be represented.

Proportional

Suppose we want to transmit the data “10001101” and an “Even-Parity” bit scheme is used to detect errors, the parity bit added to the data will be_____.

Both “0” and “1” can be used

The carry propagation delay problem in parallel binary adder can be solved by _____.

Using two full adders

Two 2-input, 4-bit mulitplexers 74X157 can be connected to implement a _____ multiplexer.

2-input, 8-bit

The octal equivalent of the following binary number is _____.

117

A’ is written is ABEL as_____.

!A

Which of the following is the hexadecimal equivalent of 28?

1C

High Level Noise Margins (VNH) of CMOS 5 volt series circuits is _____.

0.9 V

Adjacent 1s detector circuit will have active high output for the input.

0011

Modern information techniques are relying more on _____ transmission.

Digital

The _____ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.

Two

How many data select lines are required for selecting eight inputs?

3

Select the mode of programming in which GAL 16V8 cam be programmed.

All of the given option

_____ has the fastest switching speed and low power requirement.

Advanced low power Schottky

The PLA can be programmed to give an output of constant _____ or _____.

0.1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called ___ of the flip-flop.

Hold time

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

Each stage of Master-slave flip-flop works at ___ of the clock signal.

One half

In Master-Slave flip-flop the clock signal is connected to slave flip-flip using ___

NOT

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is ___

1111

___ is said to occur when multiple internal variables change due to change in one input variable

Race condition

The Synchronous counters are also known as Ripple Counters:

False

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the ___

Set-up time

The n flip-flops store ___ states.

2^n

When the ___ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of ___

1,2

A positive edge-trigged flip-flop changes its state when ___

Low-to-high transition of clock

A decade counter is ___

Mod-10 counter

The look-ahead carry circuits_____

Reduce propagation delay

If two numbers in BCD representation generate an invalid BCD number then the binary __ is added to the result

0110

Both the multiplexers are selected simultaneously when _____is set to logic _____ in 2-inputs, 8-bit Multiplexer.

G, Low

Function labels required to represent the input/output combinations for each segment in 7-segment display
7

Multiplexers are also known as _____

Data selectors

The PLA can be programmed to give and output of constant_____ or _____
0, 1

Cin is part of _____ Adder.

Full

The look-ahead carry circuits_____

Reduce propagation delay

Which of the following gates has the outputs 1 if and only if at last one input is 1?

OR

A sop expression can be implemented by on ___combination of gates.

AND-OR

The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through ___ ALU units in 16-bit ALU.

Four

Digital circuits operates with_____ voltage value(s)
2

In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles_____
Lower priority outputs

To determine the seven expressions for each of the seven outputs in 7-segment display, seven _____ variable Karnaugh maps are used.
4

The output of a NAND Gate is ____ when all the inputs are one.

Zero

The _____ is the slowest and consumes more power.

Standard TTL

The between expression X-AB+CD represents
Two ANDs ORed together

The expression F-A+B+C describes the operation of three bits___ Gate.

OR

Which one of the following is NOT a valid rule of Boolean Algebra?

A=A’

A 5-Variable Karnaugh map has

Thirty two cells

____ is invalid number of cells in a single group formed by the adjacent cells K-map

12

In 32-bit Single –Precision floating point format representation the range of exponent value is from _____to _____

+127 to -126

____ has the fastest switching speed and low power requirements

Advanced low power schottky

Which of the following is a volatile memory?
DRAM

_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.
Combinational Input

The AND Gate performs a logical _____ function.
Division

The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacent 1s are detected in the input, the output is set to high.

1

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

row, column

Which of the following Output Equations determines the output of the State Machine?
MAX = Q0Q1EN

The maximum value, represented by a single hexadecimal digit is _____.

"F"

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.
1

The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.
High

Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.
Negative-OR, Negative-AND

Two signals _____ and _____ provide the timing inputs to the State Machine.
PTIME and QTIME

The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.
4

PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.
PLDs

The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.
CONSTATE

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.
Shift Registers

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.
Synchronous

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.
None of the given

The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.
XOR, NAND

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.
Four

In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.
NAND, NAND

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.
8 AND

8-bit parallel data can be converted into serial data by using _____ multiplexer.
8-to-1

The _____ input overrides the _____ input.
Asynchronous, synchronous

A SOP expression can be implemented by an _____ combination of gates.
AND-OR

The 64-cell array organized as 8 x 8 cell array is considered
as an 8 byte memory

The terminal count of a 4-bit binary counter in the UP mode is _____.

1100

A 3-variable karnaugh map has
eight cells

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.
Q output of all flip-flops to clock input of next flip-flops

Memory is arranged in _____.
Two-dimensional manner

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.
1001

Subtractors also have output to check if 1 has been _____.
Primed

The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.
Three

A multiplexer with a register circuit converts
Parallel data to serial

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.
True

The n flip-flops store _____ states.
2^n

The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.
four

Why demultiplexer is called a data distributor?
Single input to Single Output

When the transmission line is idle in an asynchronous transmission
It is set to logic high

UVERPROM is stands for
Ultra-Voilet

In memory write cycle, the time for which the WE signal remains active is known as the _____.
Write pulse width

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.
AND

PALs tend to execute _____ logic.
SOP

The ROM used by a computer is relatively _____ as it stores few buyers of code used to Boot the Computer system on power up.
Small

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?
WE

You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);
NSY2 or EWY2

A NOR based S-R latch is implemented using _____ gates instead of _____ gates.
NOR, NAND

Implementation of Latch is required almost _____ transistor.
Six

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.
7.8 microsec

The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.
NAND

For a Standard SOP expression, a _____ is placed in the cell

corresponding to the product term (Minterm) present in the expression.
1

Select the mode of programming in which GAL16V8 can be programmed:
All of the given

Divide-by-32 counter can be achieved by using
Flip-Flop and DIV 32

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.
REQ1

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

One

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:
1111

Adding two octal numbers "36" and "71" result in _____.
127

The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.
Truth Table

The domain of the expression AB'CD + AB' + C'D + B is
A, B, C and D

If the number of samples that are collected is reduced by half, the

reconstructed signal will be _____ from/to the original.
Same

In DRAM read cycle R /W signal is activated to read data which is made available on the _____ data line.
D(OUT)

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.
True

Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.
RAM

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.
Top

Which one flip-flop has an invalid output state?
SR

The output of a NAND gate is _____ when all the inputs are one.
Zero

The Transition table is very similar to the _____ table.
State

Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.
256

Canonical form is a unique way of representing _____.
SOP

_____ Counters as the name indicates are not triggered simultaneously.
Synchronous

Cin is part of _____ Adder.
Full

Flash memories Operation are classified into _____ different operation.
Two

A Product term is 0 when_____

Any one literal is 0

In 8-inpit multiplexer, the two outputs are connected through a/an___gate.

OR

____ Device dissipate varying amount of power depending upon the frequency of operation.

CMOS

Boolean Addition operation is performed by a(an)___ gate.

OR

A SOP expression can be implemented by an_____ combination of gates.

AND-OR

The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.

(2^64)-1

In 16-bit ALU, The G output is activated if the 4-bi unit generate a Carry ____ irrespective of Carry___.

Out,In

A standard POS from has ____ ters that have all the variables in the domain of the expression.

Sum

In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles_____.

Lower priority inputs

Which of the following is the example of comparater?

XNOR

IN CMOS 5 Volt series, Input voltage of Logic high signal (VIH) with a ranges from ____ to ____ volts.

3,5,5

The Adjacent 1 S Detector accepts 4-bits input. If ____ adjacent 1S are detected in the input, the output is set to high.

4

DE Morgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

Negative-AND, Negative-OR

Adding two octal numbers "36 and 71" result in ____.

127

Any of the _____ forms of the Karnaugh Map can be used to simplify Boolean expressions

Four

Quine-McCluskey and K-Map methods are used for _____ of Boolean expression.

Simplification

The number "1259" may belong to ____ number system.

Decimal or Hexadecimal system

The series of TTL chips are characterized by their____.

Switching Speed only

All ABEL statements must end with_____.

;

In sequential circuit memory elements are connected with____.

Clock

In the 32-bit Single Precision Floating Point format, the exponent value____ is reserved to represent infinity exponents.

255

The _____ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

PLA

The limitation in implementation of parallel binary address is known as_____.

Carry input

The Gray code is different form the unsigned binary code because___.

Successive value of Gray code by only one bit

Removing the NOT gate at the output of the NOR gate result in an____.

OR gate

Portable devices that run on batteries use___ circuit that have low power dissipation.

Integrated

The domain of the expression AB'CD+B is

B only

_____ is a single input gate

OR

To represent in digital value, the number of digit (0s and 1s) that represent a quantity is ____ to the range of values that are to be represented.
Equal

BCD code of 16 is____.

00010001

To determine the seven expressions for each of the seven outputs in 7-segment display, seven____ variable Karnaugh Maps are used.

3

In Odd parity generator circuit which gate is used to detect parity errors?

XOR

A 3-variable Karnaugh map has

Eight cells

The measurable values generally change over a
Continuous range

____ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.
GAL

When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?
1001

How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decorder?
Three

The simplified expression using either of the two K-maps are_____.
Identical

Which of the following expression in the product of sums form?

AB+CD

CMOS technology is characterized by low power dissipation with____ switching speeds.

Slow

GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

True

High level Noise Margins (VNH) of CMOS 5 volt series circuits is_____

0.9 V

The output of the expression F=A+B+C will be Logic _____when A=0, B=1, C=1. the symbol"+" here represents OR Gate
One

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

SET

3.3 v CMOS series is characterized by _____ and_____as compared to the 5 v CMOS series.

Fast switching speeds, very low power dissipation (page61)

The binary value “1010110” is equivalent to decimal _____
86

The _____ Encoder is used as a keypad encoder.

Decimal-to-BCD Priority

How many data select lines are required for selecting eight inputs?

3

The Quad Multiplexer has _____ outputs

4

Demultiplexer has

Single input and multiple outputs.

The expression _____ is an example of Commutative Law for Multiplication.

AB=BA

The look-ahead carry circuits_____

Reduce propagation delay

What is the output expression of segment ‘b’ implementation in BCD to 7-segment decoder?

B’+C’D’+CD

2-input, 8-bit Multiplexer, by setting the S input to logic_____the____ inputs of both the multiplexers are selected.

High, B

The maximum decimal number that can be represented using the 64-bit unsigned representation_____
(2^64)-1

When two or more products terms are assumed by Boolean addition, the result is a ____
SOP

Tri-State Buffer is a ___ gate with a control line that disconnects the

NOT

The 4-bits 2's complement representation of "7" is _____

1001

_____and _____ are the steps of the Quine-McCluskey.
Find prime implicants and select minimal set of the prime implicants.

The binary number 1011,101 has an Integer part represented by_____ and a fraction part ___ separated by a decimal point.

1011,101

Subtractors also have output to check if 1 has been _____

Borrowed

CMOS technology is characterized by low power dissipation with_____ switching speeds.
Slow

The _____ description is used to simulate the logic circuit and verify its operation.
Test vector

How many outputs can an integrated circuit comparator have?
Three

Which of the following is not the correct method of grouping?
Diagonally

The output of the expression F=A.B.C will be logic _____when A=1,B=0, C=1.

Zero

The _____ gate and ___ gate implementation connected at the B input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.
AND, OR

In the 32-bit Single Precision Floating point format, the exponent value _____ is reserved infinity exponent.

99

The Boolean expression (AB'CS') is used

A product term

The product of an XOR gate is zero(0), when _____All the inputs are zero

I and IV only

_____ methods are used to Convert Decimal fractions to Binary.

2

To display the number___ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

29

TTL based devices work with a dc supply of_____ volts.

+5

_____ come in different configurations they are identified by number.

PALs

The digital circuits operate with combination of values given below:

+5 volts , 0 volts

Binary decoders have _____ inputs and _____ outputs.

N, 2^n

Combinational lagic is used for combinational circuits, where as registered logic is based on_____

Sequential

A multiplexer circuit has___ input(s) and _____output(s).

Multiple, single

The logical sum of two or more logical product term is called

SOP

Demultiplexer is also called_____

Data distributor

1010 – 0101 = _____

0101

The product term in standard SOP are called:

Minterms

The cell marked 6 in 4-varable k-represent minterm 6 or the maxterm 6 having the following binary value of variables A,B,C and D.

A=0,B=1,C=1,D=0

If Odd-parity is being used therefore the 4-bit data and the parity bit should up to give -----

Odd

The quine-McCluskey method has ------ number of step.

2

In look ahead circuits G stands for.

Propagation delay