

CS302 Quiz No.01 Solution Fall2021

Quiz #1 (1 to 20) Lectures♥

Inputs          Output

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

This function table represents \_\_\_\_\_ Gate.

Or gate

The ABEL symbol for “OR” operation is

#

A standard SOP form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.

Sum

Which one of the following is not a valid rule of Boolean algebra?

$$A = \bar{A}$$

How many data select lines are required for selecting eight inputs?

3 (correct)

If two adjacent 1s are detected in the input, the output is set to high. Input combinations will be

0011(ans)

The 4-variable Karnaugh Map (K-Map) has \_\_\_\_\_ rows and \_\_\_\_ columns

4,4, (ans)

The boolean expression  $A + B' + C$  is

A sum term(ans)

The boolean expression  $AB'CD'$  is

A product term(ans)

Don't care conditions are marked as \_\_\_\_\_ in the output column of the function table

X(ans)

An example of SOP expression is

Both (a) and (b)(ans)

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1 (ans)

A SOP expression having a domain of 3 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.

Select correct option:

2 (Correct)

Multiplexers are also known as \_\_\_\_\_.

**Data Selectors**

The OR Gate performs a Boolean \_\_\_\_\_ function

Addition (Correct)

Sum term (Max term) is implemented using \_\_\_\_\_ gates

OR (Correct)

The number "1259" may belong to \_\_\_\_\_ number system.

Binary or Hexadecimal system (Correct)

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result

1111 (Correct)

"1101" in signed representation is equivalent to \_\_\_\_\_

13 (Correct)

TTL based devices work with a dc supply of \_\_\_\_ Volts

+5 (Correct)

In decimal value "275" the weight of the digit "7" is \_\_\_\_\_

100 (Not Sure)

The decimal "10" will have an octal equivalent \_\_\_\_\_

9 (Not Sure)

Caveman number system is Base \_\_\_\_\_ number system

5 (Correct)

How many bits must each word have in one-to-four line de-multiplexer to be implemented using a memory?

1 bits

The total amount of memory is depends upon \_\_\_\_\_

The size of the address bus of the microprocessor

\_\_\_\_\_ can be determined the Instability condition.

### Logic diagram

If we add an inverter at the output of AND gate, what function is produced?

### NAND

Which is also known as coincidence detector?

### AND gate

Transition table include \_\_\_\_\_

### Squares

For every possible combination of logical states in the inputs, which table shows the logical state of a digital circuit output?

### Truth table

Stack is an acronym for \_\_\_\_\_

### LIFO memory

When an Asynchronous sequential circuit changes two or more binary states variables a Condition occurs called \_\_\_\_\_

### Race condition

Positive OR gate is also a negative

### AND gate

Time delay device is memory element of \_\_\_\_\_

### Asynchronous circuits

Boolean algebra is also called

- a) Arithmetic algebra
- b) Switching algebra

c) Both A & B

Boolean function must be brought into \_\_\_\_\_ To perform product of max terms

### OR terms

The binary number 10101 is equivalent to the decimal number \_\_\_\_\_.

21

The domain of expression  $ABCD + AB + CD + B$  is—

B only

The Boolean expression  $A BC D$  is—

Sum term

The universal gate is\_\_\_\_\_.

NAND gate

According to boolean algebra absorption law, which of the following is correct?

$Xy+y=x$

A Boolean function may be transformed into

Logical diagram

The inverter is \_\_\_\_\_

NOT gate

The resulting circuit of a NAND gate are connected together is\_\_\_\_\_

NOT gate

$X*y = y*x$  is the

Identity element

Minterms are also called

Standard product

OR gate and \_\_\_\_\_ will form The NOR gate?

NOT gate

The NAND gate is AND gate followed by .....

NOT gate

Max terms are also called \_\_\_\_\_.

Standard sum

In Boolean algebra Multiplicative inverse is

A

By the repeated use of \_\_\_\_\_ Digital circuit can be made

NAND gates

The only function of NOT gate is \_\_\_\_\_ of the following.

Invert input signal

Boolean algebra is defined as a set of \_\_\_\_\_.

Two values

First operator precedence for evaluating Boolean expressions is

Parenthesis

The output is \_\_\_\_\_ When an input signal 1 is applied to a NOT gate

0

The bar sign (-) indicates \_\_\_\_\_ In Boolean algebra?

NOT operation

The value of n is \_\_\_\_\_ when the resolution of an n bit DAC with a maximum input of 5 V is 5 mV.

10

2's complement of binary number 0101 is \_\_\_\_\_

1011

An OR gate has 4 inputs. The output is ..... When One input is high and the other three are low.

High

To convert BCD to seven segments \_\_\_\_\_ device is used.

Decoder

Decimal number 10 is equal to binary number \_\_\_\_\_.

1010

In 2's complement representation the number 11100101 represents the decimal number \_\_\_\_\_.

-27

BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are\_\_\_\_\_.

All

A decade counter skips \_\_\_\_\_.

Binary states 1010 to 1111

\_\_\_\_\_ Number of States A ring counter with 5 flip flops will have?

5

Positive edge-triggered flip-flop changes its state when \_\_\_\_\_

Low-to-high transition of clock

If S=1 and R=1, for negative edge triggered flip-flop then  $Q(t+1) =$  \_\_\_\_\_

Invalid

Adjacent 1s detector circuit will have active low output for the input

1101

A 5-variable karnaugh map has

Thirty two cells

8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer

8-to-1 ok

In asynchronous digital systems all the circuits change their state with respect to a common clock

False

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 16

The Synchronous counters are also known as Ripple Counters:

False ok

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

The 3-to-8 Decoder has active-low outputs and three extra \_\_\_\_ gates connected at the three inputs to reduce the four unit load to a single unit load.

Not

Which of the number is not a representative of hexadecimal system?

“1001” correct

High level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_

0.9 V correct

To get the answer “1” in Boolean addition of three variables, \_\_\_\_\_

One of the variables must be 1 correct

The 3-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms

8 correct

\_\_\_\_\_ is invalid number of cells in a single group formed by the adjacent cells in K-map

2 correct

Consider  $A=1, B=0, C=1$ . A, B and C represent the input of three bit NAND gate the output of the NAND gate will be \_\_\_\_\_

Zero

The Binary number 1011.101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_\_ separated by a decimal point.

1011, 101 correct

$1011+101 =$  \_\_\_\_\_

10000 correct

Adding two octal numbers "36" and "71" result in \_\_\_\_\_

127 correct

The first Least Most digit in decimal number system has

Has position 0 and weight equal to 1 not sure

Sum term (Max term) is implemented using \_\_\_\_\_ gates

OR correct

The OR Gate performs a Boolean \_\_\_\_\_ function

Addition correct

Adding two octal numbers "36" and "71" result in \_\_\_\_\_

127 correct

If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be \_\_\_\_\_

24582 not sure

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

TRUE correct

The three fundamental gates are \_\_\_\_\_

NOT, OR, AND correct

A SOP expression having a domain of 3 variables will have a truth table having \_\_\_\_ combinations of inputs and corresponding output values.

8 correct

The 4-variable K-Map has \_\_\_\_\_ rows and \_\_\_\_\_ columns of cells.

4, 4 correct

NAND gate is form by connecting \_\_\_\_\_

AND Gate and then NOT Gate correct

Which of the following is the octal equivalent of 28 decimal number?

34

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

$(2^{64})-1$

In a 4-variable K-map, a 2-variable product term is produced by

A 4-cell group of 1s

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term present in the expression.

1

The \_\_\_\_\_ input select/deselects both the decoders simultaneously.

Enable

NAND and \_\_\_\_\_ gates are known as Universal Gates.

NOR

The declaration section of ABEL generally includes the device declaration, \_\_\_\_\_ declarations and set declarations.

Pin

An SOP expression having a domain of 2 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.

4

In the 32-bit Single Precision Floating formation, the exponent value \_\_\_\_\_ is reserved to represent 0 exponents.

0

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

Slow

The complement of a variable is always

The inverse of the variable

$A(B + C) = A.B + A.C$  is the expression of \_\_\_\_\_.

Distributive Law

If the number 2025 is represented in floating point, then exponent is \_\_\_\_\_.

3

Excess-8 code of -6 is \_\_\_\_\_.

0010

A 3-variable Karnaugh map has

Eight cells

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is \_\_\_\_\_ to the range of values that are to be represented.

### Proportional

Suppose we want to transmit the data "10001101" and an "Even-Parity" bit scheme is used to detect errors, the parity bit added to the data will be\_\_\_\_\_.

### Both "0" and "1" can be used

The carry propagation delay problem in parallel binary adder can be solved by \_\_\_\_\_.

Using two full adders

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a \_\_\_\_\_ multiplexer.

2-input, 8-bit

The octal equivalent of the following binary number is \_\_\_\_\_.

117

A' is written in ABEL as\_\_\_\_\_.

!A

Which of the following is the hexadecimal equivalent of 28?

1C

High Level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_.

0.9 V

Adjacent 1s detector circuit will have active high output for the input.

0011

Modern information techniques are relying more on \_\_\_\_\_ transmission.

Digital

The \_\_\_\_\_ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.

Two

How many data select lines are required for selecting eight inputs?

3

Select the mode of programming in which GAL 16V8 can be programmed.

All of the given option

\_\_\_\_\_ has the fastest switching speed and low power requirement.

Advanced low power Schottky

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_.

0.1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called \_\_\_\_ of the flip-flop.

Hold time

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

Each stage of Master-slave flip-flop works at \_\_\_\_ of the clock signal.

One half

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using \_\_\_\_

NOT

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is \_\_\_\_

1111

\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

Race condition

The Synchronous counters are also known as Ripple Counters:

False

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the \_\_\_\_

Set-up time

The n flip-flops store \_\_\_\_ states.

$2^n$

When the \_\_\_\_ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of \_\_\_\_

1,2

A positive edge-triggered flip-flop changes its state when \_\_\_\_

Low-to-high transition of clock

A decade counter is \_\_\_\_

Mod-10 counter

The look-ahead carry circuits \_\_\_\_\_

Reduce propagation delay

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_ is added to the result

0110

Both the multiplexers are selected simultaneously when \_\_\_\_\_ is set to logic \_\_\_\_\_ in 2-inputs, 8-bit Multiplexer.

G, Low

Function labels required to represent the input/output combinations for each segment in 7-segment display

7

Multiplexers are also known as \_\_\_\_\_

Data selectors

The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_

0, 1

Cin is part of \_\_\_\_\_ Adder.

Full

The look-ahead carry circuits\_\_\_\_\_

Reduce propagation delay

Which of the following gates has the outputs 1 if and only if at least one input is 1?

OR

A sop expression can be implemented by on \_\_\_combination of gates.

AND-OR

The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through \_\_\_ ALU units in 16-bit ALU.

Four

Digital circuits operates with \_\_\_\_\_ voltage value(s)

2

In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles \_\_\_\_\_

Lower priority outputs

To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_\_\_ variable Karnaugh maps are used.

4

The output of a NAND Gate is \_\_\_\_\_ when all the inputs are one.

Zero

The \_\_\_\_\_ is the slowest and consumes more power.

Standard TTL

The between expression  $X-AB+CD$  represents

Two ANDs ORed together

The expression  $F = A + B + C$  describes the operation of three bits \_\_\_ Gate.

OR

Which one of the following is NOT a valid rule of Boolean Algebra?

$A = A'$

A 5-Variable Karnaugh map has

Thirty two cells

\_\_\_ is invalid number of cells in a single group formed by the adjacent cells K-map

12

In 32-bit Single –Precision floating point format representation the range of exponent value is from \_\_\_ to \_\_\_

+127 to -126

\_\_\_\_\_ has the fastest switching speed and low power requirements

Advanced low power schottky

Which of the following is a volatile memory?

DRAM

\_\_\_\_\_ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

Combinational Input

The AND Gate performs a logical \_\_\_\_\_ function.

Division

The Adjacent 1s Detector accepts 4-bit inputs. If \_\_\_\_\_ adjacent 1s are detected in the input, the output is set to high.

1

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

The FAST Model Page Access allows \_\_\_\_\_ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a \_\_\_\_\_ with a \_\_\_\_\_.

Row, column

Which of the following Output Equations determines the output of the State Machine?

MAX = QQQ1EN

The maximum value, represented by a single hexadecimal digit is \_\_\_\_\_.

“F”

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a \_\_\_\_\_.

1

The Static Ram (SRAM) is non-volatile and is not a \_\_\_\_\_ density memory as a latch is required to store a single bit of information.

High

Demorgan's two theorems prove the equivalency of the NAND and \_\_\_\_\_ gates and the NOR and \_\_\_\_\_ gates respectively.

Negative-OR, Negative-AND

Two signals \_\_\_\_\_ and \_\_\_\_\_ provide the timing inputs to the State Machine.

PTIME and QTIME

The 74HC163 is a 4-bit Synchronous counter, it has \_\_\_\_\_ data output pins.

4

PLDs have In-System Programming (ISP) capability that allows the \_\_\_\_\_ to be programmed after they have been installed on a circuit board.

PLDs

The CONSTATE.CLK = Clock is used to indicate that the \_\_\_\_\_ state variables change on a clock transition.

CONSTATE

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using \_\_\_\_\_.

Shift Registers

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as \_\_\_\_\_ inputs.

Synchronous

For a down counter that counts from (111 to 000), if current state is "101" the next state will be \_\_\_\_\_.

None of the given

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

XOR, NAND

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to \_\_\_\_\_ location(s) using a single address.

Four

In NAND based S-R latch, output of each \_\_\_\_\_ gate is connected to the input of the other \_\_\_\_\_ gate.

NAND, NAND

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires \_\_\_\_\_ gates for the 8 product terms (minterms) with an 8-input OR gate.

8 AND

8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer.

8-to-1

The \_\_\_\_\_ input overrides the \_\_\_\_\_ input.

Asynchronous, synchronous

A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.

AND-OR

The 64-cell array organized as 8 x 8 cell array is considered

As an 8 byte memory

The terminal count of a 4-bit binary counter in the UP mode is \_\_\_\_\_.

1100

A 3-variable karnaugh map has

Eight cells

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_.

Q output of all flip-flops to clock input of next flip-flops

Memory is arranged in \_\_\_\_\_.

Two-dimensional manner

If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result.

1001

Subtractors also have output to check if 1 has been \_\_\_\_\_.

Primed

The Test Vector definition defines the test vectors for all the three counter inputs and \_\_\_\_\_ counter output/outputs.

Three

A multiplexer with a register circuit converts

Parallel data to serial

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

The n flip-flops store \_\_\_\_\_ states.

$2^n$

The S-R latch has two inputs, therefore \_\_\_\_\_ different combinations of inputs can be applied to control the operation of the S-R latch.

Four

Why demultiplexer is called a data distributor?

Single input to Single Output

When the transmission line is idle in an asynchronous transmission

It is set to logic high

UVERPROM is stands for

Ultra-Violet

In memory write cycle, the time for which the WE signal remains active is known as the \_\_\_\_\_.

Write pulse width

The outputs of SR latches in elevator state machine are feed back to the \_\_\_\_\_ gate array for connection to the D-flipflops.

AND

PALs tend to execute \_\_\_\_\_ logic.

SOP

The ROM used by a computer is relatively \_\_\_\_\_ as it stores few buyers of code used to Boot the Computer system on power up.

Small

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration  $t_{WD}$ ?

-WE

You have to choose suitable option when your timer will reset by considering this given code:

```
TRSTATE.CLK = clk;
```

```
TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);
```

NSY2 or EWY2

A NOR based S-R latch is implemented using \_\_\_\_\_ gates instead of \_\_\_\_\_ gates.

NOR, NAND

Implementation of Latch is required almost \_\_\_\_\_ transistor.

Six

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in \_\_\_\_\_ when Distributed refresh is used.

7.8 microsec

The NOR logic gate is the same as the operation of the \_\_\_\_\_ gate with an inverter connected to the output.

NAND

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1

Select the mode of programming in which GAL16V8 can be programmed:

All of the given

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 32

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the \_\_\_\_\_ can be pressed at any time either on the first floor or the second floor in elevator.

REQ1

Consider  $A=1$ ,  $B=0$ ,  $C=1$ . A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be \_\_\_\_\_.

One

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1111

Adding two octal numbers "36" and "71" result in \_\_\_\_\_.

127

The ABEL Input file can use a \_\_\_\_\_ instead of the equation to specify the Boolean expressions.

Truth Table

The domain of the expression  $AB'CD + AB' + C'D + B$  is

A, B, C and D

If the number of samples that are collected is reduced by half, the reconstructed signal will be \_\_\_\_\_ from/to the original.

Same

In DRAM read cycle R /W- signal is activated to read data which is made available on the \_\_\_\_\_ data line.

D(OUT)

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

True

Implementation of the FIFO buffer in \_\_\_\_\_ is usually takes the form of a circular buffer.

RAM

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack \_\_\_\_\_.

Top

Which one flip-flop has an invalid output state?

SR

The output of a NAND gate is \_\_\_\_\_ when all the inputs are one.

Zero

The Transition table is very similar to the \_\_\_\_\_ table.

State

Consider the sum of weight method for converting decimal into binary value, \_\_\_\_\_ is the highest weight for 411.

256

Canonical form is a unique way of representing \_\_\_\_\_.

SOP

\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously.

Synchronous

Cin is part of \_\_\_\_\_ Adder.

Full

Flash memories Operation are classified into \_\_\_\_\_ different operation.

Two

A Product term is 0 when \_\_\_\_\_

Any one literal is 0

In 8-input multiplexer, the two outputs are connected through a/an \_\_\_ gate.

OR

\_\_\_\_\_ Device dissipate varying amount of power depending upon the frequency of operation.

CMOS

Boolean Addition operation is performed by a(an) \_\_\_ gate.

OR

A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.

AND-OR

The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.

$(2^{64})-1$

In 16-bit ALU, The G output is activated if the 4-bit unit generate a Carry \_\_\_\_\_ irrespective of Carry\_\_\_\_\_.

Out,In

A standard POS form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.

Sum

In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles\_\_\_\_\_.

Lower priority inputs

Which of the following is the example of comparator?

XNOR

IN CMOS 5 Volt series, Input voltage of Logic high signal ( $V_{IH}$ ) with a ranges from \_\_\_\_ to \_\_\_\_ volts.

3,5,5

The Adjacent 1 S Detector accepts 4-bits input. If \_\_\_\_ adjacent 1S are detected in the input, the output is set to high.

4

DE Morgan's two theorems prove the equivalency of the NAND and \_\_\_\_ gates and the NOR and \_\_\_\_ gates respectively.

Negative-AND, Negative-OR

Adding two octal numbers "36 and 71" result in \_\_\_\_.

127

Any of the \_\_\_\_ forms of the Karnaugh Map can be used to simplify Boolean expressions

Four

Quine-McCluskey and K-Map methods are used for \_\_\_\_\_ of Boolean expression.

Simplification

The number "1259" may belong to \_\_\_\_\_ number system.

Decimal or Hexadecimal system

The series of TTL chips are characterized by their \_\_\_\_\_.

Switching Speed only

All ABEL statements must end with \_\_\_\_\_.

;

In sequential circuit memory elements are connected with \_\_\_\_\_.

Clock

In the 32-bit Single Precision Floating Point format, the exponent value \_\_\_\_\_ is reserved to represent infinity exponents.

255

The \_\_\_\_\_ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

PLA

The limitation in implementation of parallel binary address is known as \_\_\_\_\_.

Carry input

The Gray code is different from the unsigned binary code because \_\_\_\_\_.

Successive value of Gray code by only one bit

Removing the NOT gate at the output of the NOR gate result in an \_\_\_\_\_.

OR gate

Portable devices that run on batteries use \_\_\_ circuit that have low power dissipation.

Integrated

The domain of the expression  $AB'CD+B$  is

B only

\_\_\_\_\_ is a single input gate

OR

To represent in digital value, the number of digit (0s and 1s) that represent a quantity is \_\_\_ to the range of values that are to be represented.

Equal

BCD code of 16 is \_\_\_\_\_.

00010001

To determine the seven expressions for each of the seven outputs in 7-segment display, seven \_\_\_ variable Karnaugh Maps are used.

3

In Odd parity generator circuit which gate is used to detect parity errors?

XOR

A 3-variable Karnaugh map has

Eight cells

The measurable values generally change over a

Continuous range

\_\_\_\_\_ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.

GAL

When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?

1001

How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decorder?

Three

The simplified expression using either of the two K-maps are\_\_\_\_\_.

Identical

Which of the following expression in the product of sums form?

AB+CD

CMOS technology is characterized by low power dissipation with\_\_\_\_\_ switching speeds.

Slow

GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

True

High level Noise Margins (VNH) of CMOS 5 volt series circuits is\_\_\_\_\_

0.9 V

The output of the expression  $F=A+B+C$  will be Logic \_\_\_\_\_ when  $A=0$ ,  $B=1$ ,  $C=1$ . The symbol "+" here represents OR Gate

One

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be \_\_\_\_\_.

SET

3.3 v CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5 v CMOS series.

Fast switching speeds, very low power dissipation (page61)

The binary value "1010110" is equivalent to decimal \_\_\_\_\_

86

The \_\_\_\_\_ Encoder is used as a keypad encoder.

Decimal-to-BCD Priority

How many data select lines are required for selecting eight inputs?

3

The Quad Multiplexer has \_\_\_\_\_ outputs

4

Demultiplexer has

Single input and multiple outputs.

The expression \_\_\_\_\_ is an example of Commutative Law for Multiplication.

$AB=BA$

The look-ahead carry circuits\_\_\_\_\_

Reduce propagation delay

What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?

$B'+C'D'+CD$

2-input, 8-bit Multiplexer, by setting the S input to logic \_\_\_\_\_ the \_\_\_\_\_ inputs of both the multiplexers are selected.

High, B

The maximum decimal number that can be represented using the 64-bit unsigned representation \_\_\_\_\_

$(2^{64})-1$

When two or more products terms are assumed by Boolean addition, the result is a \_\_\_\_\_

SOP

Tri-State Buffer is a \_\_\_\_\_ gate with a control line that disconnects the

NOT

The 4-bits 2's complement representation of "7" is \_\_\_\_\_

1001

\_\_\_\_\_ and \_\_\_\_\_ are the steps of the Quine-McCluskey.

Find prime implicants and select minimal set of the prime implicants.

The binary number 1011,101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_\_ separated by a decimal point.

1011,101

Subtractors also have output to check if 1 has been \_\_\_\_\_

Borrowed

CMOS technology is characterized by low power dissipation with \_\_\_\_\_ switching speeds.

Slow

The \_\_\_\_\_ description is used to simulate the logic circuit and verify its operation.

Test vector

How many outputs can an integrated circuit comparator have?

Three

Which of the following is not the correct method of grouping?

Diagonally

The output of the expression  $F=A.B.C$  will be logic \_\_\_\_\_ when  $A=1, B=0, C=1$ .

Zero

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.

AND, OR

In the 32-bit Single Precision Floating point format, the exponent value \_\_\_\_\_ is reserved infinity exponent.

99

The Boolean expression  $(AB'CS')$  is used

A product term

The product of an XOR gate is zero(0), when \_\_\_\_\_ All the inputs are zero

I and IV only

\_\_\_\_\_ methods are used to Convert Decimal fractions to Binary.

2

To display the number \_\_\_\_\_ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

29

A SOP expression is equal to I \_\_\_\_\_

When one or more product terms in the expression are equal to 1

The output A B is set to 1 when the input combinations is

A=01, B=10

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

True

High level Noise Margins (V<sub>NH</sub>) of CMOS 5 volt series circuits is \_\_\_\_\_

0.9 V

If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them into floating point representation and then multiplying them, the value of mantissa of result will be

\_\_\_\_\_

24.582 (But not sure)

The output of the expression  $F = A + B + C$  will be Logic \_\_\_\_\_ represents OR Gate.

10(binary)

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be

SET

3.3 V CMOS series is characterized by \_\_\_\_\_ and \_\_\_\_\_ as compared to the 5 V CMOS series.

Fast switch  $\ln 2$  sec delay. Very low lower dissipation Data 1

The binary value "1010110" is equivalent to decimal \_\_\_\_\_

86 (According to Formula)

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

Flip-Flop and DIV 32

DIV 16 and DIV 32

The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)

(n raise to power 2)

(n raise to power 2 and then minus 1)

(2 raise to power n)

(2 raise to power n and then minus 1)

A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state. On the next clock pulse, to what state does the counter go?

1001

1011

0011

1100

A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is \_\_\_\_\_

0001

1111

1000

1110

Divide-by-160 counter is achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

DIV 16 and DIV 32

DIV 16 and DIV 10

A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.

3

7

8

15

RCO stands for \_\_\_\_\_

Reconfiguration Counter Output

Ripple Counter Output

Reconfiguration Clock Output

Ripple Clock Output

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

Clock Skew

Ripple Effect

None of given options

For a down counter that counts from (111 to 000), if current state is "101" the next state will be

\_\_\_\_\_

110

010

None of given options

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

Flip-Flop and DIV 32

Div 10 and DIV 16

Ripple Clock Output

The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins

2

4

6

8

\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously

Asynchronous

Synchronous

Positive-Edge triggered

Negative-Edge triggered

Q : A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.

3

7

8

15

Q : Design of state diagram is one of many steps used to design

A clock

A truncated counter

An UP/DOWN counter

Any counter

Q : A synchronous decade counter will have \_\_\_\_\_ flip-flops

3

4

7

10

Q : Karnaugh map is used in designing

A clock

A counter

An UP/DOWN counter

All of the above

Q : \_\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

Hold and Wait

Clock Skew

Race condition

Hold delay

Q : Three cascaded modulus-10 counters have an overall modulus of

30

100

1000

10000

Q : An Astablemultivibrator is known as a(n) \_\_\_\_\_

Oscillator

Booster

One-shot

Dual-shot

Q: \_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

Clock Skew

Ripple Effect

None of given options

Q: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_

Gated flip-flops

Pulse triggered flip-flops

Positive-Edge triggered flip-flops

Negative-Edge triggered flip-flops

Q: In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together

True

False

Quiz: A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must  $J$  and  $K$  be?

$J = 1, K = 0$

$J = 1, K = X$  (Don't care)

$J = X$  (Don't care),  $K = 0$

$J = 0, K = X$  (Don't care)

Q: The Synchronous counters are also known as Ripple Counters: :

True

False

Q:A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

False

Quiz: The terminal count of a 4-bit binary counter in the DOWN mode is\_\_\_\_\_

0000

0011

1100

1111

Quiz: An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting\_\_\_\_\_

Q output of all flip-flops to clock input of next flip-flops

Q' output of all flip-flops to clock input of next flip-flops

Q output of all flip-flops to J input of next flip-flops

Q' output of all flip-flops to K input of next flip-flops

The terminal count of a modulus-13 binary counter is

0000

1111

1101

1100

Quiz: A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

False

Quiz: A 4-bit UP/DOWN counter is in DOWN mode and in the 1010 state. On the next clock pulse, to what state does the counter go?

1001

1011

0011

1100

Quiz: Design of state diagram is one of many steps used to design

A clock

A truncated counter

An UP/DOWN counter

Any counter

Quiz: An Astable multivibrator is known as a(n) \_\_\_\_\_

Oscillator

Booster

One-shot

Dual-shot

Quiz: The glitches due to "Race Condition" can be avoided by using a \_\_\_\_\_

Gated flip-flops

Pulse triggered flip-flops

Positive-Edge triggered flip-flops

Negative-Edge triggered flip-flops

Quiz: A decade counter is \_\_\_\_\_

Mod-3 counter

Mod-5 counter

Mod-8 counter

Mod-10 counter

The terminal count of a 4-bit binary counter in the DOWN mode is \_\_\_\_\_

0000

0011

1100

1111

The Synchronous counters are also known as Ripple Counters:

True

False

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

Clock Skew

Ripple Effect

None of given options

Divide-by-160 counter is achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

DIV 16 and DIV 32

DIV 16 and DIV 10

Design of state diagram is one of many steps used to design

A clock

A truncated counter

An UP/DOWN counter

Any counter

In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is \_\_\_\_\_

0000

1111

0001

10000