



CS302P

FINAL TERM

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فائل کو پڑھنے سے پہلے اپڈیٹ والے
لفظ پر کلک کر کے اپڈیٹ کر لے کچھ نئے
سوالات اپڈیٹ کیے جاتے ہیں۔

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- The parallel outputs of a counter circuit represent the _____
 - Counter modulus
 - Clock frequency
 - Parallel data word ✓ SPARKY
 - Clock count
- Convert the Gray code 1011 to binary.
 - 1101 ✓ SPARKY
 - 1010
 - 0111
 - 1011
- An identify comparator is defined as a digital comparator which has _____
 - No output terminals
 - Three output terminals za25
 - Two output terminals
 - Only one output terminal ✓ SPARKY
- What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
 - 0 to 2^n
 - 0 to $2^n + 1$
 - 0 to 2^{n+1}

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d. 0 to $2n - 1$ ✓ SPARKY

5. To create a Johnson Counter by using D-flip flops, how flip flops should be connected together?

a. Q' output of previous flip flop should be connected to clock input of second flip flop

b. Q output of previous flip flop should be connected to D input of second flip flop

c. Q' output of previous flip flop should be connected to D input of second flip flop ✓ SPARKY

d. Q output of previous flip flop should be connected to clock input of second flip flop

6. Convert the binary number 1100 to Gray code.

a. 1000

b. 0101

c. 0111

d. 1010 ✓ SPARKY

7. A counter circuit is usually constructed of

a. A number of latches connected in cascade form

b. A number of NOR gates connected in cascade form

c. A number of flip-flops connected in cascade ✓ SPARKY

d. A number of NAND gates connected in cascade form

8. A decimal counter has _____ states.

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- a. 9
- b. 2
- c. 7
- d. 10 ✓ *SPARKY*

9. Three decade counter would have _____

- a. 3 BCD counters ✓ *SPARKY*
- b. 5 BCD counters
- c. 2 BCD counters
- d. 4 BCD counters

10. How many flop flops are required to create a counter circuit which can count from 0 to 7?

- a. 1
- b. 3 ✓ *SPARKY*
- c. 4
- d. 2



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1. The K-map based Boolean reduction is based on the following Unifying Theorem: $A + A' = 1$.
 - a. Non Impact
 - b. **Complementarity** ✓ SPARKY
 - c. Force
 - d. Impact
2. When implementing a half adder by using gates, which of the following gates is used to return carry bit as an output?
 - a. **AND** ✓ SPARKY
 - b. XOR
 - c. OR
 - d. NAND
3. How many select lines would be required for an 8x1 multiplexer?
 - a. 1
 - b. 2
 - c. **3** ✓ SPARKY
 - d. 8
4. A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.
 - a. Block diagram
 - b. **Venn Diagram** ✓ SPARKY
 - c. Cycle Diagram
 - d. Triangular Diagram
5. Which of the following symbols is used to represent XOR operation?
 - a. ^
 - b. x
 - c. +

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Consider a 3-variable Karnaugh Map. How many groups of 1's can be made from the below given Karnaugh Map?

A/BC	00	01	11	10
0	0	1	1	0
1	1	1	1	1

select the correct option

 Reload Math Equations

- 4
- 6
- 2
- 1

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- a. 4
- b. 6
- c. **2** ✓ SPARKY
- d. 1

9. Which of the following gates is used for parity generation for a binary data string?

- a. AND
- b. **XOR** ✓ SPARKY

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- c. OR
- d. NOR

10. Which of the following is not a valid number for grouping of terms in K-Map?

- a. 1
- b. 4
- c. 2
- d. **3** ✓ *SPARKY*



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1. Which of the following gates is used for parity generation for a binary data string?

- a. OR
- b. NOR
- c. AND
- d. **XOR** VU-HB

2. Total number of inputs in a half adder is _____.

- a. 3
- b. **2** VU-HB
- c. 4
- d. 1

3. In order to build an XOR gate using NAND gates only, _____ gate(s) are required.

- a. **4** VU-HB
- b. 2
- c. 3
- d. 1

4. Which of the following expressions represents S output in a full adder?

- a. **$A \oplus B \oplus C_{in}$** VU-HB
- b. $(A \times C_{in}) \oplus B$
- c. $(A \times B) \oplus C_{in}$
- d. $(A+B) \times C_{in}$

5. A half adder can be built by using the combination of _____ and _____ gates.

- a. **AND, XOR** VU-HB
- b. AND, OR
- c. OR, XOR
- d. AND, NOT



1. When implementing a half adder by using gates, which of the following gates is used to return carry bit as an output?

- a. AND
- b. XOR
- c. NAND
- d. OR *

2. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

- a. 0 to $2^n - 1$ *
- b. 0 to $2^n + 1$
- c. 0 to 2^{n+1}
- d. 0 to 2^n

3. Which of the following is the modified code of Excess-3 code?

- a. EBDIC
- b. BCD *
- c. Gray Code
- d. ASCII

4. There are _____ cells in a 4-variable K-map.

- a. 24
- b. 20
- c. 8
- d. 16 *

5. It should be kept in mind that don't care terms should be used along with the terms that are present in _____.

- a. Expressions
- b. Latches
- c. K-Map
- d. **Minterms**

6. In 8x1 multiplexer, which one of the following lines must always be connected to ground in order to activate the multiplexer?

- a. Vcc
- b. **G'**
- c. Y
- d. W

7. A half adder can be built by using the combination of _____ and _____ gates.

- a. **AND, XOR**
- b. OR, XOR
- c. AND, NOT
- d. AND, OR

8. In a full adder circuit having inputs $A = 1$, $B = 1$, $C_{in} = 0$, the outputs S and C_{out} will be _____.

- a. $S = 1$, $C_{out} = 1$
- b. **$S = 0$, $C_{out} = 1$**
- c. $S = 0$, $C_{out} = 0$

- d. $S = 1$, $Cout = 0$
9. There are _____ cells in a 5-variable K-map
- a. 16
 - b. 64
 - c. **32**
 - d. 24
10. Which of the following symbols is used to represent XOR operation?
- a. \wedge
 - b. $+$
 - c. \oplus
 - d. \times



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To draw a logic circuit for boolean expression $AB'+C$, how many gates are used?

a. 3

b. 2 @studywithhamza25

c. 4

d. 1

A K-Map of size 2×2 can be used to map a _____ input boolean expression.

S
2

4 @studywithhamza25

1

3

_____ is also known as a Universal gate.

NOR @studywithhamza25

XNOR

OR

AND

If $Z = (A+B'+C)'$ then Z will be logic high only if

A = 1, B = 1, C = 1 @studywithhamza25

$$A = 0, B = 0, C = 1$$

$$A = 0, B = 1, C = 0$$

$$A = 0, B = 0, C = 0$$

If $Z = A' + B + C' + D$ then what should be the values of A, B, C, and D so that the expression returns $Z = 0$.

$$A = 1, B = 0, C = 0, D = 0 \text{ @studywithhamza25}$$

$$A = 1, B = 0, C = 1, D = 0$$

$$A = 1, B = 0, C = 1, D = 1$$

$$A = 0, B = 1, C = 0, D = 0$$

If $A = 0$ & $B = 1$, What will be the output of $F = (A \cdot B) + A' (A+B)$.

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0

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According to the commutative law of Boolean algebra, which of the following expression is TRUE?

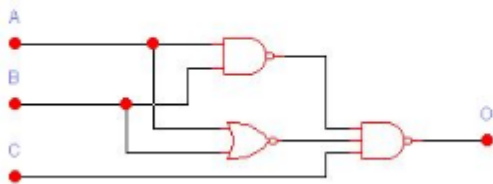
$$A \cdot B = A + B$$

$$A \cdot B = B \cdot A \text{ @studywithhamza25}$$

$$A \cdot B' = A' \cdot B$$

$$A' \cdot B' = A \cdot B$$

What will be the Boolean Expression of the stated Gate Level Diagram.



What will be the Boolean Expression of the stated Gate Level Diagram.

$A'+B+C'$

$A+B+C'$ @studywithhamza25

$A'+B'+C'$

$A+B+C$

The K-map based Boolean reduction is based on the following Unifying Theorem: $A + A' = 1$.

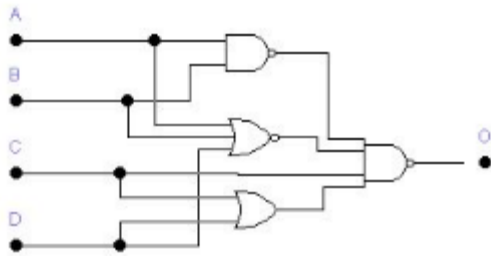
Force

Complementarity @studywithhamza25

Non Impact

Impact

What will be the simplified Boolean Expression of the stated Gate Level Diagram.



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What will be the simplified Boolean Expression of the stated Gate Level Diagram.

$A + B' + C' + D$

$A' + B + C + D'$

$A + B + C' + D$

$A' + B' + C' + D$ @studywithhamza25

If $Z = (A+B'+C)'$ then Z will be logic high only if

$A = 0, B = 1, C = 0$ @studywithhamza25

$A = 0, B = 0, C = 0$

$A = 1, B = 1, C = 1$

$A = 0, B = 0, C = 1$

Don't care conditions can be used for simplifying Boolean expressions in _____.

K-maps @studywithhamza25

Latches

Terms

Registers

_____ gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

Logic @studywithhamza25

Universal

Boolean

Inverse

According to De-Morgan's Law, the expression $(A+BC)'$ is equivalent to _____.

$A'B'+A'C'$ @studywithhamza25

$A' + B' + C'$

$A'B+AC'$

$A'B'+BC$

According to De-Morgan's law, which of the following is TRUE?

$(A + B)' = (A' + B)'$

$$A+B = (A+B)'$$

$$A + B = (A' \cdot B)'$$
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$$A \cdot B = (A' + B)'$$

There are _____ cells in a 5-variable K-map.

32 @studywithhamza25

16

64

24

Which of the following is not a valid number for grouping of terms in K-Map?

4

3 @studywithhamza25

2

1

_____ is also known as a Universal gate.

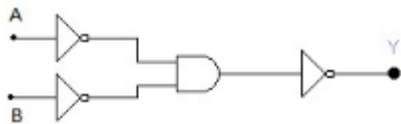
OR

AND

NOR @studywithhamza25

XNOR

What will be the Boolean Equation for (Y) for the given Gate Level Diagram.



What will be the Boolean Equation for (Y) for the given Gate Level Diagram.

A + B

A'B'

A'B @studywithhamza25

A' + B

DE Morgan's Theory is used to convert _____ gates to _____ ones.

OR/NOT, NOT/OR

AND/XOR, XOR/AND

AND/NAND, OR/NOR @studywithhamza25

AND/OR, NOR/NAND

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