CS302P
LAB QUIZZES
FINAL TERM
FALL 2024
BY
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FOR LMS HANDLING
CONTACT
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THE BRAINY SQUAD

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 9 - (Not Graded))

Question # 5 of 5 (Start time: 11:06:49 PM, 10 January 2025)

The parallel outputs of a counter circuit represent the _____

Select the correct option

○	Parallel data word
◉	Counter modulus
○	Clock count
○	Clock frequency

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 9 - (Not Graded))

Question # 4 of 5 (Start time: 11:06:22 PM, 10 January 2025)

Which of the following is the modified code of Excess-3 code?

Select the correct option

◉	Gray Code
○	EBDIC
○	BCD
○	ASCII

Graded))

Question # 3 of 5 (Start time: 11:06:03 PM, 10 January 2025)

A circuit that compares two numbers and determines their magnitude is called __

Select the correct option

○	Size comparator
◉	Magnitude comparator
○	Inverter
○	Height comparator

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 9 - (Not Graded))

Question # 2 of 5 (Start time: 11:05:30 PM, 10 January 2025)

How many flop flops are required to create a counter circuit which can count from 0 to 7?

Select the correct option

○	2
●	3
○	1
○	4

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CS302P - Digital Logic Design (Practical) (Attendance Quiz # 9 - (Not Graded))

Question # 1 of 5 (Start time: 11:05:05 PM, 10 January 2025)

An identify comparator is defined as a digital comparator which has _____

Select the correct option

◉	Only one output terminal
○	Two output terminals
○	Three output terminals
○	No output terminals

Question # 5 of 5 (Start time: 10:46:44 PM, 10 January 2025)

TTL 74LS85 is a _ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Select the correct option

○	8-bit magnitude comparator
○	8-bit word comparator
○	1-bit digital comparator
●	4-bit magnitude comparator

Question # 2 of 5 (Start time: 10:45:44 PM, 10 January 2025)

An identify comparator is defined as a digital comparator which has _

Select the correct option

○	No output terminals
○	Three output terminals
●	Only one output terminal
○	Two output terminals

Graded))

Question # 1 of 5 (Start time: 10:45:25 PM, 10 January 2025)

Comparators are used in _____

Select the correct option

○	Memory
○	Motherboard
○	Hard Drive
●	CPU

Question # 9 of 10 (Start time: 09:30:19 PM, 08 January 2025)

TTL 74LS85 is a _____

Select the correct option

- [ ] 8-bit magnitude comparator
- [ ] 8-bit word comparator
- [x] 4-bit magnitude comparator
- [ ] 1-bit digital comparator

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 8 of 10 (Start time: 09:29:07 PM, 08 January 2025)

The parallel outputs of a counter circuit represent the _____

Select the correct option

○	Parallel data word
○	Counter modulus
◉	Clock count
○	Clock frequency

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 6 of 10 (Start time: 09:28:20 PM, 08 January 2025)

Which one is a basic comparator?

Select the correct option

○	OR
○	NAND
◉	XOR
○	AND

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 5 of 10 (Start time: 09:27:45 PM, 08 January 2025)

Three decade counter would have _____

Select the correct option

○	2 BCD counters
●	3 BCD counters
○	5 BCD counters
○	4 BCD counters

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 4 of 10 (Start time: 09:27:08 PM, 08 January 2025)

Convert the Gray code 1011 to binary.

Select the correct option

◉	1101
○	0111
○	1011
○	1010

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 2 of 10 (Start time: 09:26:16 PM, 08 January 2025)

Reflected Binary Code is also known as _____ code.

Select the correct option

○	BCD
○	ASCII
●	Gray Code
○	Excess-3

Question # 1 of 10 (Start time: 09:25:41 PM, 08 January 2025)

Which of the following is an invalid BCD code?

Select the correct option

○	1001
○	0011
●	1101
○	0101

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04) Quiz

Question # 10 of 10 (Start time: 08:31:41 PM, 08 January 2025)

A counter circuit is usually constructed of _____

Select the correct option

- ○ A number of latches connected in cascade form
- ○ A number of NOR gates connected in cascade form
- ○ A number of NAND gates connected in cascade form
- ◉ A number of flip-flops connected in cascade

Click to S

Question # 9 of 10 (Start time: 08:31:34 PM, 08 January 2025)

Comparators are used in _____

Select the correct option

○	Hard Drive
○	CPU
○	Motherboard
○	Memory

Question # 8 of 10 (Start time: 08:30:10 PM, 08 January 2025)

What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

Select the correct option

Reloc

- (●) 0 to $2^n - 1$
- ( ) 0 to $2^n + 1$
- ( ) 0 to 2^n
- ( ) 0 to 2^{n+1}

Click to Save Answer & Move

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04) **Quiz Start Time: 08:26 P**

Question # 8 of 10 (Start time: 08:30:10 PM, 08 January 2025)

What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

Select the correct option

Reloc

- (●) 0 to $2^n - 1$
- ( ) 0 to $2^n + 1$
- ( ) 0 to 2^n
- ( ) 0 to 2^{n+1}

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 7 of 10 (Start time: 08:29:38 PM, 08 January 2025)

An identify comparator is defined as a digital comparator which has _____

Select the correct option

○	No output terminals
○	Two output terminals
○	Three output terminals
◉	Only one output terminal

Question # 6 of 10 (Start time: 08:29:13 PM, 08 January 2025)

Three decade counter would have _____

Select the correct option

○	2 BCD counters
●	3 BCD counters
○	5 BCD counters
○	4 BCD counters

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 5 of 10 (Start time: 08:28:33 PM, 08 January 2025)

A decimal counter has _____ states.

Select the correct option

○	2
●	10
○	9
○	7

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 4 of 10 (Start time: 08:27:58 PM, 08 January 2025)

Ripple counters are also called _____

Select the correct option

○	VLSI counters
●	Asynchronous counters
○	Synchronous counters
○	SSI counters

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 3 of 10 (Start time: 08:27:21 PM, 08 January 2025)

Why do we use Gray Code?

Select the correct option

○	Invert the code
○	Error Detection
◉	To count the number or bit changes
○	Error Correction

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 2 of 10 (Start time: 08:26:37 PM, 08 January 2025)

Which of the following is the modified code of Excess-3 code?

Select the correct option

◉	BCD
○	Gray Code
○	ASCII
○	EBDIC

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 1 of 10 (Start time: 08:26:05 PM, 08 January 2025)

In a comparator, if we get input as A>B then the output will be _____

Select the correct option

○	0
○	A
○	B
◉	1

Question # 10 of 10 (Start time: 07:28:07 PM, 08 January 2025)

In a comparator, if we get input as A>B then the output will be _____

Select the correct option

○	A
○	0
●	1
○	B

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 9 of 10 (Start time: 07:27:34 PM, 08 January 2025)

Which one is a basic comparator?

Select the correct option

- ○ OR
- ○ NAND
- ◉ XOR
- ○ AND

Question # 8 of 10 (Start time: 07:27:00 PM, 08 January 2025)

Convert the Gray code 1011 to binary.

Select the correct option

◉	1101
○	1010
○	1011
○	0111

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 7 of 10 (Start time: 07:26:29 PM, 08 January 2025)

A counter circuit is usually constructed of _____

Select the correct option

○	A number of NOR gates connected in cascade form
○	A number of NAND gates connected in cascade form
●	A number of flip-flops connected in cascade
○	A number of latches connected in cascade form

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 6 of 10 (Start time: 07:25:44 PM, 08 January 2025)

The parallel outputs of a counter circuit represent the _____

Select the correct option

◉	Counter modulus
○	Parallel data word
○	Clock frequency
○	Clock count

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 5 of 10 (Start time: 07:25:07 PM, 08 January 2025)

Which of the following is the modified code of Excess-3 code?

Select the correct option

○	ASCII
○	BCD
○	EBDIC
◉	Gray Code

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 4 of 10 (Start time: 07:24:25 PM, 08 January 2025)

Comparators are used in _____

Select the correct option

○	Memory
○	Motherboard
◉	CPU
○	Hard Drive

Question # 3 of 10 (Start time: 07:23:58 PM, 08 January 2025)

An identify comparator is defined as a digital comparator which has _____

Select the correct option

○	No output terminals
○	Three output terminals
●	Only one output terminal
○	Two output terminals

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04)

Question # 2 of 10 (Start time: 07:23:33 PM, 08 January 2025)

Ripple counters are also called _____

Select the correct option

○	VLSI counters
○	SSI counters
○	Synchronous counters
◉	Asynchronous counters

Question # 1 of 10 (Start time: 07:22:59 PM, 08 January 2025)

A decimal counter has _____ states.

Select the correct option

○	2
○	9
○	7
●	10

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 8 - (Not Graded))

Quiz Start Time: 02:37 AM, 03 January 2025

Question # 4 of 5 (Start time: 02:40:39 AM, 03 January 2025) **Total Marks:** 1

The parallel outputs of a counter circuit represent the _____

Select the correct option

Reload Math Equations

○	Parallel data word
○	Clock frequency
◉	Clock count
○	Counter modulus

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 8 - (Not Graded))

Quiz Start Time: 02:37 AM, 03 January 2025

Question # 3 of 5 (Start time: 02:40:04 AM, 03 January 2025) **Total Marks:** 1

Convert the binary number 1100 to Gray code.

Select the correct option

Reload Math Equations

○	0111
○	1000
◉	1010
○	0101

Click to Save Answer & Move to Next Question

sec(s)

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 8 - (Not Graded))

Quiz Start Time: 02:37 AM, 03 January 2025

Question # 2 of 5 (Start time: 02:39:23 AM, 03 January 2025) **Total Marks:** 1

What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

Select the correct option

Reload Math Equations

◉	0 to $2^n - 1$
○	0 to 2^{n+1}
○	0 to $2^n + 1$
○	0 to 2^n

Click to Save Answer & Move to Next Question

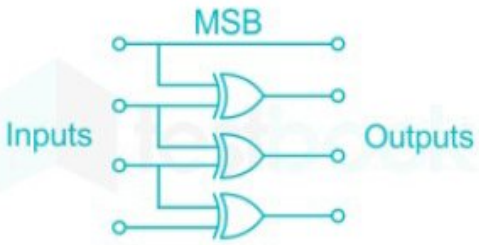
sec(s)

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 8 - (Not Graded))

Quiz Start Time: 02:37 AM, 03 January 2025

Question # 1 of 5 (Start time: 02:37:31 AM, 03 January 2025) **Total Marks:** 1

Following diagram is of _____ code conversion.



Select the correct option

Reload Math Equations

- (●) Gray
- ( ) Excess-3
- ( ) BCD
- ( ) ASCII

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 8 - (Not Graded))

Question # 5 of 5 (Start time: 01:14:47 AM, 03 January 2025)

Why do we use Gray Code?

Select the correct option

- ○ To count the number or bit changes
- ◉ Error Correction
- ○ Invert the code
- ○ Error Detection

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 8 - (Not Graded))

Question # 4 of 5 (Start time: 01:14:02 AM, 03 January 2025)

How many flop flops are required to create a counter circuit which can count from 0 to 7?

Select the correct option

○	1
○	2
◉	3
○	4

Question # 3 of 5 (Start time: 01:13:28 AM, 03 January 2025)

Which of the following is the modified code of Excess-3 code?

Select the correct option

- (●) Gray Code
- ( ) BCD
- ( ) EBDIC
- ( ) ASCII

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 8 - (Not Graded))

Question # 2 of 5 (Start time: 01:12:36 AM, 03 January 2025)

A counter circuit is usually constructed of _____

Select the correct option

○	A number of NAND gates connected in cascade form
◉	A number of flip-flops connected in cascade
○	A number of latches connected in cascade form
○	A number of NOR gates connected in cascade form

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 8 - (Not Graded))

Quiz Start Time: 01:11 AM

Question # 1 of 5 (Start time: 01:11:53 AM, 03 January 2025)

What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

Select the correct option

Reload

- ○ 0 to $2^n + 1$
- ○ 0 to 2^n
- ◉ 0 to $2^n - 1$
- ○ 0 to 2^{n+1}

Click to Save Answer & Move to N

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CS302P - Digital Logic Design (Practical) (Semester Quiz # 03) Quiz Start

Question # 10 of 10 (Start time: 11:10:55 PM, 02 January 2025)

A K-Map of size 2x2 can be used to map a _____ input boolean expression.

Select the correct option

- (●) 2
- ( ) 4
- ( ) 3
- ( ) 1

Click to Save An

Question # 9 of 10 (Start time: 11:10:14 PM, 02 January 2025) To

A full adder circuit takes _____ bit(s) as input and returns _____ bit(s) as output.

Select the correct option

Reload Math E

- [ ] 2, 1
- [x] 3, 2
- [ ] 2, 2
- [ ] 3, 1

Click to Save Answer & Move to Next Q

Question # 8 of 10 (Start time: 11:09:16 PM, 02 January 2025) **Tota**

It should be kept in mind that don't care terms should be used along with the terms that are present in _____.

Select the correct option

Reload Math Equ

○	Expressions
●	K-Map
○	Minterms
○	Latches

Click to Save Answer & Move to Next Que

Question # 7 of 10 (Start time: 11:08:46 PM, 02 January 2025)

Each product term of a group, w'xy' and wy, represents the _____ in that group.

Select the correct option

- ○ Sum of Maxterms
- ○ POS
- ◉ Sum of Minterms
- ○ Input

Click to Save Answer &

Question # 6 of 10 (Start time: 11:08:11 PM, 02 January 2025)

Don't care conditions can be used for simplifying Boolean expressions in _____.

Select the correct option

- ○ Terms
- ● K-maps
- ○ Registers
- ○ Latches

Click to Save A

Question # 5 of 10 (Start time: 11:06:47 PM, 02 January 2025)

Which of the following is not a valid number for grouping of terms in K-Map?

Select the correct option

○	1
○	4
◉	2
○	3

Click to Save Answe

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Quiz Start Time: 11:04 PM, 02 January 2025

Question # 4 of 10 (Start time: 11:05:58 PM, 02 January 2025)

Total Marks: 1

A half adder can be built by using the combination of _____ and _____ gates.

Select the correct option

Reload Math Equations

- (●) AND, XOR
- ( ) OR, XOR
- ( ) AND, NOT
- ( ) AND, OR

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03) Quiz Start Time: 11:04 PM, 02 January 2025

Question # 2 of 10 (Start time: 11:04:54 PM, 02 January 2025) **Total Marks:** 1

When implementing a half adder by using gates, which of the following gates is used to give Sum (S) as an output?

Select the correct option

Reload Math Equations

○	NOR
○	AND
◉	XOR
○	OR

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 1 of 10 (Start time: 11:04:30 PM, 02 January 2025)

Total number of inputs in a half adder is _____.

Select the correct option

○	1
●	2
○	4
○	3

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Question # 10 of 10 (Start time: 10:55:42 PM, 02 January 2025)

The K-map based Boolean reduction is based on the following Unifying Theorem: $A + A' = 1$.

Select the correct option

Relo

○	Impact
◉	Complementarity
○	Force
○	Non Impact

Click to Save Answer & Move

Question # 9 of 10 (Start time: 10:54:49 PM, 02 January 2025)

Total Ma

It should be kept in mind that don't care terms should be used along with the terms that are present in _____.

Select the correct option

Reload Math Equatio

- (●) Expressions
- ( ) Minterms
- ( ) Latches
- ( ) K-Map

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Quiz Start Time: 10:48 PM, 02 January 2025

Question # 8 of 10 (Start time: 10:53:47 PM, 02 January 2025)

Total Marks:

In 8x1 multiplexer, which one of the following lines must always be connected to ground in order to activate the mutiplexer?

Select the correct option

Reload Math Equations

- (●) G'
- ( ) Vcc
- ( ) Y
- ( ) W

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 7 of 10 (Start time: 10:52:59 PM, 02 January 2025)

Which of the following symbols is used to represent XOR operation?

Select the correct option

○	+
○	^
◉	⊕
○	X

Click t

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 6 of 10 (Start time: 10:52:23 PM, 02 January 2025)

There are _____ cells in a 4-variable K-map.

Select the correct option

○	8
○	20
●	16
○	24

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Quiz Start Time: 10:48 PM, 02 January 2025

Question # 5 of 10 (Start time: 10:51:51 PM, 02 January 2025)

Total Marks: 1

When implementing a half adder by using gates, which of the following gates is used to return carry bit as an output?

Select the correct option

Reload Math Equations

- (●) AND
- ( ) XOR
- ( ) OR
- ( ) NAND

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 4 of 10 (Start time: 10:51:02 PM, 02 January 2025)

Which of the following is not a valid number for grouping of terms in K-Map?

Select the correct option

◉	3
○	4
○	2
○	1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Quiz Start Time: 10:48 PM, 02 January

Question # 3 of 10 (Start time: 10:49:58 PM, 02 January 2025)

Total Mo

When implementing a half adder by using gates, which of the following gates is used to give Sum (S) as an output?

Select the correct option

Reload Math Equatio

- [ ] AND
- [x] XOR
- [ ] NOR
- [ ] OR

Click to Save Answer & Move to Next Questio

Question # 2 of 10 (Start time: 10:48:52 PM, 02 January 2025)

Consider a 3-variable Karnuagh Map. How many groups of 1's can be made from the below given Karnaugh Map?

A/BC	00	01	11	10
0	0	1	1	0
1	1	1	1	1

Select the correct option

Reload Math

- (●) 1
- ( ) 4
- ( ) 2
- ( ) 6

Click to Save Answer & Move to Next

Question # 1 of 10 (Start time: 10:48:10 PM, 02 January 2025)

In order to build an XOR gate using NAND gates only, _____ gate(s) are required.

Select the correct option

○	2
○	3
●	4
○	1

Click to Save Answer &

Time Left sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Quiz Start Time: 12:16 PM, 02 January 2025

Question # 10 of 10 (Start time: 12:25:03 PM, 02 January 2025)

Total Marks: 1

When implementing a half adder by using gates, which of the following gates is used to return carry bit as an output?

Select the correct option

Reload Math Equations

- XOR
- AND
- NAND
- OR

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 7 of 10 (Start time: 12:21:47 PM, 02 January 2025)

It should be kept in mind that don't care terms should be used along with the terms that are present in _____.

Select the correct option

- Latches
- Expressions
- Minterms
- K-Map

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

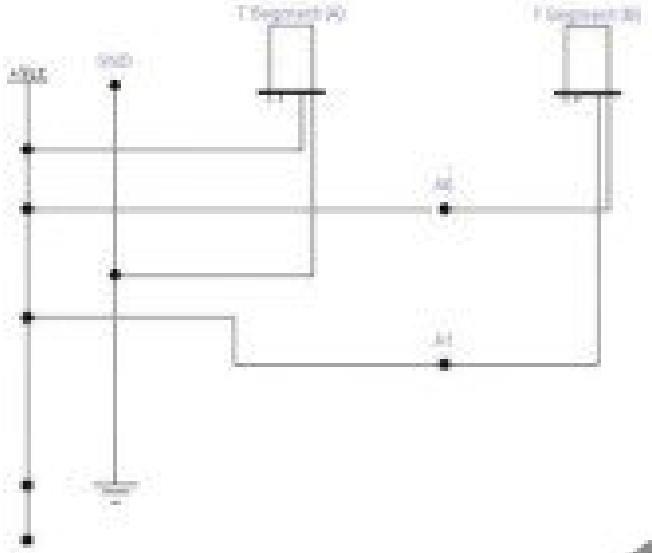
Question # 8 of 10 (Start time: 12:22:43 PM, 02 January 2025)

There are _____ cells in a 5-variable K-map.

Select the correct option

- ○ 64
- ○ 16
- ○ 24
- ◉ 32

Consider the below given EWB circuit, what values will be displayed on 7-segment displays A and B when the circuit simulation is activated in EWB?



Select the correct option

- 1, 3
- 3, 3
- 2, 3
- 0, 1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 6 of 10 (Start time: 12:21:02 PM, 02 January 2025)

A K-Map of size 2x2 can be used to map a _____ input boolean expression.

Select the correct option

- (●) 4
- ( ) 3
- ( ) 2
- ( ) 1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 3 of 10 (Start time: 12:10:59 PM, 02 January 2025)

Each product term of a group, w'x'y' and wy, represents the _____ in that group.

Select the correct option

- ○ Sum of Maxterms
- ◉ Sum of Minterms
- ○ Input
- ○ POS

Consider a 3-variable Karnaugh Map. How many groups of 1's can be made from the below given Karnaugh Map?

A/BC	00	01	11	10
0	0	1	1	0
1	1	1	1	1

Select the correct option

- ○ 1
- ● 4
- ○ 6
- ○ 2

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 2 of 10 (Start time: 12:16:29 PM, 02 January 2025)

How many select lines would be required for an 8x1 multiplexer?

Select the correct option

- 8
- 1
- 3
- 2

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03)

Question # 1 of 10 (Start time: 12:16:02 PM, 02 January 2025)

Each group of adjacent Minterms (group size in powers of twos) corresponds to a possible product term of the given _____

Select the correct option

- Word
- Function
- Value
- Set

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:48 AM, 27 December 2024

Question # 1 of 5 (Start time: 02:48:28 AM, 27 December 2024)

Total Marks: 1

The parallel outputs of a counter circuit represent the _____

Select the correct option

Reload Math Equations

- (●) Clock count
- ( ) Parallel data word
- ( ) Clock frequency
- ( ) Counter modulus

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:48 AM, 27 December 2024

Question # 2 of 5 (Start time: 02:48:59 AM, 27 December 2024)

Total Marks:

Three decade counter would have _____

Select the correct option

Reload Math Equations

- 5 BCD counters
- 4 BCD counters
- 2 BCD counters
- 3 BCD counters

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:48 AM, 27 December 2024

Question # 3 of 5 (Start time: 02:49:21 AM, 27 December 2024)

Total Marks: 1

A counter circuit is usually constructed of _____

Select the correct option

Reload Math Equations

- A number of NAND gates connected in cascade form
- A number of latches connected in cascade form
- A number of flip-flops connected in cascade
- A number of NOR gates connected in cascade form

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:48 AM, 27 December 2024

Question # 4 of 5 (Start time: 02:49:52 AM, 27 December 2024)

Total Marks: 1

How many select lines would be required for an 8x1 multiplexer?

Select the correct option

Reload Math Equations

- 6
- 1
- 3
- 2

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:52 AM, 27 December 2024

Question # 1 of 5 (Start time: 02:52:38 AM, 27 December 2024) **Total Marks:** 1

In 8x1 multiplexer, which one of the following lines must always be connected to ground in order to activate the mutiplexer?

Select the correct option

Reload Math Equations

- W
- Y
- G'
- Vcc

Click to Save Answer & Move to Next Question

sec(s)

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:52 AM, 27 December 2024

Question # 2 of 5 (Start time: 02:53:18 AM, 27 December 2024) **Total Marks:** 1

The parallel outputs of a counter circuit represent the _____

Select the correct option

Reload Math Equations

- (●) Clock count
- ( ) Clock frequency
- ( ) Parallel data word
- ( ) Counter modulus

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:52 AM, 27 December 2024

Question # 3 of 5 (Start time: 02:53:40 AM, 27 December 2024)

Total Marks: 1

Ripple counters are also called _____

Select the correct option

Reload Math Equations

- (●) Asynchronous counters
- ( ) SSI counters
- ( ) VLSI counters
- ( ) Synchronous counters

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:52 AM, 27 December 2024

Question # 4 of 5 (Start time: 02:54:04 AM, 27 December 2024)

Total Marks: 1

How many select lines would be required for an 8x1 multiplexer?

Select the correct option

Reload Math Equations

- [ ] 1
- [x] 3
- [ ] 8
- [ ] 2

Click to Save Answer & Move to Next Question

sec(s)

CS302P - Digital Logic Design (Practical) (Attendance Quiz # 7 - (Not Graded))

Quiz Start Time: 02:52 AM, 27 December 2024

Question # 5 of 5 (Start time: 02:54:28 AM, 27 December 2024) **Total Marks:**

A counter circuit is usually constructed of _____

Select the correct option

Reload Math Equations

- A number of NAND gates connected in cascade form
- A number of latches connected in cascade form
- A number of flip-flops connected in cascade
- A number of NOR gates connected in cascade form

Click to Save Answer & Move to Next Question

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