

Question # 4 of 5 (Start time: 12:37:34 PM, 07 July 2023)

Total Marks: 1

In a full adder circuit having inputs $A = 1$, $B = 1$, $C_{in} = 0$, the outputs S and C_{out} will be

Select the correct option

[Reload Math Equations](#) $S = 1, C_{out} = 1$ $S = 1, C_{out} = 0$ $S = 0, C_{out} = 1$ 

Question # 5 of 5 (Start time: 12:38:39 PM, 07 July 2023)

Total Marks: 1

Which of the following gates is used for parity generation for a binary data string?

Select the correct option

[Reload Math Equations](#) XOR AND OR

A half adder can be built by using the combination of _____ and _____ gates.

Select the correct option

 Reload Math Equations

- AND, XOR
 - AND, NOT
 - AND, OR
 - OR, XOR
- 

When implementing a half adder by using gates, which of the following gates is used to give Sum (S) as an output?

Select the correct option

 Reload Math Equations

- | | |
|----------------------------------|-----|
| <input type="radio"/> | OR |
| <input checked="" type="radio"/> | AND |
| <input type="radio"/> | XOR |
| <input type="radio"/> | NOR |