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A Good Education is a Foundation For a Better Future

CORRECT ANSWER SOLVED BY HADI
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(Final Term Past Paper)

MADE AND SOLVED BY TEAM HADI

WARNING: Team HADI is not responsible for any mistake or wrong answer. All students reading and using this document may check and confirm the answers at their own.



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Best of luck!



What is the size of the memory space that is available to **SRC processor**?

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Answer (Please select your correct option)

2⁸ bytes

2¹⁶ bytes

2³² bytes



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2⁶⁴ bytes

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Which one of the following is the memory organization of **SRC processor**?

Answer (Please select your correct option)

$2^8 * 8$ bits

$2^{16} * 8$ bits

$2^{32} * 8$ bits

$2^{64} * 8$ bits



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In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?

Answer (Please select your correct option)

- Direct Addressing Mode
- Immediate addressing mode
- Indirect Addressing Mode
- Register (Direct) Addressing Mode



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Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?

Answer (Please select your correct option)

- :=  correct answer solved by hadi
- &
- %
- ©

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Question No : 5 of 52

Marks: 1 (Budgeted Time 1 Min)

Which one of the following register holds the address of the next instruction to be executed?

Answer (Please select your correct option)

- Accumulator
- Address Mask
- Instruction Register
- Program Counter

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Question No : 6 of 52

Marks: 1 (Budgeted Time 1 Min)

Which one of the following register holds the instruction that is being executed?

Answer (Please select your correct option)

Accumulator

Address Mask

Instruction Register

Program Counter



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Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

Answer (Please select your correct option)

Processor-Memory-Switch level (PMS level)



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Instruction Set Level

Register Transfer Level

Logic design level

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Which one of the following design levels is called the gate level?

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Answer (Please select your correct option)

Logic Design Level



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Circuit Level

Mask Level

Register transfer Level

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_____ Instructions usually involve calculating the target address and evaluating a condition.

Answer (Please select your correct option)

Add

Branch

Load

Store



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Which one of the following instructions is used to load register from memory using a relative address?

Answer (Please select your correct option)

la

nop

ldr

str



correct answer
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An interface that is used to connect the computer bus with I/O devices is called _____.

Answer (Please select your correct option)

- Buffer
- I/O port
- Memory mapping
- Processor



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Every I/O port has a unique identifier associated with it, which is called its -----

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Answer (Please select your correct option)

- Address
- Access point
- Interval Identifier
- Device driver

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_____ refers to the situation in which all I/O operations are performed under the direct control of a program running on the CPU.

Answer (Please select your correct option)

Direct memory access



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Virtual memory

Partial decoding

Programmed I/O

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_____ is the process of periodically checking the status of a device to see if it is ready for the next I/O operation.

Answer (Please select your correct option)

Polling



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Snooping

Data Bus Multiplexing

Pipelining

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Question No : 15 of 52

Marks: 1 (Budgeted Time 1 Min)

Which one of the following is NOT a technique used when the CPU wants to exchange data with peripheral device?

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Answer (Please select your correct option)

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Direct Memory Access

Interrupt driven I/O

Programmed I/O

Virtual Memory



correct answer
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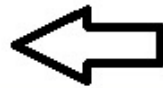
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Which one is the last instruction of the ISR that is to be executed when the ISR terminates?

Answer (Please select your correct option)

IRET



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IRQ

INT

NMI

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----- is the time needed by the CPU to recognize (not service) an interrupt request.

Answer (Please select your correct option)

Interrupt Latency



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Response Deadline

Timer delay

Throughput

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In Multiple Interrupt Lines approach, a number of interrupt lines are provided between the _____ modules.

Answer (Please select your correct option)

External and Internal

CPU and I/O

CPU and Memory

Memory and I/O



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Falcon-A Simulator loads a FALCON-A binary file with a _____ extension and presents its contents into different areas of the simulator.

Answer (Please select your correct option)

.bin

.binfa

.fa

.asmfa

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Question No : 20 of 52

Marks: 1 (Budgeted Time 1 Min)

In Direct memory access (DMA), a _____ is needed to control the total activity and to synchronize the transfer of data.

Answer (Please select your correct option)

DMA memory unit

DMA controller

Control software

Programmed I/O



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_____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

Answer (Please select your correct option)

Programmed I/O

Interrupt driven I/O

Direct memory access

Polling



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Taking control of the system bus for a few bus cycles is known as _____.

Answer (Please select your correct option)

Bus Scheduling

Cycle Stealing

Cycle Transferring

CPU Scheduling



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A component connected to the system bus and having control of it during a particular bus cycle is called _____.

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Answer (Please select your correct option)

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Address decoder

BIOS

Master component



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Slave component

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Question No : 24 of 52

Marks: 1 (Budgeted Time 1 Min)

CRC has _____ overhead as compared to Hamming code.

Answer (Please select your correct option)

- Equal
- Greater
- Lesser
- Absolutely no



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Question No : 25 of 52

Marks: 1 (Budgeted Time 1 Min)

We represent e^{\wedge} instead of e to show _____.

Answer (Please select your correct option)

Sign Magnitude Form

Radix Complement Form

Diminished Radix Compliment Form

Biased Representation



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In floating point representations _____ is also called mantissa.

Answer (Please select your correct option)

Sign

Base

Significand

Exponent



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_____ occurs when the exponent is too large and can not be represented in the exponent field.

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Answer (Please select your correct option)

Underflow

Overflow

Rounding Off

Normalization



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Question No : 28 of 52

Marks: 1 (Budgeted Time 1 Min)

In Double-Precision Binary Floating Point Representation the size of fraction is _____.

Answer (Please select your correct option)

23-bits

52-bits

11-bits

1-bits



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Question No : 29 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is a combination of arithmetic, logic and shifter unit along with some multiplexers.

Answer (Please select your correct option)

Computer Bus

CPU Register

Flip Flop

ALU

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_____ is a place for safe storage and provides the fastest possible storage after the registers.

Answer (Please select your correct option)

Hard Disk

Cache

Compact Disk

Floppy Disk



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_____ is nonvolatile i.e. it retains the information in it when power is removed from it.

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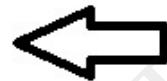
Answer (Please select your correct option)

RAM

DRAM

ROM

SRAM



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Based on the statistical results, the cache block which has been least used in the recent past, is replaced with a new block. This technique is called _____.

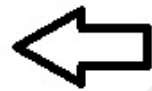
Answer (Please select your correct option)

Always Replacement

Random Replacement

LFU (Least Frequently Used)

Write Allocate



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Question No : 33 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ acts as a cache between main memory and secondary memory.

Answer (Please select your correct option)

Read Only Memory

Flash Memory

Virtual Memory

Magnetic Tape

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In _____ technique memory is divided into segments of variable sizes depending upon the requirements.

Answer (Please select your correct option)

Multiplexing

Segmentation

Hamming code

Partial decoding



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Question No : 35 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is the maximum rate at which data can be transmitted through networks.

Answer (Please select your correct option)

Transmission Time

Latency

Transport Latency

Bandwidth

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Question No : 36 of 52

Marks: 1 (Budgeted Time 1 Min)

In physical media of networks, for increased and better performance we use _____ which are usually made of glass.

Answer (Please select your correct option)

Coaxial Cables

Twisted Pair Cables

Fiber Optic Cables

Shielded Twisted Pair Cables



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Question No : 37 of 52

Marks: 1 (Budgeted Time 1 Min)

In _____ topology, all the computers are connected in the form of a circle.

Answer (Please select your correct option)

Bus

Ring

Mesh

Star

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Connection Oriented Communication reserves the _____ until the transfer is completed.

Answer (Please select your correct option)

Bandwidth



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Error

Checksum

Protocol

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Question No : 39 of 52

Marks: 1 (Budgeted Time 1 Min)

In connection-less communication message is divided into _____.

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Answer (Please select your correct option)

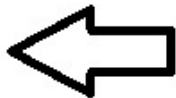
Tracks

Sectors

Platters

Packets

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Question No : 40 of 52

Marks: 1 (Budgeted Time 1 Min)

SPARC (Scalable Processor Architecture) is an example of _____ architecture.

Answer (Please select your correct option)

CISC

RISC

SRC

FALCON



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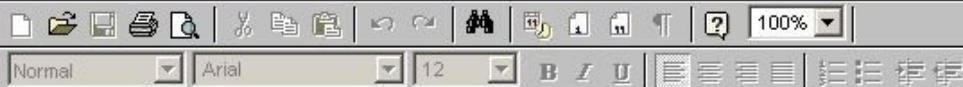
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Differentiate between Latency and throughput.

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Answer (Please [click here to Add Answer](#))



Latency is defined as the time required to process a single instruction, while throughput is defined as the number of instructions processed per second

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Which attributes a device should have in order to be qualified as a master device?

Answer (Please [click here to Add Answer](#))



A Master must have the capability to place addresses on the address bus and direct the bus activity during a buscycle

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Differentiate between Spatial Locality and Temporal Correlation.

Answer (Please [click here to Add Answer](#))

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Spatial Locality This would mean that in a part of a program, if we have a particular address being accessed then it is highly probable that the data available at the next address would be highly accessed.

Temporal Correlation In this case, we say that at a particular time, if we have utilized a particular part of the memory then we might access the adjacent parts very soon.

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Question No : 44 of 52

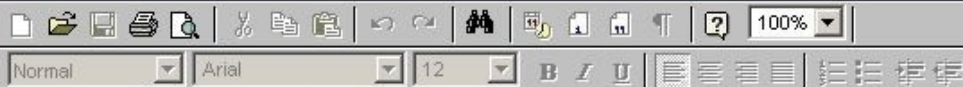
Marks: 2 (Budgeted Time 4 Min)

Name any two methods that are used to measure I/O subsystem performance.

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Answer (Please [click here to Add Answer](#))



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Differentiate between sender overhead and receiver overhead related to performance issues of networks.

Answer (Please [click here to Add Answer](#))

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Normal Arial 12 B I U

Sender overhead It is the time for the processor to inject message in to the network.

Receiver overhead It is the time for the processor to pull the message from the network.

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Question No : 46 of 52

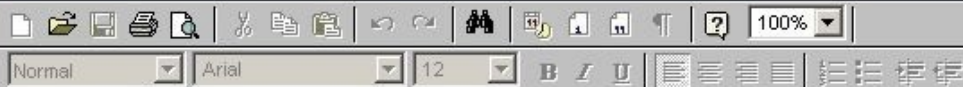
Marks: 3 (Budgeted Time 6 Min)

Write down the categories of instructions supported by FALCON-A processor and also state that in type 1 instruction format of FALCON-A, how many bits are reserved for the op-code?

Answer (Please [click here to Add Answer](#))

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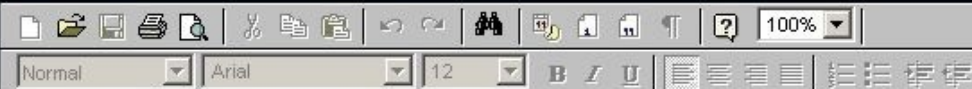
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Find the average rotational latency (in milliseconds) of the disk if it rotates at 15,000 rpm.

Answer (Please [click here to Add Answer](#))

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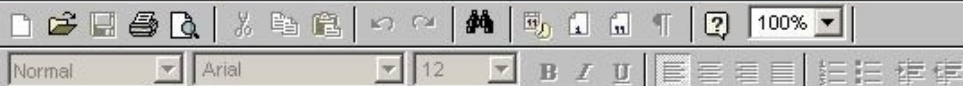
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If a DRAM has 512 rows and its refresh time is 8ms, what should be the average frequency of row refresh operation?

Answer (Please [click here to Add Answer](#))

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Refresh time =8ms

Number of rows =512

Therefore we have to do 512 row refresh operations in a 9 ms interval, in other words

one row refresh operation every $= (8 * 10^{-3}) / 512$
 $= 1.56 * 10^{-5}$ second

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Briefly explain the following features of FALCON-E.

- a. Number of registers
- b. Size of each register
- c. Memory word size
- d. Memory space

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Answer (Please [click here to Add Answer](#))



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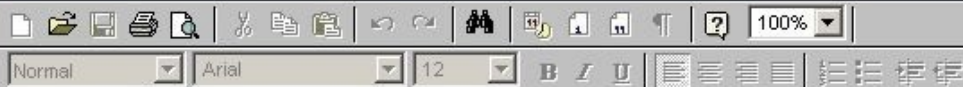
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Explain briefly how the interrupting module is identified in software polling and also point out the major drawback of Software Poll and Daisy Chain.

Answer (Please [click here to Add Answer](#))

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According to the Radix conversion algorithm, convert the hexadecimal number $C4_{16}$ to base 10 (Write down all the steps which are involved in conversion).

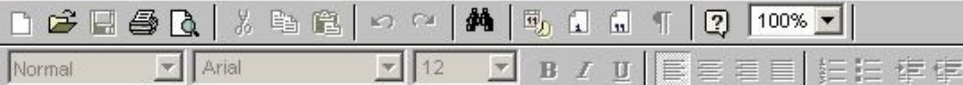
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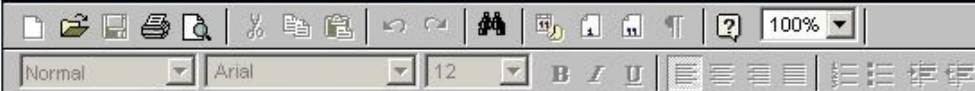
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Find the average access time of a level of memory hierarchy if the hit rate is 80%. The memory access takes 10ns on a hit and 100ns on a miss.

Answer (Please [click here to Add Answer](#))

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