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A Good Education is a Foundation For a Better Future

CORRECT ANSWER SOLVED BY HADI
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(Final Term Past Paper)

MADE AND SOLVED BY TEAM HADI

WARNING: Team HADI is not responsible for any mistake or wrong answer. All students reading and using this document may check and confirm the answers at their own.



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Best of luck!



Question No : 1 of 52

Marks: 1 (Budgeted Time 1 Min)

What does the instruction "ldr R3, 58" of SRC do?

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Answer (Please select your correct option)

it will load the register R3 with the contents of the memory location M [PC+58]

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correct answer

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It will load the register R3 with the relative address itself (PC+58).

It will store the register R3 contents to the memory location M [PC+58]

No operation

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Question No : 2 of 52

Marks: 1 (Budgeted Time 1 Min)

What functionality is performed by the instruction "lar R3, 36" of SRC?

Answer (Please select your correct option)

- it will load the register R3 with the contents of the memory location M [PC+36]
- It will load the register R3 with the relative address itself (PC+36).
- It will store the register R3 contents to the memory location M [PC+36]
- No operation

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What is the instruction length of the SRC processor?

Answer (Please select your correct option)

8 bits

16 bits

32 bits

64 bits

TEAM HADI(VU)



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Question No : 4 of 52

Marks: 1 (Budgeted Time 1 Min)

What does the word 'D' in the 'D-flip-Flop' stands for?

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Answer (Please select your correct option)

Data 

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Digital

Dynamic

Double

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Question No : 5 of 52

Marks: 1 (Budgeted Time 1 Min)

Almost every commercial computer has its own particular ----- language

Answer (Please select your correct option)

assembly language



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English language

Higher level language

3GL

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Question No : 6 of 52

Marks: 1 (Budgeted Time 1 Min)

Which field of the machine language instruction is the "**type of operation**" that is to be performed?

Answer (Please select your correct option)

Op-code (or the operation code)



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CPU registers

Memory cells

I/O locations

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_____ is/are defined as the time required processing a single instruction.

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Answer (Please select your correct option)

Latency and Throughput

Latency



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Throughput

Hazards

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In pipelining ----- is increased by overlapping the instruction execution

Answer (Please select your correct option)

Latency

Throughput

Execution time

Clock speed

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Which of the following register(s) takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system?

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Answer (Please select your correct option)

Instruction Register

Memory address register

Memory Buffer Register

Registers A and C

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In which one of the following addressing modes, data is the part of the instruction itself, and so there is no need of address calculation?

Answer (Please select your correct option)

Direct Addressing Mode



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Immediate addressing mode

Indirect Addressing Mode

Register (Direct) Addressing Mode

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Question No : 11 of 52

Marks: 1 (Budgeted Time 1 Min)

Which one of the following type of error occurs when a 0 is received instead of a stop bit (which is always a 1)?

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Answer (Please select your correct option)

Framing error



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Parity error

Over-run error

Under-run error

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Question No : 12 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.

Answer (Please select your correct option)

Partial decoding



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Full encoding

Partial multiplexing

Half encoding

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Question No : 13 of 52

Marks: 1 (Budgeted Time 1 Min)

Consider Falcon A, with 16 address lines, the total address space is _____ Kbytes.

Answer (Please select your correct option)

2^{16}



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2^{10}

2^6

2^8

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Question No : 14 of 52

Marks: 1 (Budgeted Time 1 Min)

CPU can exchange data with a peripheral device using _____ technique.

Answer (Please select your correct option)

Memory Contention

Direct Memory Access

Pre-fetching

Pipelining



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Question No : 15 of 52

Marks: 1 (Budgeted Time 1 Min)

Which one of the following is NOT a technique used when the CPU wants to exchange data with peripheral device?

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Answer (Please select your correct option)

Direct Memory Access

Interrupt driven I/O

Programmed I/O

Virtual Memory



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Question No : 16 of 52

Marks: 1 (Budgeted Time 1 Min)

Which one is the last instruction of the ISR that is to be executed when the ISR terminates?

Answer (Please select your correct option)

- IRET  correct answer solved by hadi
- IRQ
- INT
- NMI

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----- is the time needed by the CPU to recognize (not service) an interrupt request.

Answer (Please select your correct option)

Interrupt Latency



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Response Deadline

Timer delay

Throughput

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Question No : 18 of 52

Marks: 1 (Budgeted Time 1 Min)

In Multiple Interrupt Lines approach, a number of interrupt lines are provided between the _____ modules.

Answer (Please select your correct option)

External and Internal

CPU and I/O

CPU and Memory

Memory and I/O

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In FALCON-A assembler and simulator (FALSTM), variables are defined by using the _____ directive.

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Answer (Please select your correct option)

.bin

.equ

.iret

.end

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Question No : 20 of 52

Marks: 1 (Budgeted Time 1 Min)

In Direct memory access (DMA), a _____ is needed to control the total activity and to synchronize the transfer of data.

Answer (Please select your correct option)

DMA memory unit

DMA controller

Control software

Programmed I/O



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Question No : 21 of 52

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_____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

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Answer (Please select your correct option)

Programmed I/O

Interrupt driven I/O

Direct memory access

Polling

correct answer
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A component connected to the system bus and having control of it during a particular bus cycle is called _____.

Answer (Please select your correct option)

Address decoder

BIOS

Master component

Slave component

correct answer
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Question No : 23 of 52

Marks: 1 (Budgeted Time 1 Min)

A Hard Disk sector has the _____ parts.

Answer (Please select your correct option)

- Header only
- Data section and a trailer
- Data section only
- Header, data section and a trailer



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Question No : 24 of 52

Marks: 1 (Budgeted Time 1 Min)

CRC has _____ overhead as compared to Hamming code.

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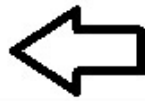
Answer (Please select your correct option)

Equal

Greater

Lesser

Absolutely no



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Question No : 25 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ are computed by the ALU and stored in processor status register.

Answer (Please select your correct option)

Condition Codes



Control Signals

Flip Flops

Multiplexers

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_____ occurs when the exponent is too large and can not be represented in the exponent field.

Answer (Please select your correct option)

- Underflow
- Overflow
- Rounding Off
- Normalization



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Question No : 27 of 52

Marks: 1 (Budgeted Time 1 Min)

In Single-Precision Binary Floating Point Representation the size of exponent is _____.

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Answer (Please select your correct option)

8-bits



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11-bits

1-bits

23-bits

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The _____ is m-bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus.

Answer (Please select your correct option)

Memory address register (MAR)



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Program counter register

Accumulator register

Instruction register

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_____ is a place for safe storage and provides the fastest possible storage after the registers.

Answer (Please select your correct option)

Hard Disk

Cache

Compact Disk

Floppy Disk

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Question No : 30 of 52

Marks: 1 (Budgeted Time 1 Min)

For a request for data, if the data is available in the cache it results in a _____.

Answer (Please select your correct option)

Cache Miss

Spatial Locality

Temporal Locality

Cache Hit



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Question No : 31 of 52

Marks: 1 (Budgeted Time 1 Min)

For write to complete in Write through, the CPU has to wait. This wait state is called _____.

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Answer (Please select your correct option)

Write Through

Write Back

Write Allocate

Write Stall



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Question No : 32 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ contains permanent pattern of data that cannot be changed.

Answer (Please select your correct option)

RAM

Hard Disk

Cache

ROM



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Question No : 33 of 52

Marks: 1 (Budgeted Time 1 Min)

In Control Field of page table, _____ indicate the availability of page in main memory.

Answer (Please select your correct option)

Access Control Bits

Used Bits

Presence Bits

Redundant Bits



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Question No : 34 of 52

Marks: 1 (Budgeted Time 1 Min)

In _____ technique memory is divided into segments of variable sizes depending upon the requirements.

Answer (Please select your correct option)

Multiplexing

Segmentation

Hamming code

Partial decoding

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Question No : 35 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ depends upon the average number of calls and the service time taken by a particular server.

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Answer (Please select your correct option)

Throughput



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Latency

Poisson Distribution

Response Time

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Question No : 36 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is also called traffic intensity and its value must be between 0 and 1.

Answer (Please select your correct option)

Little's Law

Poisson Distribution

Server Utilization

SPEC



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Question No : 37 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is the maximum rate at which data can be transmitted through networks.

Answer (Please select your correct option)

Transmission Time

Latency

Transport Latency

Bandwidth



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Question No : 38 of 52

Marks: 1 (Budgeted Time 1 Min)

The time for the message to pass through the network, except the time of flight is called _____.

Answer (Please select your correct option)

Transmission Time



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Latency

Transport Latency

Bandwidth

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_____ refers to the interconnection of machines in a building or a campus.

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Answer (Please select your correct option)

SAN

LAN

WAN

MAN

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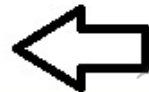
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SPARC (Scalable Processor Architecture) is an example of _____ architecture.

Answer (Please select your correct option)

- CISC
- RISC
- SRC
- FALCON



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What is distributed computing?

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Answer (Please [click here to Add Answer](#))



In distributed computing, all elements which are interconnected operate under one operating system. To a user, it appears as a virtual uni-processor system.

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Write any two differences between EAGLE and Modified EAGLE.

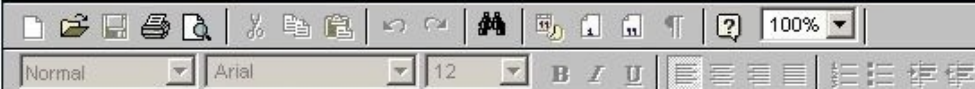
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Answer (Please [click here to Add Answer](#))

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The modified EAGLE is an improved version of the processor EAGLE. there were several limitations in EAGLE, and these have been remedied in the modified EAGLE processor.

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Differentiate between selector channel and multiplexer channel.

Answer (Please [click here to Add Answer](#))

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Normal Arial 12 B I U

Selector Channel It is the DMA controller that can do block transfers for several devices but only one at a time.

Multiplexer Channel It is the DMA controller that can do block transfers for several devices at once.

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Differentiate between PROM and EPROM.

Answer (Please [click here to Add Answer](#))

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PROM The PROM stands for Programmable Read only Memory. It is also nonvolatile and may be written into only once. For PROM, the writing process is performed electrically in the field. PROMs provide flexibility and convenience.

EPROM Erasable Programmable Read-only Memory or EPROM chips have quartz windows and by applying ultraviolet light erase the data can be erased from the EPROM. Data can be restored in an EPROM after erasure. EPROMs are more expensive than PROMs and are generally used for prototyping or small-quantity, special purpose work.

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How can you define an instruction set? Name the essential elements of computer instructions.

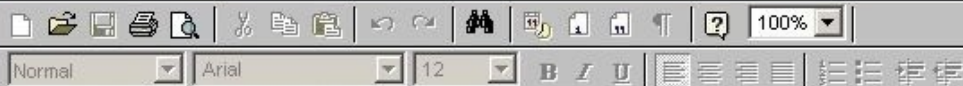
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Answer (Please [click here to Add Answer](#))

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INSTRUCTION SET An instruction set is a collection of all possible machine language commands that are understood and can be executed by a processor.

ESSENTIAL ELEMENTS OF COMPUTER INSTRUCTIONS: There are four essential elements of an instruction; the type of operation to be performed, the place to find the source operand(s), the place to store the result(s) and the source of the next instruction to be executed by the processor.

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What is the relationship between hard disk Platters, Tracks and Sectors?

Answer (Please [click here to Add Answer](#))

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A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address. So, before the actual data, there is a header and this header consisting of few bytes like 10 bytes. Along with header there is a trailer. Every sector has three parts: a header, data section and a trailer.

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Question No : 47 of 52

Marks: 3 (Budgeted Time 6 Min)

Find out the Sign, Significant and Exponent from the following floating point number.

$$-0.7 \times 10^{-4}$$

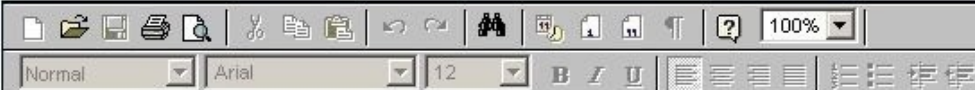
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Answer (Please [click here](#) to Add Answer)

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Sign = 0

Significant= 0.7

Exponent= -4

Base = 10= fixed for given type of representation

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What is the use of translation lookaside buffer (TLB) and how it is implemented inside the CPU?

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Answer (Please [click here to Add Answer](#))

Normal Arial 12 B I U

To speed up the process of virtual address translation, translation Lookaside buffer (TLB) is implemented as a small cache inside the CPU, which stores the most recent page table entry reference made in the MMU.

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Write the Structural RTL description for "un-conditional jump" instruction i.e. **jump [ra+c2]**.

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Answer (Please [click here to Add Answer](#))



Step	RTL
T0-T2	Instruction Fetch
T3	$(ra=0): A \leftarrow PC, (ra \neq 0): A \leftarrow R[ra];$
T4	$C \leftarrow A + c2(\text{sign extend});$
T5	$PC \leftarrow C;$

Step	RTL
T0-T2	Instruction fetch
T3	$n<4..0> \leftarrow IR<4..0>;$
T4	$C \leftarrow (N \& 0) \oplus R[rb]<15..N>;$
T5	$R[ra] \leftarrow C;$

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A hard disk with 10 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector. What is the total capacity of the disk?

Answer (Please [click here to Add Answer](#))

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512 bytes x 512

sectors=0.2MB/track

0.2MB x 1024 tracks =0.2GB/platter

Therefore the hard disk has the total capacity of $10 \times 0.2=2\text{GB}$

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Question No : 51 of 52

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Show all the steps involved in integer division algorithm to divide 45_{10} by 5_{10} .

Answer (Please click here to Add Answer)

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D 000000 101101 , d= 000101

D=000001 011010
d=000101

Dif(-) q=0

D=000010 110100
d=000101

Dif(-) q=00

D=000101 101000
d=000101

Dif(+) q=001

D=000001 010000
d=000101

Dif(-) q=0010

D=000010 100000
d=000101

Dif(-) q=00100

D=000101 000000
d=000101

Dif(+) q=001001



Start Time: 7:37 PM
116:00
Time Left

Hence remainder = $(000000)_{12} = 0$
Quotient = $(001001)_{12} = 9_{10}$

ANSWER

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Suppose an I/O system with a single disk gets (on average) 100 I/O requests/second and the average time for a disk to service an I/O request is 6ms. What is the utilization of the I/O system?

Answer (Please [click here to Add Answer](#))

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Time for an I/O request = 6ms
=0.006sec

Server utilization = 100×0.006
= 0.6 sec

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