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Past Papers by Waqar Siddhu
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What does the instruction "ldr R3, 58" of SRC do?

Answer (Please select your correct option)

VuAnswers.com

it will load the register R3 with the contents of the memory location M [PC+58]

correct

It will load the register R3 with the relative address itself (PC+58).

It will store the register R3 contents to the memory location M [PC+58]

No operation

Made by: Waqar Siddhu

What functionality is performed by the instruction "lar R3, 36" of SRC?

Answer (Please select your correct option)

VuAnswers.com

it will load the register R3 with the contents of the memory location M [PC+36]

It will load the register R3 with the relative address itself (PC+36).

correct

It will store the register R3 contents to the memory location M [PC+36]

No operation

Made by: Waqar Siddhu

What is the instruction length of the SRC processor?

Answer (Please select your correct option)

VuAnswers.com

8 bits

16 bits

32 bits

correct

64 bits

Made by: Waqar Siddhu

What does the word 'D' in the 'D-flip-Flop' stands for?

Answer (Please select your correct option)

VuAnswers.com

- Data
- Digital
- Dynamic
- Double

correct

Made by: Waqar Siddhu

Almost every commercial computer has its own particular ----- language

Answer (Please select your correct option)

VuAnswers.com

assembly language

correct

English language

Higher level language

3GL

Made by: Waqar Siddhu

Which field of the machine language instruction is the "**type of operation**" that is to be performed?

Answer (Please select your correct option)

VuAnswers.com

Op-code (or the operation code)

correct

CPU registers

Memory cells

I/O locations

Made by: Waqar Siddhu

_____ is/are defined as the time required processing a single instruction.

Answer (Please select your correct option)

VuAnswers.com

Latency and Throughput

Latency

correct

Throughput

Hazards

Made by: Waqar Siddhu

In pipelining ----- is increased by overlapping the instruction execution

Answer (Please select your correct option)

VuAnswers.com

Latency

Throughput

Execution time

Clock speed

correct

Made by: Waqar Siddhu

Which of the following register(s) takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system?

Answer (Please select your correct option)

VuAnswers.com

Instruction Register

Memory address register

correct

Memory Buffer Register

Registers A and C

Made by: Waqar Siddhu

In which one of the following addressing modes, data is the part of the instruction itself, and so there is no need of address calculation?

Answer (Please select your correct option)

VuAnswers.com

Direct Addressing Mode

correct

Immediate addressing mode

Indirect Addressing Mode

Register (Direct) Addressing Mode

Made by: Waqar Siddhu

Which one of the following type of error occurs when a 0 is received instead of a stop bit (which is always a 1)?

Answer (Please select your correct option)

VuAnswers.com

Framing error

correct

Parity error

Over-run error

Under-run error

Made by: Waqar Siddhu

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.

Answer (Please select your correct option)

VuAnswers.com

Partial decoding

correct

Full encoding

Partial multiplexing

Half encoding

Made by: Waqar Siddhu

Consider Falcon A, with 16 address lines, the total address space is _____ Kbytes.

Answer (Please select your correct option)

VuAnswers.com

2^{16}

correct

2^{10}

2^6

2^8

Made by: Waqar Siddhu

CPU can exchange data with a peripheral device using _____ technique.

Answer (Please select your correct option)

VuAnswers.com

Memory Contention

Direct Memory Access

correct

Pre-fetching

Pipelining

Made by: Waqar Siddhu

Which one of the following is **NOT** a technique used when the CPU wants to exchange data with peripheral device?

Answer (Please select your correct option)

VuAnswers.com

Direct Memory Access

Interrupt driven I/O

Programmed I/O

Virtual Memory

correct

Made by: Waqar Siddhu

Which one is the last instruction of the ISR that is to be executed when the ISR terminates?

Answer (Please select your correct option)

VuAnswers.com

IRET

correct

IRQ

INT

NMI

Made by: Waqar Siddhu

----- is the time needed by the CPU to recognize (not service) an interrupt request.

Answer (Please select your correct option)

VuAnswers.com

Interrupt Latency

correct

Response Deadline

Timer delay

Throughput

Made by: Waqar Siddhu

In Multiple Interrupt Lines approach, a number of interrupt lines are provided between the _____ modules.

Answer (Please select your correct option)

VuAnswers.com

External and Internal

CPU and I/O

correct

CPU and Memory

Memory and I/O

Made by: Waqar Siddhu

In FALCON-A assembler and simulator (FALSIM), variables are defined by using the _____ directive.

Answer (Please select your correct option)

VuAnswers.com

.bin

.equ

correct

.iret

.end

Made by: Waqar Siddhu

In Direct memory access (DMA), a _____ is needed to control the total activity and to synchronize the transfer of data.

Answer (Please select your correct option)

VuAnswers.com

DMA memory unit

DMA controller

correct

Control software

Programmed I/O

Made by: Waqar Siddhu

_____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

Answer (Please select your correct option)

VuAnswers.com

Programmed I/O

Interrupt driven I/O

Direct memory access

correct

Polling

Made by: Waqar Siddhu

A component connected to the system bus and having control of it during a particular bus cycle is called _____.

Answer (Please select your correct option)

VuAnswers.com

Address decoder

BIOS

Master component

correct

Slave component

Made by: Waqar Siddhu

A Hard Disk sector has the _____ parts.

Answer (Please select your correct option)

VuAnswers.com

- Header only
- Data section and a trailer
- Data section only
- Header, data section and a trailer

correct

Made by: Waqar Siddhu

CRC has _____ overhead as compared to Hamming code.

Answer (Please select your correct option)

VuAnswers.com

Equal

Greater

Lesser

Absolutely no

correct

Made by: Waqar Siddhu

_____ are computed by the ALU and stored in processor status register.

Answer (Please select your correct option)

VuAnswers.com

Condition Codes

correct

Control Signals

Flip Flops

Multiplexers

Made by: Waqar Siddhu

_____ occurs when the exponent is too large and can not be represented in the exponent field.

Answer (Please select your correct option)

VuAnswers.com

Underflow

Overflow

correct

Rounding Off

Normalization

Made by: Waqar Siddhu

In Single-Precision Binary Floating Point Representation the size of exponent is _____.

Answer (Please select your correct option)

VuAnswers.com

8-bits

correct

11-bits

1-bits

23-bits

Made by: Waqar Siddhu

The _____ is m-bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus.

Answer (Please select your correct option)

VuAnswers.com

Memory address register (MAR)

correct

Program counter register

Accumulator register

Instruction register

Made by: Waqar Siddhu

_____ is a place for safe storage and provides the fastest possible storage after the registers.

Answer (Please select your correct option)

VuAnswers.com

Hard Disk

Cache

correct

Compact Disk

Floppy Disk

Made by: Waqar Siddhu

For a request for data, if the data is available in the cache it results in a _____.

Answer (Please select your correct option)

VuAnswers.com

Cache Miss

Spatial Locality

Temporal Locality

Cache Hit

correct

Made by: Waqar Siddhu

For write to complete in Write through, the CPU has to wait. This wait state is called _____.

Answer (Please select your correct option)

VuAnswers.com

Write Through

Write Back

Write Allocate

Write Stall

correct

Made by: Waqar Siddhu

_____ contains permanent pattern of data that cannot be changed.

Answer (Please select your correct option)

VuAnswers.com

RAM

Hard Disk

Cache

ROM

correct

Made by: Waqar Siddhu

In Control Field of page table, _____ indicate the availability of page in main memory.

Answer (Please select your correct option)

VuAnswers.com

Access Control Bits

Used Bits

Presence Bits

Redundant Bits

correct

Made by: Waqar Siddhu

In _____ technique memory is divided into segments of variable sizes depending upon the requirements.

Answer (Please select your correct option)

VuAnswers.com

Multiplexing

Segmentation

correct

Hamming code

Partial decoding

Made by: Waqar Siddhu

_____ depends upon the average number of calls and the service time taken by a particular server.

Answer (Please select your correct option)

VuAnswers.com

Throughput

correct

Latency

Poisson Distribution

Response Time

Made by: Waqar Siddhu

_____ is also called traffic intensity and its value must be between 0 and 1.

Answer (Please select your correct option)

VuAnswers.com

Little's Law

Poisson Distribution

Server Utilization

correct

SPEC

Made by: Waqar Siddhu

_____ is the maximum rate at which data can be transmitted through networks.

Answer (Please select your correct option)

VuAnswers.com

Transmission Time

Latency

Transport Latency

Bandwidth

correct

Made by: Waqar Siddhu

The time for the message to pass through the network, except the time of flight is called _____.

Answer (Please select your correct option)

VuAnswers.com

Transmission Time

correct

Latency

Transport Latency

Bandwidth

Made by: Waqar Siddhu

_____ refers to the interconnection of machines in a building or a campus.

Answer (Please select your correct option)

VuAnswers.com

SAN

LAN

WAN

MAN

correct

Made by: Waqar Siddhu

SPARC (Scalable Processor Architecture) is an example of _____ architecture.

Answer (Please select your correct option)

VuAnswers.com

CISC

RISC

correct

SRC

FALCON

Made by: Waqar Siddhu

Which one of the following is the memory organization of **EAGLE processor**?

VuAnswers.com

Answer (Please select your correct option)

$2^8 * 8$ bits

$2^{16} * 8$ bits

page 120

$2^{32} * 8$ bits

$2^{64} * 8$ bits

Made by: Waqar Siddhu

-----is a collection of binary digits or bits that the computer reads and interprets.

VuAnswers.com

Answer (Please select your correct option)

assembly language

higher level language

English language

machine language

In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?

Answer (Please select your correct option)

VuAnswers.com

Direct Addressing Mode

Immediate addressing mode

Indirect Addressing Mode

Register (Direct) Addressing Mode

Made by: Waqar Siddhu

The external interface of FALCON-A consists of a _____ address bus and a _____ data bus.

Answer (Please select your correct option)

VuAnswers.com

8-bit , 8-bit

16-bit , 16-bit

176

16-bit , 24-bit

16-bit , 32-bit

Made by: Waqar Siddhu

Execution time of a program with respect to the processor is calculated as:

VuAnswers.com

Answer (Please select your correct option)

Execution Time = $IC \times CPI \times MIPS$

Execution Time = $IC \times CPI \times T$

ans

Execution Time = $CPI \times T \times MFLOPS$

Execution Time = $IC \times T$

Made by: Waqar Siddhu

In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?

Answer (Please select your correct option)

VuAnswers.com

Arithmetic

Load/store

ans

Control

Logic

Made by: Waqar Siddhu

The _____ instruction is completed once memory access has been made and the memory location has been written to.

Answer (Please select your correct option)

VuAnswers.com

Store

p 208

Branch

Load

Control

Made by: Waqar Siddhu

Which type of instructions enables mathematical computations?

VuAnswers.com

Answer (Please select your correct option)

Arithmetic

page 92

Control

Data transfer

Miscellaneous

Made by: Waqar Siddhu

_____ control signal allows the bus to read from the selected register.

VuAnswers.com

Answer (Please select your correct option)

RBE

RCE

LCON

R2BUS

For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

Answer (Please select your correct option)

VuAnswers.com

Registers

Control signals

p 171 ans

Memory

DMA controllers

Made by: Waqar Siddhu

Every I/O port has a unique identifier associated with it, which is called its -----

VuAnswers.com

Answer (Please select your correct option)

Address

ans

Access point

Interval Identifier

Device driver

Made by: Waqar Siddhu

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.

Answer (Please select your correct option)

VuAnswers.com

Partial decoding

ans

Full encoding

Partial multiplexing

Half encoding

Made by: Waqar Siddhu

Partial decoding is an attractive choice in _____.

VuAnswers.com

Answer (Please select your correct option)

Small systems

ans

Large systems

Medium systems

All of the above

Made by: Waqar Siddhu

Consider Falcon A, with 16 address lines, the total address space is _____ Kbytes.

VuAnswers.com

Answer (Please select your correct option)

2^{16}

ans

2^{10}

2^6

2^8

Made by: Waqar Siddhu

In which one of the following methods, does the CPU poll to identify the interrupting module and branch to an interrupt service routine on detecting an interrupt?

Answer (Please select your correct option)

VuAnswers.com

Multiple interrupt lines

Software Poll

ans

Daisy Chain

Parallel Priority

Made by: Waqar Siddhu

Maskable Interrupts are applied to the _____ pin of the processor.

VuAnswers.com

Answer (Please select your correct option)

INTR

ans

NMI

IRET

INT

Made by: Waqar Siddhu

Non-maskable Interrupts are detected using the _____ pin of the processor.

VuAnswers.com

Answer (Please select your correct option)

INTR

NMI

ans

IRET

INT

Made by: Waqar Siddhu

In Multiple Interrupt Lines approach, a number of interrupt lines are provided between the _____ modules.

Answer (Please select your correct option)

VuAnswers.com

External and Internal

CPU and I/O

ans

CPU and Memory

Memory and I/O

Made by: Waqar Siddhu

In FALCON-A assembler and simulator (FALSIM), variables are defined by using the _____ directive.

Answer (Please select your correct option)

VuAnswers.com

.bin

.equ

.iret

.end

Made by: Waqar Siddhu

_____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

Answer (Please select your correct option)

VuAnswers.com

Programmed I/O

Interrupt driven I/O

Direct memory access

ans

Polling

Made by: Waqar Siddhu

Taking control of the system bus for a few bus cycles is known as _____.

VuAnswers.com

Answer (Please select your correct option)

Bus Scheduling

Cycle Stealing

ans

Cycle Transferring

CPU Scheduling

Made by: Waqar Siddhu

A component connected to the system bus and having control of it during a particular bus cycle is called _____.

VuAnswers.com

Answer (Please select your correct option)

Address decoder

BIOS

Master component

ans

Slave component

Made by: Waqar Siddhu

When it is required to read data from a particular location of the disk, the head moves towards the selected track and this process is called_____.

Answer (Please select your correct option)

VuAnswers.com

Fragmentation

Defragmentation

Seek

ans

Encoding

Made by: Waqar Siddhu

CRC has _____ overhead as compared to Hamming code.

VuAnswers.com

Answer (Please select your correct option)

Equal

Greater

Lesser

ans

Absolutely no

Made by: Waqar Siddhu

The conversion of numbers from a representation in one base to another is known as _____

VuAnswers.com

Answer (Please select your correct option)

Radix Conversion

ans

Number Representation

Decimal Representation

Hexadecimal Representation

Made by: Waqar Siddhu

In _____, bits are encoded in pairs so there are only ' $n/2$ ' additions instead of ' n '.

Answer (Please select your correct option)

VuAnswers.com

Booth Recoding

Bit-Pair Recoding

ans

Fraction Division

Integer Division

Made by: Waqar Siddhu

_____ are computed by the ALU and stored in processor status register.

VuAnswers.com

Answer (Please select your correct option)

Condition Codes

ans

Control Signals

Flip Flops

Multiplexers

Made by: Waqar Siddhu

In computers, floating-point representation uses _____ to encode significand, exponent and their sign in a single word.

Answer (Please select your correct option)

VuAnswers.com

Decimal Numbers

Binary Numbers

ans

Octal Numbers

Hexadecimal Numbers

Made by: Waqar Siddhu

In floating point representations _____ is also called mantissa.

VuAnswers.com

Answer (Please select your correct option)

Sign



Base



Significant



ans p 347

Exponent



Made by: Waqar Siddhu

In Single-Precision Binary Floating Point Representation the size of exponent is _____.

VuAnswers.com

Answer (Please select your correct option)

8-bits



ans

11-bits



1-bits



23-bits



Made by: Waqar Siddhu

_____ is nonvolatile i.e. it retains the information in it when power is removed from it.

VuAnswers.com

Answer (Please select your correct option)

RAM

DRAM

ROM

ans

SRAM

Made by: Waqar Siddhu

Based on the statistical results, the cache block which has been least used in the recent past, is replaced with a new block. This technique is called _____.

Answer (Please select your correct option)

VuAnswers.com

Always Replacement

Random Replacement

LFU (Least Frequently Used)
ans

Write Allocate

Made by: Waqar Siddhu

_____ acts as a cache between main memory and secondary memory.

VuAnswers.com

Answer (Please select your correct option)

Read Only Memory

Flash Memory

Virtual Memory

ans

Magnetic Tape

Made by: Waqar Siddhu

Randomly replacing any older page to bring in the desired page is known as _____.

VuAnswers.com

Answer (Please select your correct option)

Always Replacement

LFU (Least Frequently Used)

Random Replacement

ans

Fragmentation

Made by: Waqar Siddhu

_____ are formed by concatenating the page number with the word number.

VuAnswers.com

Answer (Please select your correct option)

Memory chips

Protocols

Hazards

Virtual addresses

ans

Made by: Waqar Siddhu

In _____ technique memory is divided into segments of variable sizes depending upon the requirements.

VuAnswers.com

Answer (Please select your correct option)

Multiplexing

Segmentation

ans

Hamming code

Partial decoding

Made by: Waqar Siddhu

_____ depends upon the average number of calls and the service time taken by a particular server.

VuAnswers.com

Answer (Please select your correct option)

Throughput
ans

Latency

Poisson Distribution

Response Time

Made by: Waqar Siddhu

_____ is also called traffic intensity and its value must be between 0 and 1.

VuAnswers.com

Answer (Please select your correct option)

Little's Law

Poisson Distribution

Server Utilization

ans

SPEC

Made by: Waqar Siddhu

The time for the message to pass through the network, except the time of flight is called _____.

Answer (Please select your correct option)

VuAnswers.com

Transmission Time

ans

Latency

Transport Latency

Bandwidth

Made by: Waqar Siddhu

A set of rules followed by different components in a network is called _____.

VuAnswers.com

Answer (Please select your correct option)

Host



Connectivity



Resource Sharing



Protocol



ans

Made by: Waqar Siddhu

What is the size of the memory space that is available to **SRC processor**?

Answer (Please select your correct option)

VuAnswers.com

2⁸ bytes

2¹⁶ bytes

2³² bytes

correct

2⁶⁴ bytes

Made by: Waqar Siddhu

Which one of the following is the memory organization of **SRC processor**?

Answer (Please select your correct option)

VuAnswers.com

$2^8 * 8$ bits

$2^{16} * 8$ bits

$2^{32} * 8$ bits

correct

$2^{64} * 8$ bits

Made by: Waqar Siddhu

In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?

Answer (Please select your correct option)

VuAnswers.com

Direct Addressing Mode

correct

Immediate addressing mode

Indirect Addressing Mode

Register (Direct) Addressing Mode

Made by: Waqar Siddhu

Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?

Answer (Please select your correct option)

VuAnswers.com

:=

correct

&

%

©

Made by: Waqar Siddhu

Which one of the following register holds the address of the next instruction to be executed?

Answer (Please select your correct option)

VuAnswers.com

Accumulator

Address Mask

Instruction Register

Program Counter

correct

Made by: Waqar Siddhu

Which one of the following register holds the instruction that is being executed?

Answer (Please select your correct option)

VuAnswers.com

Accumulator

Address Mask

Instruction Register

correct

Program Counter

Made by: Waqar Siddhu

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

Answer (Please select your correct option)

VuAnswers.com

Processor-Memory-Switch level (PMS level)

correct

Instruction Set Level

Register Transfer Level

Logic design level

Made by: Waqar Siddhu

Which one of the following design levels is called the gate level?

Answer (Please select your correct option)

VuAnswers.com

Logic Design Level

correct

Circuit Level

Mask Level

Register transfer Level

Made by: Waqar Siddhu

_____ Instructions usually involve calculating the target address and evaluating a condition.

Answer (Please select your correct option)

VuAnswers.com

Add

Branch

correct

Load

Store

Made by: Waqar Siddhu

Which one of the following instructions is used to load register from memory using a relative address?

Answer (Please select your correct option)

VuAnswers.com

la

nop

ldr

correct

str

Made by: Waqar Siddhu

An interface that is used to connect the computer bus with I/O devices is called _____.

Answer (Please select your correct option)

VuAnswers.com

Buffer

I/O port

Memory mapping

Processor

correct

Made by: Waqar Siddhu

Every I/O port has a unique identifier associated with it, which is called its -----

Answer (Please select your correct option)

VuAnswers.com

Address

correct

Access point

Interval Identifier

Device driver

Made by: Waqar Siddhu

_____ refers to the situation in which all I/O operations are performed under the direct control of a program running on the CPU.

Answer (Please select your correct option)

VuAnswers.com

Direct memory access

Virtual memory

Partial decoding

Programmed I/O

correct

Made by: Waqar Siddhu

_____ is the process of periodically checking the status of a device to see if it is ready for the next I/O operation.

Answer (Please select your correct option)

VuAnswers.com

Polling

correct

Snooping

Data Bus Multiplexing

Pipelining

Made by: Waqar Siddhu

Which one of the following is **NOT** a technique used when the CPU wants to exchange data with peripheral device?

Answer (Please select your correct option)

VuAnswers.com

Direct Memory Access

Interrupt driven I/O

Programmed I/O

Virtual Memory

correct

Made by: Waqar Siddhu

Which one is the last instruction of the ISR that is to be executed when the ISR terminates?

Answer (Please select your correct option)

VuAnswers.com

IRET

correct

IRQ

INT

NMI

Made by: Waqar Siddhu

----- is the time needed by the CPU to recognize (not service) an interrupt request.

Answer (Please select your correct option)

VuAnswers.com

Interrupt Latency

correct

Response Deadline

Timer delay

Throughput

Made by: Waqar Siddhu

In Multiple Interrupt Lines approach, a number of interrupt lines are provided between the _____ modules.

Answer (Please select your correct option)

VuAnswers.com

External and Internal

CPU and I/O

correct

CPU and Memory

Memory and I/O

Made by: Waqar Siddhu

Falcon-A Simulator loads a FALCON-A binary file with a _____ extension and presents its contents into different areas of the simulator.

Answer (Please select your correct option)

VuAnswers.com

.bin

.binfa

correct

.fa

.asmfa

Made by: Waqar Siddhu

In Direct memory access (DMA), a _____ is needed to control the total activity and to synchronize the transfer of data.

Answer (Please select your correct option)

VuAnswers.com

DMA memory unit

DMA controller

correct

Control software

Programmed I/O

Made by: Waqar Siddhu

_____ allows a peripheral device to read from and/or write to memory without intervention by the CPU.

Answer (Please select your correct option)

VuAnswers.com

Programmed I/O

Interrupt driven I/O

Direct memory access

correct

Polling

Made by: Waqar Siddhu

Taking control of the system bus for a few bus cycles is known as _____.

Answer (Please select your correct option)

VuAnswers.com

Bus Scheduling

Cycle Stealing

correct

Cycle Transferring

CPU Scheduling

Made by: Waqar Siddhu

A component connected to the system bus and having control of it during a particular bus cycle is called _____.

Answer (Please select your correct option)

VuAnswers.com

Address decoder

BIOS

Master component

correct

Slave component

Made by: Waqar Siddhu

CRC has _____ overhead as compared to Hamming code.

Answer (Please select your correct option)

VuAnswers.com

Equal

Greater

Lesser

Absolutely no

correct

Made by: Waqar Siddhu

We represent e^{\wedge} instead of e to show _____.

Answer (Please select your correct option)

VuAnswers.com

Sign Magnitude Form

Radix Complement Form

Diminished Radix Compliment Form

Biased Representation

correct

Made by: Waqar Siddhu

In floating point representations _____ is also called mantissa.

Answer (Please select your correct option)

VuAnswers.com

Sign

Base

Significant

correct

Exponent

Made by: Waqar Siddhu

_____ occurs when the exponent is too large and can not be represented in the exponent field.

Answer (Please select your correct option)

VuAnswers.com

Underflow

Overflow

correct

Rounding Off

Normalization

Made by: Waqar Siddhu

In Double-Precision Binary Floating Point Representation the size of fraction is _____.

Answer (Please select your correct option)

VuAnswers.com

23-bits

52-bits

correct

11-bits

1-bits

Made by: Waqar Siddhu

_____ is a combination of arithmetic, logic and shifter unit along with some multiplexers.

Answer (Please select your correct option)

VuAnswers.com

Computer Bus

CPU Register

Flip Flop

ALU

correct

Made by: Waqar Siddhu

_____ is a place for safe storage and provides the fastest possible storage after the registers.

Answer (Please select your correct option)

VuAnswers.com

Hard Disk

Cache

correct

Compact Disk

Floppy Disk

Made by: Waqar Siddhu

_____ is nonvolatile i.e. it retains the information in it when power is removed from it.

Answer (Please select your correct option)

VuAnswers.com

RAM

DRAM

ROM

correct

SRAM

Made by: Waqar Siddhu

Based on the statistical results, the cache block which has been least used in the recent past, is replaced with a new block. This technique is called _____.

Answer (Please select your correct option)

VuAnswers.com

Always Replacement

Random Replacement

LFU (Least Frequently Used)

correct

Write Allocate

Made by: Waqar Siddhu

_____ acts as a cache between main memory and secondary memory.

Answer (Please select your correct option)

VuAnswers.com

Read Only Memory

Flash Memory

Virtual Memory

correct

Magnetic Tape

Made by: Waqar Siddhu

In _____ technique memory is divided into segments of variable sizes depending upon the requirements.

Answer (Please select your correct option)

VuAnswers.com

Multiplexing

Segmentation

correct

Hamming code

Partial decoding

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_____ is the maximum rate at which data can be transmitted through networks.

Answer (Please select your correct option)

VuAnswers.com

Transmission Time

Latency

Transport Latency

Bandwidth

correct

Made by: Waqar Siddhu

In physical media of networks, for increased and better performance we use _____ which are usually made of glass.

Answer (Please select your correct option)

VuAnswers.com

Coaxial Cables

Twisted Pair Cables

Fiber Optic Cables

Shielded Twisted Pair Cables

correct

Made by: Waqar Siddhu

In _____ topology, all the computers are connected in the form of a circle.

Answer (Please select your correct option)

VuAnswers.com

Bus

Ring

Mesh

Star

correct

Made by: Waqar Siddhu

Connection Oriented Communication reserves the _____ until the transfer is completed.

Answer (Please select your correct option)

VuAnswers.com

Bandwidth

correct

Error

Checksum

Protocol

Made by: Waqar Siddhu

In connection-less communication message is divided into _____.

Answer (Please select your correct option)

VuAnswers.com

Tracks

Sectors

Platters

Packets

correct

Made by: Waqar Siddhu

SPARC (Scalable Processor Architecture) is an example of _____ architecture.

Answer (Please select your correct option)

VuAnswers.com

CISC

RISC

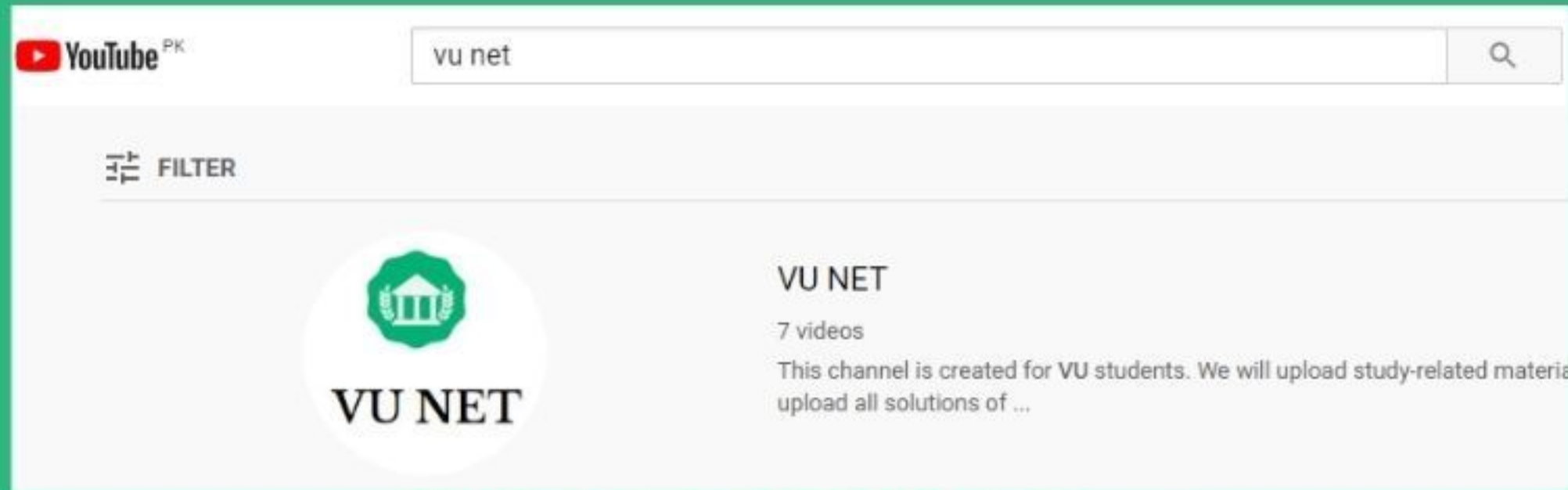
SRC

FALCON

correct

Made by: Waqar Siddhu

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