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CS501-Advance Computer
Architecture
FINAL TERM MCQS
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ALL answers are verified if found any mistake then Correct ACCORDINGLY

1. A software routine performed when an interrupt is received by the computer is called as_
 - a. **Interrupt**
 - b. Interrupt handler
 - c. Exception
 - d. Trap
2. Which of the following pins of the processor is designated for maskable interrupts?
 - a. NMI
 - b. MI
 - c. **INTR**
 - d. RINT
3. $ET = \text{---}$
 - a. $CP \times IC \times T$
 - b. **$CPI \times IC \times T$**
 - c. $CPI / IC \times T$
 - d. $CPI \times IC/T$
4. By which file extension does the FALCON-A assembler loads a FALCON-A-assembly file?
 - a. **.asmfa**
 - b. .org
 - c. .exe
 - d. .src
5. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
 - a. Daisy chain
 - b. **Software poll**
 - c. Multiple interrupt lines
 - d. All of given option_

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_____ signal has output direction with respect to printer.

O<7...0>

- b. STROBE#
- c. INT#
- d. **ACKNLG#**

6. _____ is said to occur when a 0 is received instead of a stop bit

- a. **Framing error**
- b. Parity error
- c. Block error
- d. Over-run error

7. A component connected to the system bus and having control of it during a particular bus cycle is called _____

- a. Slave component
- b. **Master component**
- c. System bus
- d. Buffer component

8. The information about the interrupt vector is given in 8-bit from 0 to 7, which is translated to bit _____ on the data bus

- a. **16 to 32**
- b. 11 to 18
- c. 0 to 7
- d. 8 to 15

9. An interface that can be used to connect the microcomputer bus to _____ is called as I/O port

- a. Flip flop
- b. Memory
- c. **Peripheral devices**
- d. Multiplexers

10. _____ allows a peripheral to read and write memory without intervention by the CPU

- a. Programmed I/O
- b. Interrupt driven I/O
- c. **Direct memory access(DMA)**
- d. Polling

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11. Every interrupt handler has an interrupt return (IRET) instruction, this instruction is an example of _____ return
- NEAR
 - FAR**
 - SHORT
 - RELATIVE
12. Which I/O technique will be used by a sound card that may need to access data stored in the computer's RAM?
- Programmed I/O
 - Interrupt driven I/O
 - Direct memory access(DMA)**
 - Polling
13. What should be the behavior of interrupt during critical section?
- Must remain disable**
 - Must remain enable
 - Depends on current situation
 - Only important interrupts be enable
14. Identify the type of serial communication error condition in which "0" is received instead of stop bit(which is always a "1")
- Framing error**
 - Parity error
 - Overrun error
 - Under run error
15. The Pentium does allow the use of some part of its ___ accumulator register EAX
- 8 bits
 - 16 bits
 - 32 bits**
 - 64 bits
16. ___ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer
- Computer bus**
 - Hazard
 - Memory
 - Disk

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17. Where does the processor store the address of the first instruction of the ISR?
- Interrupt vector**
 - Interrupt request
 - Interrupt handler
 - All of the given options
18. _____ is the time needed by the CPU to recognize (not service) an interrupt request.
- Interrupt latency**
 - Response deadline
 - Timer delay
 - Throughput
19. At the start of the transfer operation in synchronous communication, the master activates the _____ signal.
- Read**
 - Enable
 - Data
 - Acknowledge
20. Which is the last instruction of the ISR that is to be executed when the ISR terminates?
- IRET**
 - IRQ
 - INT
 - NMI
21. Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
- Daisy-Chaining Priority
 - Asynchronous Priority
 - Parallel Priority**
 - Semi-synchronous Priority
22. If a character is not available at the beginning of an interval, an _____ is said to occur.
- Under-run Error**
23. Tri-state buffers are used for removing _____.
- Instruction collision
 - bus collision
 - Instruction contention
 - bus contention**
24. When a particular sector is found, the data is transferred to _____.
- RAM

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- b. **I/O module**
- c. Cache memory
- d. Instruction register

25. Identify the following type of serial communication error condition:

“The prior character that was received was not still read by the CPU and is overwritten by a new received character.”

- a. Framing error
- b. Parity error
- c. **Overrun error**
- d. Under-run error

26. Taking control of the system bus for a few bus cycles is known as

_____.

- a. Bus Stealing
- b. **Cycle Stealing**
- c. Cycle Transferring
- d. None of given

27. The average latency to the desired data is halfway round the disk so, what will be the average rotation latency of the disk rotates at 20,000rpm.

- a. 1.25ms
- b. **1.5ms**
- c. 1.0ms
- d. 2.0ms

28. What is the status of the ACKNLG# signal when a character is completely received by the printer?

- a. It goes from low to high
- b. **. It goes from high to low page 239**
- c. It toggles its state
- d. It remains unaffected

29. Interrupt driven I/O is better than _____.

- a. **Polling**
- b. Data forwarding
- c. Stall
- d. First In First Out

31. Select the parts of a hard disk.

- a. Header only
- b. Data section and a trailer
- c. Data section only

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d. Header, data section and a trailer

32. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower- priority devices up to the device with the lowest priority, which is placed last in the series?
- a. Asynchronous
 - b. Daisy-Chaining Priority**
 - c. Parallel
 - d. Semi-synchronous
33. Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.
- a. Framing error
 - b. Parity error
 - c. Overrun error
 - d. Under-run error**
34. In the little-endian format exchanging data between computer, the data transmitted by one will be received in a “swapped” form by the other.
- a. Organized
 - b. Signals
 - c. Swapped**
 - d. Arranged
35. The source file of FALSIM should contain _____ text only.
- a. Unicode
 - b. ASCII**
 - c. ANSI
 - d. UTF
36. A component connected to the _____ and with which the master component can communicate during a particular bus cycle. Normally the CPU with its bus control logic is the master component.
- a. Slave component
 - b. System bus**
 - c. Master component
 - d. Bus component
37. In which technique does the hardware directly access host memory for reading or writing

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independent of CPU?

- a. **Direct Memory Access (DMA)**
- b. Programmed I/O
- c. Interrupt driven I/O
- d. Polling

38. Most parallel I/O ports used with peripheral devices are mapped on a range of _____.

- a. Bus addresses
- b. Direct memory access
- c. **Contiguous addresses**
- d. Cache

39. _____ signal is used in printer with DB-25 interface to reset its controller.

- a. #PE
- b. #STROB
- c. **#INIT**
- d. #SLCT

40. Why DMA is faster than Programmer I/O technique because?

- a. DMA transfers data directly using CPU
- b. **DMA transfers data directly without using CPU CONCEPTUAL**
- c. DMA uses buffers with CPU
- d. DMA uses interrupted driven I/O

41. _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored?

- Microprogramming
- b. Instruction pre-fetching
- c. Pipelining
- d. **Partial decoding**

42. In 8086/8088 processor, interrupt vector table is located at the memory location _____.

- a. **0**
- b. 4
- c. 256
- d. 1024

43. When an I/O module has a capability of executing a specific set of instructions for specific I/O devices in the memory without the involvement of CPU is called _____

- a. Selector Channel

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b. **I/O Channel**

c. I/O processors

d. Cycle Stealing

44. How does DMA save CPU time?

a. **By controlling transfer between I/O devices and memory directly**

b. By storing all data in a buffer to be later transferred to the CPU

c. By periodically polling

d. By issuing an interrupt request to the CPU to request attention

45. Connection to a CPU that provides a data path between the CPU and external

devices, such as a keyboard, display, or reader is called _____

a. Buffer

b. **I/O port**

c. Memory mapping

d. Processor

46. _____ lets the user execute the program, one instruction at a time.

a. **Single Step**

b. Execute

c. Change PC

d. List File

47. In _____ a separate address space of the CPU is reserved for I/O operations.

a. **Isolated I/O**

b. Memory Mapped I/O

c. All of above

d. None of above

48. Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?

a. Direct Memory Access (DMA)

b. Interrupt driven I/O

c. Programmed I/O

d. **Virtual Memory**

49. A computer interface is an _____ circuit that matches the requirements of the two subsystems between which it is connected.

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- b. **Electronic**
c. Primary
d. Obituary
50. _____ the device usually means reading its status register every so often until the device's status changes to indicate that has completed the request.
a. Interrupting
b. Masking
c. **Polling**
d. Executing
51. For input ports, the incoming data should be placed on the data bus only during the I/O read bus cycle. For this purpose, _____ are used.
a. Flip Flops
b. **Tri-state Buffers**
c. AND Gates
d. Registers
52. Which of the following is not true regarding serial communication?
a. Easy to implement
b. Inefficient
c. **High cost**
d. Slow
53. In a printer with DB-25 interface, _____ signal is better for edge triggered systems.
a. BUSY#
b. PE#
c. **ACKNLG#**
d. STROB#
54. The _____ can be determined from the number of platters and the number of tracks.
a. Speed of processing
b. Execution time
c. **Storage capacity**
d. Latency
55. The directive _____ is used to define variables.
a. **.equ**
b. .db

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d. .org

56. _____ means that the CPU should input data from an input device only when the device is ready to provide data and send data to an output device only when it is ready to receive data.

- a. Data location
- b. **Data synchronization**
- c. Data transfer
- d. Asynchronous transmission

57. The main issue/s in error control is/are _____.

- a. Detection of Error
- b. Correction of Error
- c. **Both Detection of Error and Correction of Error**
- d. Avoidance of Error

58. _____ signal has input direction with respect to printer

- a. BUSY
- b. **STROBE#**
- c. PE#
- d. ACKNLG#

59. A parallel port can be considered to be a big _____ gate.

- a. OR
- b. **AND**
- c. NOR
- d. NOR

60. Every time you press a key, an interrupt is generated.

This is an example of

- a. **Hardware interrupt**
- b. Software interrupt
- c. All of the given
- d. None of the given

61. How Interrupt driven I/O is better than polling because?

- a. Interrupt driver I/O is easy to design
- b. Interrupt driver I/O is enhanced version of polling
- c. **Interrupt driver I/O does not waste time on checking which device is available**
- d. Interrupt driven I/O is easy to program

62. How can you define an interrupt?

- a. A process where an external device can speed up the working of the microprocessor

b. A process where memory can speed up programs execution speed

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- c. **A process where an external device can get the attention of the microprocessor**
- d. A process where input devices can takeover the working of the microprocessor
63. _____ is/are example(s) of synchronous communication.
- a. **Register to Register**
- b. Register to Memory
- c. Memory to Memory
- d. All of the given
64. _____ depends upon the present position of the head and the position of the required sector.
- a. Direct memory Access
- b. Execution time
- c. Throughput
- d. **Seek time**
65. Which one of the following is the memory organization of SRC processor?
- $2^8 * 8$ bits
- $2^{16} * 8$ bits
- $2^{32} * 8$ bits (Page 46)**
- $2^{64} * 8$ bits
66. Type A format of SRC uses _____ instructions
- Two (Page 47)**
- three
- four
- five
67. The instruction ---- will **load** the register R3 with the contents of the memory location M [PC+56]
- Add R3, 56
- lar R3, 56
- ldr R3, 56 (Page 47)**
- str R3, 56
68. Which format of the instruction is called the accumulator?
- 3-address instructions
- 3-address instructions
- 2-address instructions
- 1-address instructions (Page 32)**
- 0-address instructions
69. Which one of the following are the **code size** and the **Number of memory bytes** respectively for a 2-address instruction?
- 4 bytes, 7 bytes

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7 bytes, 16 bytes (Page 36)

- 10 bytes, 19 bytes
- 13 bytes, 22 bytes

70. Which operator is used to name registers, or part of registers, in the Register Transfer Language?

- := (Page 66)**
- &
- %
- ©

71. The transmission of data in which each character is self-contained units with its own start and stop bits is -----

- Asynchronous**
- Synchronous
- Parallel
- All of the given options

72. Circuitry that is used to move data is called -----

- Bus**
- Port
- Disk
- Memory

73. Which one of the following is **NOT** a technique used when the CPU wants to exchange data with a peripheral device?

- Direct Memory Access (DMA).
- Interrupt driven I/O
- Programmed I/O

Virtual Memory (Page 268)

74. Every time you press a key, an interrupt is generated. This is an example of

- Hardware interrupt (Page 275)**
- Software interrupt
- Exception
- All of the given

75. The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are

- Maskable
- Non-maskable
- Non-vectored

Vectored (Page 277)

76. Which is the last instruction of the ISR that is to be executed when the ISR terminates?

- IRET (Page 278)**
- IRQ
- INT
- NMI

77. If NMI and INTR both interrupts occur simultaneously, then which one has the precedence over the other

- NMI (Page 279)**
- INTR

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- IRET
- All of the given

78. Identify the following type of serial communication error condition:

The prior character that was received was not still read by the CPU and is over written by a new received character.

- Framing error
- Parity error
- Overrun error (Page 240)**
- Under-run error

79. -----the device usually means reading its status register every so often until the device's status changes to indicate that it has completed the request.

- Executing
- Interrupting
- Masking
- Polling**

80. Which I/O technique will be used by a sound card that may need to access data stored in the computer's RAM?

- Programmed I/O
- Interrupt driven I/O
- Direct memory access(DMA)**
- Polling

81. For increased and better performance we use_ which are usually made of glass.

- Coaxial Cables
- Twisted Pair Cables
- Fiber Optic Cables (Page 390)**
- Shielded Twisted Pair Cables

82. In_ if we find some call party busy we can have provision of call waiting.

- Delay System (Page 381)**
- Loss System
- Single Server Model
- None of the given

83. In_ technique memory is divided into segments of variable sizes depending upon the requirements.

- Paging
- Segmentation (Page 365)**
- Fragmentation
- None of the given

84. For a request of data if the requested data is not present in the cache, it is called a ___

- Cache Miss (Page 358)**
- Spatial Locality
- Temporal Locality
- Cache Hit

85. An entire_ memory can be erased in one or a few seconds which is much faster than EPROM.

- PROM
- Cache

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EEPROM

Flash Memory (Page 356)

86. ___ chips have quartz windows and by applying ultraviolet light data can be erased from them.

PROM

Flash Memory

EPROM (Page 356)

EEPROM

87. The ___ signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.

REQUEST (Page 350)

COMPLETE

None of the given

88. ___ is a combination of arithmetic, logic and shifter unit along with some multiplexers and control unit.

Barrel Rotator

Control Unit

Flip Flop

ALU (Page 347)

89. In Multiple Interrupt Line, a number of interrupt lines are provided between the ___ modules

CPU and the I/O (Page 283)

CPU and Memory

Memory and I/O

None of the given

90. The data movement instructions ___ data within the machine and to or from input/output devices.

Store

Load

Move

None of given (Page 141)

91. CRC has----- overhead as compared to Hamming code.

Equal

Greater

Lesser (Page 329)

None of the given

92. The ___ is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide memory address register (MAR) .

Instruction Register(IR)

memory address register (MAR)

) memory Buffer Register(MBR) (Page 350)

Program counter (PC)

93. In ___ technique, a particular block of data from main memory can be placed in only one location into the cache memory .

Set Associative Mapping

Direct Mapping (Page 360)

Associative Mapping

Block Placement

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94. ___ indicate the availability of page in main memory.
- Access Control Bits
 - Used Bits
 - Presence Bits**
 - None of the given
95. The ___ RTN describes the overall effect of instructions on the programmer visible registers.
- ▶ **Abstract**
 - ▶ Concrete
 - ▶ Absolute
 - ▶ Basic
96. The instruction set is of ___ importance in governing the structure and function of the pipeline.
- ▶ Least
 - ▶ **Primary**
 - ▶ Secondary
 - ▶ No
97. ___ is the most general and least useful performance metrics for RISC machines.
- ▶ **MIPS**
 - ▶ Instruction Count
 - ▶ Number of registers
 - ▶ Clock Speed
98. A ___ provides four functions: Select, DataIn, DataOut and Read/Write.
- ▶ ALU
 - ▶ Bus
 - ▶ Register
 - ▶ **Memory Cell (Page 351)**
99. We can classify or partition the SRC instructions by their overall ___ behavior.
- ▶ **Register transfer**
 - ▶ Memory transfer
 - ▶ Execution
 - ▶ Logical
100. The ___ RTN describes detailed register transfer steps in the data path that produce the overall effect.
- ▶ Abstract
 - ▶ **Concrete**
 - ▶ Absolute
 - ▶ Basic

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▶ **32-bit**

▶ 16-bit

▶ 64-bit

▶ 8-bit

102. _____ Operations refers to a processor that can issue more than one instruction simultaneously.

▶ Macro

▶ Micro

▶ Scalar

▶ **Superscalar**

103. Exceptions which are _____ occur in response to events that are paced by the internal processor clock.

▶ Asynchronous

▶ **Synchronous**

▶ Internal

▶ External

104. In the hazard detection by hardware, resolved by pipeline stalls, if the instructions are in the adjoining stages, then the hazard must be detected in stage _____.

▶ 4

▶ 2

▶ **3**

▶ 1

105.

1-bit sign, 8-bit exponent, 23-bit fraction and a bias of 127 is used for _____ Binary Floating Point Representation

▶ Double precision

▶ **Single Precision (Page 348)**

▶ All of above

▶ Half Precision

106.

The average rotational latency if the disk rotated at 20,000rpm is _____

▶ 0.5 ms

▶ 3.5 ms

▶ 2.5 ms

▶ **1.5 ms (Page 324)**

107.

A hard disk with 5 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector. What is the total capacity of the disk?

▶ 1.5 GB

▶ **1 GB (Page 324)**

▶ 2 GB

▶ 3 GB

108.

Where does the processor store the address of the first instruction of the ISP?

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Interrupt vector (Page 277)

- Interrupt request
- Interrupt handler
- All of the given options

109. In ____, a separate address space of the CPU is reserved for I/O operations.

Isolated I/O (Page 236)

- Memory Mapped
- I/O All of above
- None of above

110. ----- is the time needed by the CPU to recognize (not service) an interrupt request.

Interrupt Latency (Page 279)

- Response
- Deadline Timer
- delay Throughput

111. How can you define an interrupt?

- A process where an external device can speedup the working of the microprocessor
- A process where memory can speed up programs execution speed
- A process where an external device can get the attention of the microprocessor
- A process where input devices can takeover the working of the microprocessor

112. A software routine performed when an interrupt is received by the computer is called as -----

- Interrupt
- Interrupt handler**
- Trap

113.

In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?

- Asynchronous
- Daisy-Chaining Priority**
- Parallel
- Semi-synchronous

114.

Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?

- Framing error (Page 240)**

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- Parity error
- Overrun error
- Under-run error

115. Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.

- Framing error
- Parity error
- Overrun error
- Under-run error**
(Page 240)

116.

A----- is a wiring scheme in which, for example, device A is wired to device B, device B is wired to device C, device C is wired to device D etc.

- Daisy chain**
- DMA
- Interrupt driven I/O
- Polling

117.

An ----- is the memory address of an interrupt handler.

- Interrupt vector**
- Interrupt service *
- routine Exception
- Mask

118.

The conversion of numbers from a representation in one base to another is known as ____

- Radix Conversion (Page 333)**
- Number Representation
- Decimal representation
- Hexadecimal Representation

119.

In which one of the following interrupts the device has to supply the address of the subroutine to

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the Microprocessor

- Maskable
- Non-maskable**
- Non-vectored
- Vectored

120.

----- interrupts are usually associated with the

- software hardware
- software**
- machine
- internal

121.

How Interrupt driven I/O is better than polling because?

- Interrupt driver I/O is easy to design
- Interrupt driver I/O is enhanced version of polling.
- **Interrupt driver I/O does not waste time on checking which device is available.** (Page 274)
- Interrupt driven I/O is easy to program.

122.

In Single-Precision Binary Floating Point Representation the exponent is __

- **8 bits (Page 348)**
- 11 bits
- 1 bit
- 23 bits

123.

The ____ is m-bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus Booth Recording

- **memory address register (MAR) (Page 350)**
- memory Buffer Register (MBR)
- Program counter (PC)
- Instruction Register (IR)

124.

A combination of parallel and sequential hardware used to build a multiplier is known as __

- Parallel Array
- Multiplier Booth Recording
- **Series Parallel Multiplier (Page 342)**
- None of the given

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125.

The register file is a collection of n -bit wide registers used for data transfer between memory and the CPU.

- 8
- 16
- 32 (Page 350)
- 64

126.

The _____ of an m digit number x is $x_c' = b^{m-1} - x$

- Radix Complement
- **Diminished Radix Complement (Page 337)**
- Signed Magnitude Form
- Biased Representation

127.

Shifting of the radix point towards left or right

- Shifting
- Logical
- Shift Right Shift
- **Scaling (Page 335)**

128.

In _____ adder circuit we feed carry out from the previous stage to the next stage and so on.

- **Ripple Carry Adder (Page 341)**
- Carry Look Ahead Adder
- Complement Adder
- 2's Complement Adder

129.

_____ are computed by the ALU and stored in processor status register.

- **Condition codes (Page 334)**
- Conditional Branches
- Fraction
- Division
- None of the

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given

130.

A _____ signal decides whether the input word should be shifted or bypassed.

- Control Read
- **Shift/bypass**
(Page 346)
- Control Write
- None of the given

131.

In _____ recording, bits are encoded in pairs so there are only 'n/2' additions instead of 'n'.

- Booth Recording
- **Bit Pair Recording** (Page 343)
- Integer division
- None of the given

132.

Given an m-digit base b number x, the _____ of x is $x_c = (b^m - x) \bmod b^m$

- **Radix Compliment**
(Page 337)
- Diminished Radix
- Compliment Signed
- Magnitude Form

Biased Representation

133.

For _____ of an error we just need to know that there exists an error.

- **Detection** (Page 328)
- Correction
- Both Correction and Detection
- None of the give

134.

In Double-Precision Binary Floating Representation the function is _____

- 23 bits
- **52 bits** (Page 348)

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- 1 bit

135.

_____ is the simplest form for representing a signed number

- Based representation
- Diminished Redex Complement Form
- **Sign Magnitude Form (Page 336)**
- None of the given

136.

In computers, floating-point representation uses ___ to encode significand, exponent and their sign in a single word

- Decimal Numbers
- **Binary Numbers (Page 347)**
- Octal Numbers
- Hexa decimal Numbers

137.

Which one of the following registers store a previously calculated value or a value loaded from the main memory?

- ▶ **Accumulator**
- ▶ Address Mask
- ▶ Instruction Register
- ▶ Program Counter

138.

Which one of the following portions of an instruction represents the operation to be performed?

- ▶ Address
- ▶ Instruction code
- ▶ **Opcode (Page 33)**
- ▶ Operand

139.

_____ control signal enable the input to the PC for receiving a value that is currently on the internal processor bus.

- ▶ **LPC (Page 172)**

- ▶ INC4
- ▶ LC
- ▶ Cout

140.

What is the instruction length of the FALCON-E processor?

- 8 bits
- 16 bits
- **32 bits (Page 134)**
- 64 bits

141.

Which type of instructions enables mathematical computations?

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▶ Arithmetic (Page 92)

- ▶ Control
- ▶ Data transfer
- ▶ None of the given

142.

What is the instruction length of the SRC and Falcon E processor?

- ▶ 8 bits
- ▶ 16 bits

▶ 32 bits (Page 134)

- ▶ 64 bits

143. An instruction that specifies one operand in memory and one operand in a register would be known as a _____ address instruction.

- ▶ 2-1/2

▶ 1-1/2 (Page 37)

- ▶ 0
- ▶ 2

144.

In floating point representations ___ is also called mantissa.

- ▶ Sign
- ▶ Base

▶ Significant (Page 347)

- ▶ Exponent

145. What should be the behavior of interrupts during critical sections?

▶ Must remain disable (Page 197)

- ▶ Must remain Enable
- ▶ Can be either enable or disable
- ▶ only important interrupts be enable

148. Which one of the following is a binary cell capable of storing one bit of information?

- ▶ Decoder

▶ Flip-flop (Page 76)

- ▶ Multiplexer
- ▶ Diplexer

149. Which type of instructions load data from memory into registers, or store data from register into memory and transfer data between different kinds of special-purpose registers?

- ▶ Arithmetic
- ▶ Control

▶ Data transfer (Page 88)

- ▶ Floating point

150.

What does the RTL expression [M(1234)] mean?

▶ The contents of memory whose address is 1234.

- ▶ The contents of data register 1234
- ▶ The effective address of register 1234
- ▶ The address of memory whose address is 1234.

151. Which one of the following languages presents a simple, human-oriented language to specify the operations, register communication and timing of the steps that take place within a CPU to carry out higher level (user programmable) instructions?

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- ▶ Assembly Language
- ▶ OOP(Object Oriented Language)
- ▶ **RTL (Register Transfer Language)**
- ▶ UML(Unified Modeling language)

152. Which one of the following instructions is used to load register from memory using a relative address?

- ▶ la
- ▶ lar

▶ **ldr (Page 145)**

- ▶ str

153.

Taking control of the system bus for a few bus cycles is known as _____.

- ▶ Bus Stealing

▶ **Cycle Stealing (Page 317)**

- ▶ Cycle Transferring
- ▶ None of given

154. In-----address mode, the actual data is stored in the instruction.

- ▶ Direct
- ▶ Indirect
- ▶ **Immediate**
- ▶ Relative

155. Keyboard Interrupt (INT 9) is an example of _____ interrupt.

▶ **Hardware**

- ▶ Software

156. A user program has to delete a file. The user program will be executing in the user mode. When it makes the specific system call to delete the file, an interrupt will be generated, this will cause the processor to halt its current activity and switch to supervisor mode. Once in supervisor mode, the operating system will delete the file and then control will return to the user program. This is an example of

- ▶ Hardware interrupt

▶ **Software interrupt (Page 275)**

- ▶ Exception
- ▶ All of the given

157. By which file extension does the FALCON-A Assembler loads a FALCON-A assembly file?

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- ▶ .org
- ▶ .exe
- ▶ .src

157.

All -----interrupts have priority over all interrupts

▶ **internal, external (Page 279)**

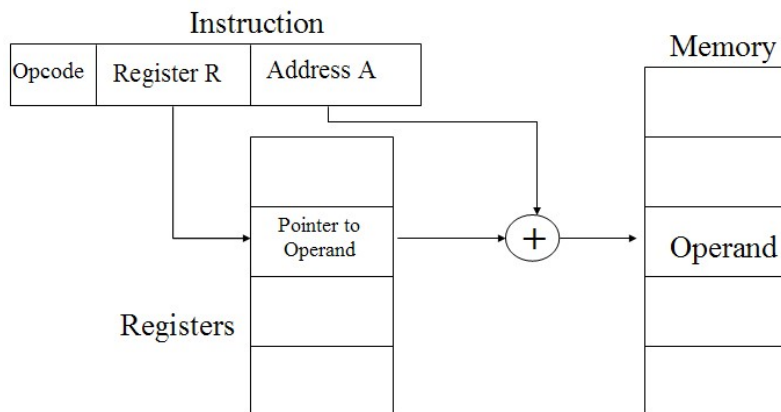
- ▶ external, internal

158. The can also be used anywhere in the source file to force code at a particular address in the memory.

- ▶ .end directive
- ▶ .start directive
- ▶ .label directive

▶ **.org directive (Page 298)**

Question No:106



In this figure, the constant value specified by the immediate field is added to the register value, and the resultant is the index of memory location that is referred i.e. Effective Address = A + (content of R) .

Identify the addressing mode.

▶ **Displacement(Page 139)**

- ▶ Immediate
- ▶ Indexed
- ▶ Relative

159. In which one of the following addressing modes, the operand does not specify an address but it is the actual data to be used.

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- ▶ Indirect
- ▶ **Immediate**
- ▶ Relative



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160. When is the "Divide error interrupt" generated?

- ▶ When an attempt is made to divide by decimal number
- ▶ When an attempt is made to multiply by zero
- ▶ **When an attempt is made to divide by zero (Page 197)**
- ▶ When negative number is stored in a register

161. Which one of the following is a term used to describe a storage systems' resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques?

- ▶ Interrupt handling
- ▶ Programmed I/O
- ▶ Polling
- ▶ **RAID [click here for detail](#)**

162. _____ is the time for first bit of the message to arrive at the receiver including delays.

- ▶ Transmission Time
- ▶ Latency
- ▶ Transport Latency
- ▶ **Time of Flight (Page 388)**

163.

Falcon-A Simulator loads a FALCON-A binary file with a _extension and presents its contents into different areas of the simulator.

- ▶ .bin
- ▶ **.binfa (Page 5)**
- ▶ .fa
- ▶ None of the given

164. In machines where instructions can be executed in parallel or out of order, two additional hazards can occur: WAW and -----

- ▶ None of the given
- ▶ **WAR**
- ▶ RAW
- ▶ RAR

165. For ___ of an error we just need to know that there exists an error.

- ▶ None of the given
- ▶ Correction
- ▶ **Detection (Page 328)**
- ▶ Both Correction and Detection

166. Identify the type of serial communication error condition in which 0 is

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received instead of a stop bit (which is always a 1)?

▶ **Framing error (Page 240)**

- ▶ Parity error
- ▶ Overrun error
- ▶ Under-run error

167. _____ is/are defined as the number of instructions processed per second

▶ **Throughput (Page 203)**

- ▶ Latency Time to process 1 request.
- ▶ Throughput and Latency
- ▶ None of the given

168. Raid Level_ is not a true member of the RAID family.

▶ **0 (Page 330)**

- ▶ 2
- ▶ 3
- ▶ 4

169. Which one of the following is an address (binary bit pattern) issued by CPU?

- ▶ Memory
- ▶ **Effective (Page 39)**
- ▶ Base
- ▶ Next instruction

170. Which one the following interrupts is initiated with an INT instruction?

- ▶ Hardware
- ▶ **Software**
- ▶ Both hardware and Software
- ▶ None of the given

171. An -- is a program that takes basic computer instructions and converts them into a pattern of bits that the computer's processor can use to perform its basic operations.

- ▶ **Assembler**
- ▶ Debugger
- ▶ Editor
- ▶ Console

172. Dirty bit is a status bit which is used to indicate whether_____.

a. The block is accessible or not

b. The block has been modified or not

c. The block is valid or not

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d. The block has been accessed frequently or not

173. In 1x8 memory cell arrangement, each block is connected through a bi-directional data bus implemented with ___ tri-state buffer(s).

a. 1

b. 2 page 317

c. 4

d. 8

174. The register file is a collection of ___ bit wide registers used for data transfer between memory and the CPU.

a. 8

b. 16

c. 32 page 316

d. 64

175. _____ Human works with base 10 and computers work with base _____.

a. 8

b. 10

c. 2 page 301

c. 16

176. Raid level ___ distributes the parity strips across all disks.

a. 2

b. 3

c. 4

d. 5 page 300

177. Shifting of the radix point towards left or right is called _____

a. Shifting

b. Logical Shift

c. Right Shift

d. Scaling page 302

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178. In computers, floating-point representation uses ____ to encode significand, exponent and their sign in a single word

a. Decimal Numbers

b. Binary Numbers page 313

c. Octal Number

d. Hexa decimal Numbers

179. The _____ is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide memory address register (MAR).

a. Memory Buffer Register (MBR) page 316

b. Program Counter (PC)

c. Instruction Register (IR)

d. Memory Address Register (MAR)

180. Adding a data pin to a chip with 2^m words of s bits increases the number of bits it can store by only a factor of ____

a. $s/(s+1)$

b. $(s+1)/s$ page 320

c. $(s+2)/s$

d. s^2/s

181. A given block in cache is identified uniquely by its main memory blocknumber, referred to as ____.

i. Ticket

ii. Serial

c. Tag page 323

d. Label

182. The conversion of numbers from a representation in one base to another is known as ____.

a. Radix Conversion page 301

b. Number Representation

c. Decimal representation

d. Hexadecimal Representation

183. Multiple copies of the same data can exist in memory hierarchy simultaneously. The Cache needs updating mechanism to prevent old data values from being used. This is the problem of ____.

a. Cache Miss

b. Dirty bit

c. Cache Coherence page 327

d. Write Allocate

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184. Raid Level _____ is not a true member of the RAID family.

a. 0 page 298

- b. 2
- c. 3
- d. 4

185. In Double-Precision Binary Floating Point Representation the fraction is

a. 23 bits

b. 52 bits page 314

- c. 11 bits
- d. 1 bit

186. _____ is nonvolatile and may be written into only once.

a. PROM page 321

- b. EPROM
- c. EEPROM
- d. Main memory

187. _____ is non volatile i-e it retains the information in it when power is removed from it

- a. RAM
- b. Hard Disc

c. ROM page 320

d. Cache

188. A typical one level decoder has _____ input(s) and _____ output(s).

- i. n, n
- ii. 2^n , n
- iii. n, n^2

d. n, 2^n page 318

189. Along with the information bits, we add up another bit, which is called?

- a. Start bit
- b. Header bit

c. Parity bit page 297

d. Stop bit

190. Which of the following is NOT a function of memory cell?

a. Activate page 317

- b. DataIn
- c. DataOut
- d. Read/Write

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191. The ___ of an m digit number x is $\lfloor \frac{x^c}{b^m} \rfloor = \lfloor \frac{b^m - 1 - x}{b^m} \rfloor$

a. Radix Compliment

b. Diminished Radix Compliment page 304

c. Signed Magnitude Form

d. Biased Representation

192. _____ The memory management unit (MMU) is located between _____ and _____.

a. Main memory and secondary memory

b. The CPU and the physical memory page 328

c. Secondary memory and Virtual memory

d. ROM and RAM

193. Given an m-digit base b number x, the ___ of x is

$$x^c = (b^m - x) \bmod b^m$$

a. Radix Compliment page 304

b. Diminished Radix Compliment

c. Signed Magnitude Form

d. Biased Representation

194. For ___ of an error we just need to know that there exists an

a. Detection page 297

error.

b. Correction

c. Both Correction and Detection

d. None of the given

195. ___ is much faster than EPROM.

a. Main memory

b. Rom

c. Hard disk

d. Flash Memory page 321

196. CRC has ___ overhead as compared to Hamming code.

a. Equal

b. Greater

c. Lesser page 298

d. None of the given

197. very large page size results in increased _____.

a. Through put

b. access time page 330

c. Delay

d. Execution time

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198. For write to complete in Write through, the CPU has to wait. This wait state is called__.

- a. Write Buffer
- b. Cache Miss
- c. Write Allocate

d. Write Stalls page 327

199. The__ signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.

a. REQUEST page 316

- b. R/W
- c. COMPLETE
- d. None of the given

200. A 64kx1 Static RAM Chip has a cell array which consists of _____ row(s) and _____ column(s).

- a. 64, 1
- b. 1, 64
- c. 64, 256

d. 256, 256 page 317

201. ___ chips have quartz windows and by applying ultraviolet light data can be erased from them.

- a. PROM
- b. Flash Memory

c. EPROM page 321

d. EEPROM

202. ___ is the concept in which a process is copied into the main memory from the secondary memory according to the requirement.

a. Paging

b. Demand Paging page 329

- c. Segmentation
- d. Logical Partition

203. In virtual memory mechanism, pages are formulated in the _____ memory and brought into the _____ memory.

- a. Secondary, cache
- b. Main, cache
- c. Main, secondary

d. Secondary, main page 328

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204. Which is a status bit that indicates whether the block in cache has been modified or not modified?
- a. Presence bit
 - b. Dirty bit** page 327
 - c. Access bit
 - d. End bit
205. _____ refers to the fact that once a particular data item is accessed, it is likely that it will be referenced again within a short period of time.
- a. Spatial Locality
 - b. Temporal Locality** page 322
 - c. Full Locality
 - d. Half Locality
206. combination of parallel and sequential hardware used to build a multiplier is known as _____
- i. Parallel Array Multiplier
 - ii. Both Recording
 - iii. Series Parallel Multiplier**
 - iv. None of the given
207. When _____ signal is high, this would correspond to a read operation equivalent to having an input data to the CPU and output from the memory.
- a. R/W** page 316
 - b. COMPLETE
 - c. REQUEST
 - d. None of the given
208. The _____ is m-bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus Booth Recording
- a. memory address register (MAR)** page 316
 - b. memory Buffer Register(MBR)
 - c. Program counter (PC)
 - d. Instruction Register(IR)
209. Adding an address pin to a memory chip increases the capacity of memory by a factor of ____.
- a. 1.5
 - b. 2** page 320
 - c. 2.5
 - d. 3

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210. ___ is a read-mostly memory that can be written into at any time without erasing prior contents

- a. PROM
- b. EPROM
- c. Flash Memory

d. EEPROM page 321

211. A 16kx4 Static RAM Chip is arranged in the form of four _____ memory cells

a. 64x256 page 318

- b. 16x4
- c. 4x16
- d. 256x256

212. _____ is the simplest form for representing a signed number

- a. Biased Representation
- b. Diminished Radix Compliment Form

c. Sign Magnitude Form page 304

- d. None of the given

213. The Direct memory access (DMA) scheme results in direct link between _____ and _____.

- a. the CPU and the physical memory

b. main memory and secondary memory page 331

- c. Secondary memory and Virtual memory
- d. Cache memory and Registers

214. An entire _____ memory can be erased in one or a few seconds which is much faster than EPROM.

- a. PROM
- b. Cache
- c. EEPROM

d. Flash page 321

215. _____ refers to the fact when a given address has been referenced, the next address is highly probable to be accessed within a short period of time

- a. Temporal Locality

b. Spatial Locality page 322

- c. Full Locality
- d. Half Locality

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216. A _____ signal decides whether the input word should be shifted or bypassed.
- a. Control Read
 - b. shift/bypass page 312**
 - c. Control Write
 - d. None of the given
217. In _____ adder circuit we carry out from the previous stage to the next stage and so on.
- a. Ripple Carry Adder page 308**
 - b. Carry Look Ahead Adder
 - c. Complement Adder
 - d. 2's Complement Adder
218. In Single-Precision Binary Floating Point Representation the exponent is _____.
- a. 8 bits page 313**
 - b. 11 bits
 - c. 1 bit
 - d. 23 bits
219. Each memory reference issued by the CPU is translated from the logical address space to _____.
- a. Effective address
 - b. Physical address page 328**
 - c. Virtual address
 - d. Cache address
220. _____ are computed by the ALU and stored in processor status register.
- a. Condition codes page 311**
 - b. Conditional Branches
 - c. Fraction Division
 - d. None of the given
221. In _____, bits are encoded in pairs so there are only 'n/2' additions instead of 'n'.
- a. Booth Recording
 - b. Bit Pair Recording page 309**
 - c. Integer division
 - d. None of the given

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222. _____ is a combination of arithmetic, logic and shifter unit along with some multiplexers and control unit.

- a. Barrel Rotator
- b. Control Unit
- c. Flip Flop

d. ALU page 313

223. The cache contains a copy of portions of the _____.

a. Main memory page 321

- b. Rom
- c. EPROM
- d. Flash memory

224. What is the basic idea of “carry look ahead”?

- a. To reduce congestion

b. To speed up the ripple carry page 308

- c. To solve the redundancy
- d. To synchronize with CPU clock

225. Along with the information bits we add up another bit which is called the _____ bit.

- a. CRC
- b. Hamming
- c. Error Detection

d. Parity page 297

226. Virtual memory acts as a cache between _____ and _____.

- a. Secondary memory and Virtual memory
- b. Cache memory and Registers
- c. ROM and RAM

d. Main memory and secondary memory page 328

227. - Please choose one Which one of the following is the memory organization of SRC processor?

- $2^8 * 8$ bits
- $2^{16} * 8$ bits
- **$2^{32} * 8$ bits (Page 46)**
- $2^{64} * 8$ bits

228. Please choose one Type A format of SRC uses -----instructions

- **Two (Page 47)**
- three
- four
- five

229. - Please choose one The instruction -----will load the register R3 with the contents of the memory location M [PC+56]

• Add R3, 56

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- lar R3, 56
 - ldr R3, 56 (Page 47)
 - str R3, 56
230. - Please choose one Which format of the instruction is called the accumulator?
- 3-address instructions
 - 2-address instructions
 - 1-address instructions (Page 32)
 - 0-address instructions
231. Please choose one Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
- 4 bytes, 7 bytes
 - 7 bytes, 16 bytes (Page 36)
 - 10 bytes, 19 bytes
 - 13 bytes, 22 bytes
232. - Please choose one Which operator is used to name registers, or part of registers, in the Register Transfer Language?
- := (Page 66)
 - &
 - %
 - ©
233. - Please choose one The transmission of data in which each character is self-contained units with its own start and stop bits is -----
- Asynchronous
 - Synchronous
 - Parallel
 - All of the given options
234. - Please choose one Circuitry that is used to move data is called -----
- Bus
 - Port
 - Disk
 - Memory
235. - Please choose one Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
- Direct Memory Access (DMA).
 - Interrupt driven I/O
 - Programmed I/O
 - Virtual Memory (Page 268)
236. Please choose one Every time you press a key, an interrupt is generated. This is an example of
- Hardware interrupt (Page 275)
 - Software interrupt
 - Exception
 - All of the given
237. - Please choose one The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are
- Maskable
 - Non-maskable
 - Non-vectored
 - Vectored (Page 277)
238. - Please choose one Which is the last instruction of the ISR that is to be executed when the ISR terminates?
- IRET (Page 278)

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- IRQ
 - INT
 - NMI
239. - Please choose one If NMI and INTR both interrupts occur simultaneously, then which one has the precedence over the other
- NMI (Page 279)
 - INTR
 - IRET
 - All of the given
240. Identify the following type of serial communication error condition: The prior character that was received was not still read by the CPU and is over written by a new received character.
- Framing error
 - Parity error
 - Overrun error (Page 240)
 - Under-run error
241. -----the device usually means reading its status register every so often until the device's status changes to indicate that it has completed the request.
- Executing
 - Interrupting
 - Masking
 - Polling
242. - Please choose one Which I/O technique will be used by a sound card that may need to access data stored in the computer's RAM?
- Programmed I/O
 - Interrupt driven I/O
 - Direct memory access(DMA)
 - Polling
243. - Please choose one For increased and better performance we use _____ which are usually made of glass.
- Coaxial Cables
 - Twisted Pair Cables
 - Fiber Optic Cables (Page 390)
 - Shielded Twisted Pair Cables
244. - Please choose one In _____ if we find some call party busy we can have provision of call waiting.
- Delay System (Page 381)
 - Loss System
 - Single Server Model
 - None of the given
245. In _____ technique memory is divided into segments of variable sizes depending upon the requirements.
- Paging
 - Segmentation (Page 365)
 - Fragmentation
 - None of the given
246. - Please choose one For a request of data if the requested data is not present in the cache, it is called a _____
- Cache Miss (Page 358)
 - Spatial Locality
 - Temporal Locality
 - Cache Hit
247. Please choose one An entire _____ memory can be erased in one or a few seconds which is much faster than EPROM.

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- PROM
- Cache
- EEPROM
- Flash Memory (Page 356)

248. - Please choose one _____ chips have quartz windows and by applying ultraviolet light data can be erased from them.

- PROM
- Flash Memory
- EPROM (Page 356)
- EEPROM

249. - Please choose one The _____ signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.

- REQUEST (Page 350)
- COMPLETE
- None of the given

250. _____ is a combination of arithmetic, logic and shifter unit along with some multiplexers and control unit.

- Barrel Rotator]
- Control Unit
- Flip Flop
- ALU (Page 347)

251. - Please choose one In Multiple Interrupt Line, a number of interrupt lines are provided between the _____ modules.

- CPU and the I/O (Page 283)
- CPU and Memory
- Memory and I/O
- None of the given

252. - Please choose one The data movement instructions _____ data within the machine and to or from input/output devices.

- Store
- Load
- Move
- None of given (Page 141)

253. - Please choose one CRC has ----- overhead as compared to Hamming code.

- Equal
- Greater
- Lesser (Page 329)
- None of the given

254. - Please choose one The _____ is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide memory address register (MAR) .

- Instruction Register(IR)
- memory address register (MAR)
- memory Buffer Register(MBR) (Page 350)
- Program counter (PC)

255. In _____ technique, a particular block of data from main memory can be placed in only one location into the cache memory .

- Set Associative Mapping
- Direct Mapping (Page 360)
- Associative Mapping
- Block Placement

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256. - Please choose one _____ indicate the availability of page in main memory.
- Access Control Bits
 - Used Bits
 - **Presence Bits**
 - None of the given
257. The _____ RTN describes the overall effect of instructions on the programmer visible registers.
- **Abstract**
 - Concrete
 - Absolute
 - Basic
258. - Please choose one The instruction set is of _____ importance in governing the structure and function of the pipeline.
- Least
 - **Primary**
 - Secondary
 - No
 - Uestion
259. - Please choose one _____ is the most general and least useful performance metrics for RISC machines.
- **MIPS**
 - Instruction Count
 - Number of registers
 - Clock Speed
260. - Please choose one A _____ provides four functions: Select, DataIn, DataOut and Read/Write.
- ALU
 - Bus
 - Register
 - **Memory Cell (Page 351)**
261. Question No: 5 (Marks: 1) - Please choose one We can classify or partition the SRC instructions by their overall _____ behavior.
- **Register transfer**
 - Memory transfer
 - Execution
 - Logical
262. - Please choose one The _____ RTN describes detailed register transfer steps in the data path that produce the overall effect.
- Abstract
 - **Concrete**
 - Absolute
 - Basic
263. Please choose one All members of the MC68000 family are _____ processors.
- **32-bit**
 - 16-bit
 - 64-bit
 - 8-bit
264. - Please choose one _____ Operations refers to a processor that can issue more than one instruction simultaneously.
- Macro
 - Micro

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- Scalar
 - **Superscalar click here for detail**
265. - Please choose one Exceptions which are _____ occur in response to events that are paced by the internal processor clock.
- Asynchronous
 - **Synchronous click here for detail**
 - Internal
 - External
266. - Please choose one In the hazard detection by hardware, resolved by pipeline stalls, if the instructions are in the adjoining stages, then the hazard must be detected in stage _____.
- 4
 - 2
 - **3**
 - 1
267. Please choose one 16k x4 static RAM Chip is arranged in the form of four _____ cells.
- 16x512
 - 32x512
 - 256x512
 - **64x256 (Page 352)**
268. - Please choose one In a DRAM cell, the storage capacitor will discharge in around _____
- **4 -15 ms (Page 354)**
 - 2 - 10 ms
 - 5-20 ms
 - 10-25 ms
269. Please choose one 1-bit sign, 8-bit exponent, 23-bit fraction and a bias of 127 is used for _____ Binary Floating Point Representation
- Double precision
 - **Single Precision (Page 348)**
 - All of above
 - Half Precision
270. - Please choose one The average rotational latency if the disk rotated at 20,000rpm is _____
- 0.5 ms
 - 3.5 ms
 - 2.5 ms
 - **1.5 ms (Page 324)**
271. Question No: 5 (Marks: 3) - Please choose one A hard disk with 5 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector. What is the total capacity of the disk?
- 1.5 GB
 - **1 GB (Page 324)**
 - 2 GB
 - 3 GB
272. Where does the processor store the address of the first instruction of the ISR?
- **Interrupt vector (Page 277)**
 - Interrupt request
 - Interrupt handler
 - All of the given options
273. In _____, a separate address space of the CPU is reserved for I/O operations.
- **Isolated I/O (Page 236)**

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- Memory Mapped I/O
 - All of above
 - None of above
274. ----- is the time needed by the CPU to recognize (not service) an interrupt request.
- **Interrupt Latency (Page 279)**
 - Response Deadline
 - Timer delay
 - Throughput
275. _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
- Microprogramming
 - Instruction pre-fetching
 - Pipelining
 - **Partial decoding (Page 255)**
276. How can you define an interrupt?
- A process where an external device can speedup the working of the microprocessor
 - A process where memory can speed up programs execution speed
 - **A process where an external device can get the attention of the microprocessor**
 - A process where input devices can takeover the working of the microprocessor
277. An interface that can be used to connect the microcomputer bus to _____ is called an I/O Port.
- Flip Flops
 - Memory
 - **Peripheral devices (Page 234)**
 - Multiplexers
278. A software routine performed when an interrupt is received by the computer is called as -----
- Interrupt
 - **Interrupt handler**
 - Exception
 - Trap
279. Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
- Daisy-Chaining Priority
 - Asynchronous
 - **Priority Parallel Priority (Page 281)**
 - Semi-synchronous Priority
280. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
- Asynchronous
 - **Daisy-Chaining Priority**
 - Parallel
 - Semi-synchronous
281. Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
- **Framing error (Page 240)**
 - Parity error
 - Overrun error
 - Under-run error
282. Identify the following type of serial communication error condition in which no character is available at the

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beginning of an interval.

- Framing error
- Parity error
- Overrun error
- **Under-run error (Page 240)**

283. _____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.

- **Computer**
- Hazard
- Memory
- Disk

284. Connection to a CPU that provides a data path between the CPU and external devices, such as a keyboard, display, or reader is called-----

- Processer
- Program
- **Buses**
- memory address

285. VLIW stands for -----

- Very Lengthy Interaction Word
- Very Length Instruction Width
- Very Long Instruction Word (Page 219)
-) none of given options

286. A -----is a wiring scheme in which, for example, device A is wired to device B, device B is wired to device C, device C is wired to device D etc.

- **Daisy chain**
- DMA
- Interrupt driven
- I/O Polling

287. Question # 8 of 10 (Total Marks: 1) Select correct option: An ----- is the memory address of an interrupt handler.

- **Interrupt vector**
- Interrupt service routine
- Exception
- Mask

288. The conversion of numbers from a representation in one base to another is known as _____

- **Radix Conversion (Page 333)**
- Number Representation
- Decimal representation
- Hexadecimal Representation

289. If an interrupt is set by the timer component or by the peripheral device then how would you categorize it?

- **Hardware**
- Software
- Exception
- All of the given options

290. : 1 In which one of the following interrupts the device have to supply the address of the subroutine to the

- Microprocessor
- Maskable
- **Non-maskable click here for detail**
- Non-vectored Vectored

291. ----- interrupts are usually associated with the software

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- Hardware
 - software
 - Machine
 - internal
292. When the address of the subroutine is already known to the Microprocessor then it is called as ----- interrupt.
- Maskable
 - Non-maskable
 - Non-vectored
 - Vectored
293. How Interrupt driven I/O is better than polling because?
- Interrupt driver I/O is easy to design
 - Interrupt driver I/O is enhanced version of polling.
 - Interrupt driver I/O does not waste time on checking which device is available. (Page 274)
 - Interrupt driven I/O is easy to program.
294. In Single-Precision Binary Floating Point Representation the exponent is _____
- 8 bits (Page 348)
 - 11 bits
 - 1 bit
 - 23 bits
295. : The _____ is m-bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus Booth Recording
- memory address register (MAR) (Page 350)
 - memory Buffer Register(MBR)
 - Program counter (PC)
 - Instruction Register(IR)
296. A combination of parallel and sequential hardware used to build a multiplier is known as _____
- Parallel Array Multiplier
 - Booth Recording
 - Series Parallel Multiplier (Page 342)
 - None of the given
297. The register file is a collection of _____ bit wide registers used for data transfer between memory and the CPU .
- 8
 - 16
 - 32 (Page 350)
 - 64
298. The _____ of an m digit number x is $x_c' = bm - 1 - x$
- Radix Compliment
 - Diminished Radix Compliment (Page 337)
 - Signed Magnitude Form
 - Biased Representation
299. Shifting of the radix point towards left or right is called _____
- Shifting
 - Logical Shift
 - Right Shift
 - Scaling (Page 335)
300. Question # 7 of 10 (Total Marks: 1) Select correct option: In _____ adder circuit we feed carry out from the previous stage to the next stage and so on.
- Ripple Carry Adder (Page 341)
 - Carry Look Ahead Adder
 - Complement Adder

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- 2's Complement Adder
301. _____ are computed by the ALU and stored in processor status register.
- **Condition codes (Page 334)**
 - Conditional Branches
 - Fraction Division
 - None of the given
302. A _____ signal decides whether the input word should be shifted or bypassed
- . Control Read
 - **Shift/bypass (Page 346)**
 - Control Write
 - None of the given
303. Along with information bits we add up another bit which is called the _____ bit.
- CRC
 - Hamming
 - Error Detection
 - **Parity (Page 328)**
304. In _____ recording ,bits are encoded in pairs so there are only ' n/2' additions instead of 'n'.
- Booth Recording
 - **Bit Pair Recording (Page 343)**
 - Integer division
 - None of the given
305. _____ signal is high, this would correspond to a read operation equivalent to having an input data to the CPU and output from the memory REQUEST .
- **R/W (Page 350)**
 - COMPLETE
 - REQUEST
 - None of the given
306. Given an m-digit base b number x, the _____ of x is $x_c = (b^m - x) \bmod b^m$
- **Radix Compliment (Page 337)**
 - Diminished Radix Compliment
 - Signed Magnitude Form
 - Biased Representation
307. For _____ of an error we just need to know that there exists an error.
- **Detection (Page 328)**
 - Correction
 - Both Correction and Detection
 - None of the given
308. In Double-Precision Binary Floating Representation the function is _____
- 23 bits
 - **52 bits (Page 348)**
 - 1 bits
 - 1 bit
309. : _____ is the simplest form for representing a signed number
- Based representation
 - Diminished Redex Complement Form
 - **Sign Magnitude Form (Page 336)**
 - None of the given
310. In computers, floating-point representation uses _____ to encode significand, exponent and their sign in a single word
- Decimal Numbers

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- Binary Numbers (Page 347)

- Octal Numbers
- Hexa decimal Numbers

311. : Which one of the following registers store a previously calculated value or a value loaded from the main memory?
- ▶ Accumulator
 - ▶ Address Mask
 - ▶ Instruction Register
 - ▶ Program Counter
312. Which one of the following portions of an instruction represents the operation to be performed?
- ▶ Address
 - ▶ Instruction code
 - ▶ Opcode (Page 33)
 - ▶ Operand
313. _____ control signal enable the input to the PC for receiving a value that is currently on the internal processor bus.
- ▶ LPC (Page 172)
 - ▶ INC4
 - ▶ LC
 - ▶ Cout
314. What is the instruction length of the FALCON-E processor?
- ▶ 8 bits
 - ▶ 16 bits
 - ▶ 32 bits (Page 134)
 - ▶ 64 bit
315. Which type of instructions enables mathematical computations?
- ▶ Arithmetic (Page 92)
 - ▶ Control
 - ▶ Data transfer
 - ▶ None of the given
316. What is the instruction length of the SRC and Falcon E processor?
- ▶ 8 bits
 - ▶ 16 bits
 - ▶ 32 bits (Page 134)
 - ▶ 64 bits
317. : An instruction that specifies one operand in memory and one operand in a register would be known as a _____ address instruction.
- ▶ 2-1/2
 - ▶ 1-1/2 (Page 37)
 - ▶ 0
 - ▶ 2
318. In floating point representations _____ is also called mantissa.
- ▶ Sign
 - ▶ Base
 - ▶ Significant (Page 347)
 - ▶ Exponent
319. What should be the behavior of interrupts during critical sections?
- ▶ Must remain disable (Page 197)
 - ▶ Must remain Enable
 - ▶ Can be either enable or disable

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▶ only important interrupts be enable

320. Which one of the following is a binary cell capable of storing one bit of information?
- ▶ Decoder
 - ▶ Flip-flop (Page 76)
 - ▶ Multiplexer
 - ▶ Diplexer
321. Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?
- ▶ Arithmetic
 - ▶ Control
 - ▶ Data transfer (Page 88)
 - ▶ Floating point
322. What does the RTL expression [M(1234)] means?
- ▶ The contents of memory whose address is 1234.
 - ▶ The contents of data register 1234
 - ▶ The effective address of register 1234
 - ▶ The address of memory whose address is 1234.
323. Which one of the following languages presents a simple, human-oriented language to specify the operations, register communication and timing of the steps that take place within a CPU to carry out higher level (user programmable) instructions?
- ▶ Assembly Language
 - ▶ OOP(Object Oriented Language)
 - ▶ RTL (Register Transfer Language)
 - ▶ UML(Unified Modeling language)
324. Which one of the following instructions is used to load register from memory using a relative address?
- ▶ la
 - ▶ lar
 - ▶ ldr (Page 145)
 - ▶ str 23
325. Taking control of the system bus for a few bus cycles is known as _____.
- ▶ Bus Stealing
 - ▶ Cycle Stealing (Page 317)
 - ▶ Cycle Transferring
 - ▶ None of given
326. : In-----address mode, the actual data is stored in the instruction.
- ▶ Direct
 - ▶ Indirect
 - ▶ Immediate
 - ▶ Relative
327. Keyboard Interrupt (INT 9) is an example of ----- interrupt.
- ▶ Hardware
 - ▶ Software
328. user program has to delete a file. The user program will be executing in the user mode. When it makes the specific system call to delete the file, an interrupt will be generated, this will cause the processor to halt its current activity and switch to supervisor mode. Once in supervisor mode, the operating system will delete the file and then control will return to the user program. This is an example of
- ▶ Hardware interrupt
 - ▶ Software interrupt (Page 275)
 - ▶ Exception

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- ▶ All of the given
329. By which file extension does the FALCON-A Assembler loads a FALCON-A assembly file?
- ▶ **.asmfa (Page 8)**
 - ▶ .org
 - ▶ .exe
 - ▶ .src 24
330. All -----interrupts have priority over all -----interrupt
- ▶ **internal, external (Page 279)**
 - ▶ external, internal
331. The ----- can also be used anywhere in the source file to force code at a particular address in the memory.
- ▶ .end directive
 - ▶ .start directive
 - ▶ **.org directive (Page 298)**
 - ▶ .label directive
332. : In this figure, the constant value specified by the immediate field is added to the register value, and the resultant is the index of memory location that is referred i.e. Effective Address = A + (content of R) . Identify the addressing mode.
- ▶ **Displacement (Page 139)**
 - ▶ Immediate
 - ▶ Indexed
 - ▶ Relative
333. In which one of the following addressing modes, the operand does not specify an address but it is the actual data to be used.
- ▶ Direct
 - ▶ Indirect
 - ▶ **Immediate click here for detail**
 - ▶ Relative 25
334. : When is the “Divide error interrupt generated?
- ▶ When an attempt is made to divide by decimal number
 - ▶ When an attempt is made to multiply by zero
 - ▶ **When an attempt is made to divide by zero (Page 197)**
 - ▶ When negative number is stored in a register
335. Which one of the following is a term used to describe a storage systems' resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques?
- ▶ Interrupt handling
 - ▶ Programmed I/O
 - ▶ Polling
 - ▶ **RAID click here for detail**
336. : _____ is the time for first bit of the message to arrive at the receiver including delays.
- ▶ Transmission Time
 - ▶ Latency
 - ▶ Transport Latency\
 - ▶ **Time of Flight (Page 388)**
337. Falcon-A Simulator loads a FALCON-A binary file with a _____ extension and presents its contents into different areas of the simulator.
- ▶ .bin
 - ▶ **.binfa (Page 5)**
 - ▶ .fa
 - ▶ None of the given
338. In machines where instructions can be executed in parallel or out of order, two additional hazards can occur:

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WAW and -----

- ▶ None fo the given
- ▶ WAR
- ▶ **RAW**
- ▶ RAR

