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Past Papers by Waqar Siddhu  
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What is distributed computing?

Answer ( [Please click here to Add Answer](#) )

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In distributed computing, all elements which are interconnected operate under one operating system. To a user, it appears as a virtual uni-processor system.

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Write any two differences between EAGLE and Modified EAGLE.

Answer ( [Please click here to Add Answer](#) )

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The modified EAGLE is an improved version of the processor EAGLE. there were several limitations in EAGLE, and these have been remedied in the modified EAGLE processor.

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Differentiate between selector channel and multiplexer channel.

Answer ( [Please click here to Add Answer](#) )

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**Selector Channel** It is the DMA controller that can do block transfers for several devices but only one at a time.

**Multiplexer Channel** It is the DMA controller that can do block transfers for several devices at once.

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Differentiate between PROM and EPROM.

Answer ( [Please click here to Add Answer](#) )

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**PROM** The PROM stands for Programmable Read only Memory. It is also nonvolatile and may be written into only once. For PROM, the writing process is performed electrically in the field. PROMs provide flexibility and convenience.

**EPROM** Erasable Programmable Read-only Memory or EPROM chips have quartz windows and by applying ultraviolet light erase the data can be erased from the EPROM. Data can be restored in an EPROM after erasure. EPROMs are more expensive than PROMs and are generally used for prototyping or small-quantity, special purpose work.

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How can you define an instruction set? Name the essential elements of computer instructions.

Answer ( [Please click here to Add Answer](#) )

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**INSTRUCTION SET** An instruction set is a collection of all possible machine language commands that are understood and can be executed by a processor.

**ESSENTIAL ELEMENTS OF COMPUTER INSTRUCTIONS:** There are four essential elements of an instruction; **the type of operation to be performed**, **the place to find the source operand(s)**, **the place to store the result(s)** and **the source of the next instruction** to be executed by the processor.

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What is the relationship between hard disk Platters, Tracks and Sectors?

Answer ( [Please click here to Add Answer](#) )

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A hard disk is the most frequently used peripheral device. It consists of a set of platters. Each platter is divided into tracks. The track is subdivided into sectors. To identify each sector, we need to have an address. So, before the actual data, there is a header and this header consisting of few bytes like 10 bytes. Along with header there is a trailer. Every sector has three parts: a header, data section and a trailer.

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Find out the Sign, Significand and Exponent from the following floating point number.

$$-0.7 \times 10^{-4}$$

Answer ( [Please click here to Add Answer](#) )

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**Sign = 0**

**Significand= 0.7**

**Exponent= -4**

**Base = 10= fixed for given type of representation**

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What is the use of translation lookaside buffer (TLB) and how it is implemented inside the CPU?

Answer ( [Please click here to Add Answer](#) )

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To speed up the process of virtual address translation, translation Lookaside buffer (TLB) is implemented; as a small cache inside the CPU, which stores the most recent page table entry reference made in the MMU.

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Write the Structural RTL description for "un-conditional jump" instruction i.e. **jump [ra+c2]**.

Answer ( Please [click here](#) to Add Answer )

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Rich text editor toolbar showing icons for file operations, undo, redo, bold, italic, underline, and text alignment. The font is set to Arial, size 12, and zoom is 100%.

Step	RTL
T0-T2	Instruction Fetch
T3	$(ra=0): A \leftarrow PC, (ra \neq 0): A \leftarrow R[ra];$
T4	$C \leftarrow A + c2(\text{sign extend});$
T5	$PC \leftarrow C;$

Step	RTL
T0-T2	Instruction fetch
T3	$n<4..0> \leftarrow IR<4..0>;$
T4	$C \leftarrow (N \neq 0) \oplus R[rb]<15..N>;$
T5	$R[ra] \leftarrow C;$

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A hard disk with 10 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector. What is the total capacity of the disk?

Answer ( [Please click here to Add Answer](#) )

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512 bytes x 512

sectors=0.2MB/track

0.2MB x 1024 tracks =0.2GB/platter

Therefore the hard disk has the total capacity of  $10 \times 0.2=2\text{GB}$

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Question No : 51 of 52

Marks: 5 (Budgeted Time 10 Min)

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Show all the steps involved in integer division algorithm to divide  $45_{10}$  by  $5_{10}$ .

Answer ( Please click here to Add Answer )

Rich text editor toolbar with icons for Bold, Italic, Underline, Bulleted List, Numbered List, Indent, Outdent, Undo, Redo, and a 100% zoom level.

**D 000000 101101 , d= 000101**

D=000001 011010  
d=000101

Dif(-) q=0

D=000010 110100  
d=000101

Dif(-) q=00

D=000101 101000  
d=000101

Dif(+) q=001

D=000001 010000  
d=000101

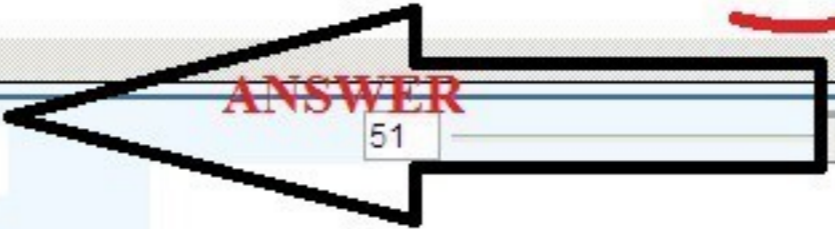
Dif(-) q=0010

D=000010 100000  
d=000101

Dif(-) q=00100

D=000101 000000  
d=000101

Dif(+) q=001001



Start Time: 7:37 PM  
**116:00**  
 Time Left

Hence remainder =  $(000000)_2 = 0$   
 Quotient =  $(001001)_2 = 9_{10}$

51

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Suppose an I/O system with a single disk gets (on average) 100 I/O requests/second and the average time for a disk to service an I/O request is 6ms. What is the utilization of the I/O system?

Answer ( [Please click here to Add Answer](#) )

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Time for an I/O request = 6ms  
= 0.006sec

Server utilization =  $100 \times 0.006$   
= 0.6 sec

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Differentiate between Latency and throughput.

Answer ( [Please click here to Add Answer](#) )

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Latency is defined as the time required to process a single instruction, while throughput is defined as the number of instructions processed per second

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Which attributes a device should have in order to be qualified as a master device?

Answer ( [Please click here to Add Answer](#) )

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A Master must have the capability to place addresses on the address bus and direct the bus activity during a buscycle

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Differentiate between Spatial Locality and Temporal Correlation.

Answer ( [Please click here to Add Answer](#) )

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**Spatial Locality** This would mean that in a part of a program, if we have a particular address being accessed then it is highly probable that the data available at the next address would be highly accessed.

**Temporal Correlation** In this case, we say that at a particular time, if we have utilized a particular part of the memory then we might access the adjacent parts very soon.

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Name any two methods that are used to measure I/O subsystem performance.

Answer ( [Please click here to Add Answer](#) )

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Differentiate between sender overhead and receiver overhead related to performance issues of networks.

Answer ( [Please click here to Add Answer](#) )

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**Sender overhead** It is the time for the processor to inject message in to the network.

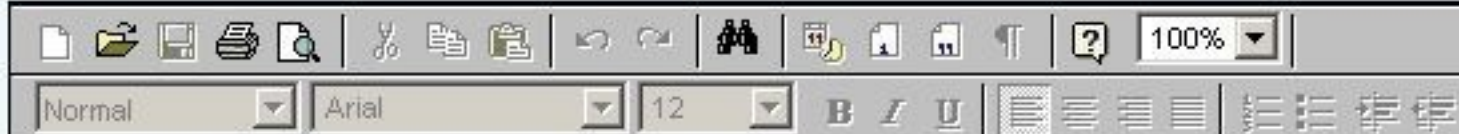
**Receiver overhead** It is the time for the processor to pull the message from the network.

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Write down the categories of instructions supported by FALCON-A processor and also state that in type 1 instruction format of FALCON-A, how many bits are reserved for the op-code?

Answer ( [Please click here to Add Answer](#) )

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Find the average rotational latency (in milliseconds) of the disk if it rotates at 15,000 rpm.

Answer ( [Please click here to Add Answer](#) )

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If a DRAM has 512 rows and its refresh time is 8ms, what should be the average frequency of row refresh operation?

Answer ( [Please click here to Add Answer](#) )

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Refresh time =8ms

Number of rows =512

Therefore we have to do 512 row refresh operations in a 9 ms interval, in other words

one row refresh operation every  $= (8 * 10^{-3}) / 512$   
 $= 1.56 * 10^{-5}$  second

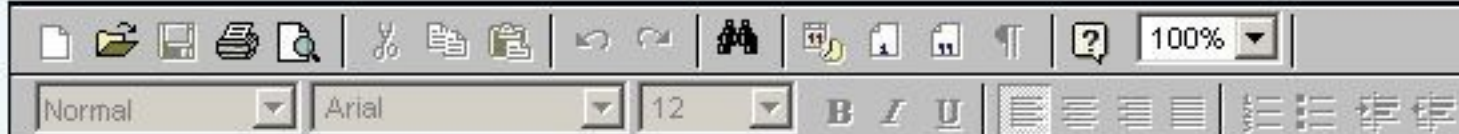
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Briefly explain the following features of FALCON-E.

- Number of registers
- Size of each register
- Memory word size
- Memory space

Answer ( [Please click here to Add Answer](#) )

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Explain briefly how the interrupting module is identified in software polling and also point out the major drawback of Software Poll and Daisy Chain.

Answer ( [Please click here to Add Answer](#) )

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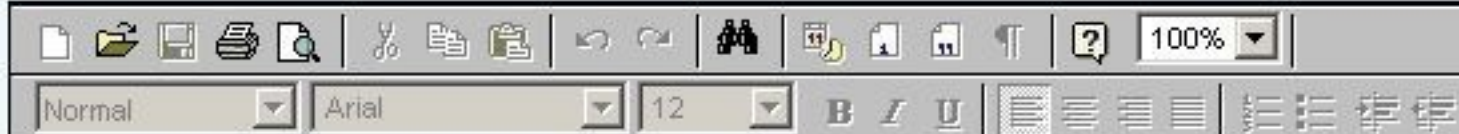


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According to the Radix conversion algorithm, convert the hexadecimal number  $C4_{16}$  to base 10 (Write down all the steps which are involved in conversion).

Answer ( [Please click here to Add Answer](#) )

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Find the average access time of a level of memory hierarchy if the hit rate is 80%. The memory access takes 10ns on a hit and 100ns on a miss.

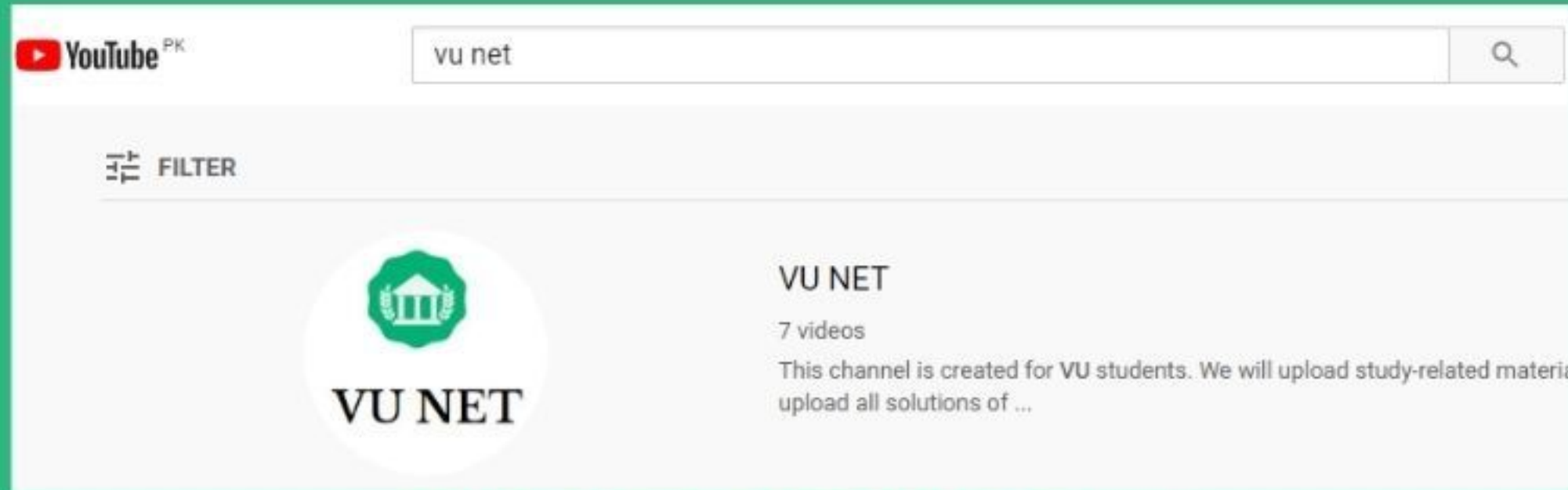
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