CS501 QUIZ 1 SOLVED

1. ___is/are example(s) of synchronous communication.

a) Register to Register

b) Register to Memory

c) Memory to Memory

d) All of the given

2. Which of the following pins of the processor is designated for maskableinterrupts?

a) NMI

b) MI

c) INTR

d) RINT

3. ET = _____

a) CP x IC x T

b) CPI x IC x T

c) CPI / IC x T

d) CPI x IC/T

4. By which file extension does the FALCON-A assembler loads a FALCON-Aassembly file?

a) .asmfa

b) .org

c) .exe

d) .src

5. _____signal has output direction with respect to printer

a) O<7…0>

b) STROBE#

c) INT#

d) ACKNLG#

6. ___is said to occur when a 0 is received instead of a stop bit

a) Framing error

b) Party error

c) Block error

d) Over-run error

7. A component connected to the system bus and having control of it during aparticular bus cycle is called _

a) Slave component

b) Master component

c) System bus

d) Buffer component

8. The information about the interrupt vector is given in 8-bit from 0 to 7, which is translated to bit____on the data bus

a) 16 to 32

b) 11 to 18

c) 0 to 7

d) 8 to 15

9. Every interrupt handler has an interrupt return (IRET) instruction, thisinstruction is an example of__return

a) NEAR

b) FAR

c) SHORT

d) RELATIVE

10. Which I/O technique will be used by a sound card that may need to access data stored in the computer`s RAM?

a) Programmed I/O

b) Interrupt driven I/O

c) Direct memory access(DMA)

d) Polling

11. What should be the behavior of interrupt during critical section?

a) Must remain disable

b) Must remain enable

c) Depends on current situation

d) Only important interrupts be enabled

12. Identify the type of serial communication error condition in which “0” isreceived instead of stop bit(which is always a “1”)

a) Framing error

b) Parity error

c) Overrun error

d) Under run error

13. The Pentium does allow the use of some part of its_____accumulator registerEAX

a) 8 bits

b) 16 bits

c) 32 bits

d) 64 bits

14. Where does the processor store the address of the first instruction of the ISR?

a) Interrupt vector

b) Interrupt request

c) Interrupt handler

d) All of the given options

15. ___is the time needed by the CPU to recognize (not service) aninterrupt request.

a) Interrupt latency

b) Response deadline

c) Timer delay

d) Throughput

16. At the start of the transfer operation in synchronous communication, the master activates the_signal.

a) Read

b) Enable

c) Data

d) Acknowledge

17. Which is the last instruction of the ISR that is to be executed when the ISR terminates?

a) IRET

b) IRQ

c) INT

d) NMI

18. Which one of the following methods for resolving the priority makes use ofindividual bits of a priority encoder?

a) Daisy-Chaining Priority

b) Asynchronous Priority

c) Parallel Priority

d) Semi-synchronous Priority

19. Tri-state buffers are used for removing____.

a) Instruction collision

b) bus collision

c) Instruction contention

d) bus contention

20. When a particular sector is found, the data is transferred to_____.

a) RAM

b) I/O module

c) Cache memory

d) Instruction registers

21. Interrupt driven I/O is better than____.

a) Polling

b) Data forwarding

c) Stall

d) First In First Out

22.Select the parts of a hard disk.

a) Header only

b) Data section and a trailer

c) Data section only

d) Header, data section and a trailer

23. In the little-endian format exchanging data between computer, the datatransmitted by one will be received in a “swapped” form by the other.

a) Organized

b) Signals

c) Swapped

d) Arranged

24. In which technique does the hardware directly access host memory for readingor writing independent of CPU?

a) Direct Memory Access (DMA)

b) Programmed I/O

c) Interrupt driven I/O

d) Polling

25. Most parallel I/O ports used with peripheral devices are mapped on a range of _____.

a) Bus addresses

b) Direct memory access

c) Contiguous addresses

d) Cache

26. ___signal is used in printer with DB-25 interface to reset its controller.

a) #PE

b) #STROB

c) #INIT

d) #SLCT

27. Why DMA is faster than Programmer I/O technique because?

a) DMA transfers data directly using CPU

b) DMA transfers data directly without using CPU

c) DMA uses buffers with CPU

d) DMA uses interrupted driven I/O

28. In 8086/8088 processor, interrupt vector table is located at the memory location _____.

a) 0

b) 4

c) 256

d) 1024

29. When an I/O module has a capability of executing a specific set of instructionsfor specific I/O devices in the memory without the involvement of CPU is called ____

a) Selector Channel

b) I/O Channel

c) I/O processors

d) Cycle Stealing

30. ___lets the user execute the program, one instruction at a time.

a) Single Step

b) Execute

c) Change PC

d) List File

31. Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?

a) Direct Memory Access (DMA)

b) Interrupt driven I/O

c) Programmed I/O

d) Virtual Memory