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1. Which is the last instruction of the ISR that is to be executed when the ISR terminates?

Options:

- IRET
- IRQ
- NMI
- INT

Correct Option: IRET

2. Where does the processor store the address of the first instruction of the ISR?

Options:

- Interrupt handler
- Interrupt vector
- Interrupt vector table
- Interrupt service routine

Correct Option: Interrupt vector

3. The third stage of the Pipelined version of SRC is:

Options:

- Instruction Fetch

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- Register Write
- Memory Access
- ALU Operation

Correct Option: ALU Operation

4. Interrupt-driven I/O is better than _____.

Options:

- Polling
- Data Forwarding
- First In First Out
- Stall

Correct Option: Polling

5. _____ is an example of a synchronous communication error condition in which "0" is received instead of a stop bit (which is always a "1").

Options:

- Under-run error
- Overrun error
- Parity error
- Framing error

Correct Option: Framing error

6. Every time you press a key, an interrupt is generated. This is an example of:

Options:

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- None of the given
- All of the given
- Software interrupt
- Hardware interrupt

Correct Option: Hardware interrupt

7. The multiplexer _____ is used to decide which value is transferred to be written back to the register file.

Options:

- MP5
- MP4
- MP2
- MP3

Correct Option: MP2

8. The information about interrupt vector is given in 8-bits, from bit 0 to 7, which is translated to bit _____ on the data bus.

Options:

- 0 to 7
- 11 to 18
- 11 to 16
- 16 to 23

Correct Option: 0 to 7

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9. In the little-endian format exchanging data between computers, the data transmitted by one will be received in a "swapped" form by the other.

Options:

- Organized
- Arranged
- Signals
- Swapped

Correct Option: Swapped

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