# CS-501 Advanced Computer Architecture

# Update MCQS For Quiz-1 File

# Solve By Vu Topper RM



بری صحبت سے تنہائی بہتر ہے اور تنہائی سے نیک صحبت بہتر ہے

**Question No:1** **(Marks:1)** **Vu-Topper RM**

In Falcon-A processor, the size of each I/O port is _____.

**A. 8 bits**

B. 16 bits

C. 256 bytes

D. 8 bytes

**Question No:2** **(Marks:1)** **Vu-Topper RM**

Total number of data registers in Motorola 68000 processor are _____.

**A. 8**

B. 12

C. 24

D. 32

**Question No:3** **(Marks:1)** **Vu-Topper RM**

Which notation do we use to name different fields of a register in RTL?

A. +

B. <-

**C. :=**

D. ()

**Question No:4** **(Marks:1)** **Vu-Topper RM**

In EAGLE, the maximum number of operands allowed in an instruction are _____.

A. 2

**B. 4** **Page 120**

C. 6

D. 8

**Question No:5** **(Marks:1)** **Vu-Topper RM**

Which of the following instruction is considered most important in a pipelined EAGLE architecture?

A. INIT
**B. NOP**
C. HALT
D. RESET

**Question No:6** **(Marks:1)** **Vu-Topper RM**

The size of data bus of MC68000 processor is _____.

A. 8 bits
**B. 16 bits**
C. 32 bits
D. 64 bits

**Question No:7** **(Marks:1)** **Vu-Topper RM**

In Type-1 instruction, bits _____ are reserved for the op-code.

**A. bits 1 through 5** **Page 91**
B. bits 0 through 4
C. bits 0 through 8
D. bits 11 through 15

**Question No:8** **(Marks:1)** **Vu-Topper RM**

Which of the given below measure(s) is/are used for comparison of performance of various machines?

A. MIPS
B. MFLOPS
C. Execution time
**D. All of the these**

**Question No:9** **(Marks:1)** **Vu-Topper RM**

Which field of the machine language instruction is the "type of operation" that is to be performed?

**A. Op-code** **Page 33**
B. I/O locations
C. Memory cells

D. CPU registers

**Question No:10 (Marks:1) Vu-Topper RM**

Which of the following bits of SRC instruction are used to hold an operand, an address index, or a branch target register?

A. The bits 16 through 0
B. The bits 17 through 0
C. The bits 26 through 22
**D. The bits 21 through 17**

"If P = 1, then load the contents of register R1 into register R2". This statement can be written in RTL as:

A. R1 ¬ R2
B. P: R1 ¬ R2
**C. P: R2 ¬ R1**
D. P: R2 ¬ R1, P: R1 ¬ R2

Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?

**A. :=**
B. %
C. @
D. &

A _____ is a computer program used to aid indetecting errors in a program.

A. Linker
B. Compiler
C. Assembler
**D. Debugger Page 24**

In which of the following addressing modes, the address of the memory from where the value is to be accessed is given in the instruction?

A. Direct Addressing
**B. Indirect Addressing** **Google**
C. Immediate Addressing
D. Register Direct Addressing

In EAGLE processor, which of the following notations is used to represent a memory word stored at address 8?
A. M [8]<0…15> := M [8] © M [9]
B. M [8]<0…15> := M [9] © M [8]
C. M [8]<15…0> := M [9] © M [8]
**D. M [8]<15…0> := M [8] © M [9]**

RTL statements separated by _____ are always executed in same clock pulse.
A. Hash (#)
B. Colon (:)
**C. Comma (,)** **Page 66**
D. Semi-colon (;)

In "DIV R3" instruction of EAGLE, the register _____ is used as both source operand and destination operand.
A. R0
**B. R2**
C. R1
D. R3

In EAGLE processor, the size of an instruction is _____.
A. 8 bit
**B. 16 bit**
C. Either 8-bits or 16-bits
D. Neither 8-bits nor 16-bits

Which of the following branch instructions has a condition which is always executed?

A. jmi
**B. jump**
C. jz
D. jpl

Which type of Instruction is stored in instruction register (IR)?

A. Previously executed instruction
**B. Next instruction to be executed**
C. Next branch instruction in the instruction sequence
D. Current instruction being executed

If the most significant two digits of hexadecimal equivalent of an SRC instruction are "E1", the opcode of such an instruction is _____.

A. str
B. shl
C. shr
**D. Didr**

Which of the following RTL descriptions is used to represent the target register of Falcon-A instruction?

**A. rb<2..0> := IR<10..8>**
B. ra<2..0> := IR<10..8>
C. rc<2..0> := IR<4..2>:
D. rb<2..0> := IR<7..5>:

In SRC, the memory is accessed in the chunks of _____ byte(s) each.

**A. 2**
B. 4
C. 6
D. 8

In a Falcon-E instruction, _____ bits are reserved for opcode.

A. 2
B. 4
**C. 6**
D. 8

Which of the following directives is used in FALSIM to define a variable?

A. .dd
**B. .dw**
C. .org
D. .equ

The instruction "Shiftl R1, R2, 20" is an example of which of the following addressing modes?

A. Displacement
B. Relative
C. Immediate
**D. Register**

**Question No:11 (Marks:1) Vu-Topper RM**

Program counter (PC) holds the memory address of _____?

**A. Next instruction Page 104**
B. Current Instruction
C. Previous Instruction
D. Previous and Current Instruction

**Question No:12 (Marks:1) Vu-Topper RM**

For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory

A. Jump
B. Branch

C. Control
**D. load/store Page 89**

**Question No:13 (Marks:1) Vu-Topper RM**
To implement an N-bit barrel shifter in form of a combinational circuit, we require N _____.
A. Selectors
**B. Multiplexers**
C. Demultiplexers
D. Tri-state buffers

**Question No:14 (Marks:1) Vu-Topper RM**
Which type of instructions help in changing the flow of the program as and when required?
**A. Control Page 137**
B. Arithmetic
C. Data transfer
D. Floating point

**Question No:15 (Marks:1) Vu-Topper RM**
In a register-based machine having 64 registers, a _____ field is required in instruction to identify a register.
**A. 6 bits Page 22**
B. 16 bits
C. 32 bits
D. 64 bits

**Question No:16 (Marks:1) Vu-Topper RM**
What is the instruction length of the FALCON-E processor?
A. 6 bits
B. 16 bits
**C. 32 bits**
D. 64 bits

**Question No:17** **(Marks:1)** **Vu-Topper RM**

Which one of the following is a bi-stable device, capable of storing one bit of Information?

A. Diplexer
B. Decoder
**C. Flip-flop** **Page 76**
D. Multiplexer

**Question No:18** **(Marks:1)** **Vu-Topper RM**

The SPARC architecture defines a _____ that allows for multiple address spaces.

A. Memory Logic Unit (MLU)
**B. Memory Shifting Unit (MSU)**
C. Memory Mapping Unit (MMU)
D. Memory Arithmetic Unit (MAU)

**Question No:19** **(Marks:1)** **Vu-Topper RM**

Motorola MC68000 is an example of _____ microprocessor.

A. SRC
B. RISC
**C. CISC** **Page 150**
D. FALCON

**Question No:20** **(Marks:1)** **Vu-Topper RM**

In Type C instruction of SRC, the maximum size of constant field is _____ bits.

A. 22
**B. 17**
C. 21
D. 16

**Question No:21** **(Marks:1)** **Vu-Topper RM**

Which of the following is NOT an advantage of using register-to-register data transfers?

A. It is faster

**B. It is simpler** **Page 35**

C. It is most compact

D. It is easier to pipeline

**Question No:22** **(Marks:1)** **Vu-Topper RM**

Which of the instruction is used to load register from memory using a relative address?

A. ld instruction

B. str instruction

C. lar instruction

**D. ldr instruction** **Page 47**

**Question No:23** **(Marks:1)** **Vu-Topper RM**

In "Jump [8]" instruction, the size of the constant field is _____ bits.

**A. 8**

B. 16

C. 32

D. 64

**Question No:24** **(Marks:1)** **Vu-Topper RM**

A collection of all possible machine language commands that a computer can understand and execute is called _____.

A. Opcodes

B. Bytecodes

C. Mnemonics

**D. Instruction Set** **Page 23**

**Question No:25** **(Marks:1)** **Vu-Topper RM**

In a simple RISC computer, the size of each register is _____.

**A. 32 bits**

B. 16 bits

C. 24 bits

D. 64 bits

**Question No:26** **(Marks:1)** **Vu-Topper RM**

Which of the following is NOT related to the architecture of a computer?

A. Instruction set

**B. Control signals**

C. I/O mechanisms

D. Memory addressing modes

**Question No:27** **(Marks:1)** **Vu-Topper RM**

The instruction "Load R1, [R3 + 20]" is an example of which of the following addressing modes?

A. Direct

**B. Register**

C. Immediate

D. Displacement

**Question No:28** **(Marks:1)** **Vu-Topper RM**

In SRC, the effective address is computed at run-time by adding a constant to value of _____ register .

**A. PC**

B. IP

C. RA

D. Flags

**Question No:29** **(Marks:1)** **Vu-Topper RM**

The syntax of the instruction 'branch and link if zero' is

**A. brlzr ra, rb, rc** **Page 170**

B. brzr ra, rb, rc

C. brnz ra, rb, rc
D. brinz ra, rb, rc

**Question No:30** **(Marks:1)** **Vu-Topper RM**
The_____ control signal enables the input to the register C for writing the incremented value of PC onto it.
**A. LC** **Page 159**
B. LPC
C. INC4
D. PCout

**Question No:31** **(Marks:1)** **Vu-Topper RM**
Which one of the following register holds the instruction that is being executed?
A. Accumulator
B. Address Mask
C. Program Counter
**D. Instruction Register** **Page 152**

**Question No:32** **(Marks:1)** **Vu-Topper RM**
_____ is defined as the number of instructions processed per second.
A. Latency
**B. Throughput** **Page 187**
C. ALU operation
D. Memory access

**Question No:33** **(Marks:1)** **Vu-Topper RM**
In pipe-lined processor, there should be a_____ port register file so that if the register write and register read stages overlap they can be performed in parallel.
A. Four
B. Two
C. One

**D. Three** **Page 188**

**Question No:34** **(Marks:1)** **Vu-Topper RM**

_____ is a register which takes input from the ALSU as memory address to be accessed and transfer the memory contents on that location onto the memory sub-system.

A. PC
B. IR
**C. MAR** **Page 140**
D. MBR

**Question No:35** **(Marks:1)** **Vu-Topper RM**

"Finite-state machine" concepts are usually used to represent the control unit where every state corresponds to_____ clock cycles(s).

**A. 1** **Page 172**
B. 2
C. 4
D. 16

**Question No:36** **(Marks:1)** **Vu-Topper RM**

_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

A. LC
B. LPC
C. INC4
**D. PCout** **Page 159**

**Question No:37** **(Marks:1)** **Vu-Topper RM**

Which one of the following control signals causes the data from the bus to be read into the register MAR.

A. MARout
B. MARin
**C. LMAR** **Page 154**

D. None of the given

**Question No:38 (Marks:1) Vu-Topper RM**

_____ operation is required to change the processor‟s state to a known, defined value.

A. Change
**B. Reset Page 208**
C. Update
D. None of the given

**Question No:39 (Marks:1) Vu-Topper RM**

There are _____ types of reset operations in SRC

**A. Two Page 195**
B. Four
C. Five
D. Three

**Question No:40 (Marks:1) Vu-Topper RM**

Which one of the following registers stores a previously calculated value or a value loaded from the main memory?

**A. Accumulator**
B. Address Mask
C. Program Counter
D. Instruction Register

**Question No:41 (Marks:1) Vu-Topper RM**

In CPU design,_____ creates or forms the interface between the data path and control unit.

A. ALU
B. Cache
C. Buses
**D. Control signal Page 153**

**Question No:42** **(Marks:1)** **Vu-Topper RM**

_____ is defined as the time required to process a single instruction.

**A. Latency** **Page 217**

B. Throughput

C. ALU operation

D. Memory access

**Question No:43** **(Marks:1)** **Vu-Topper RM**

Upon receiving the_____ signals, the SRC should perform a hard reset.

A. Rst

B. Con

**C. Strt** **Page 209**

D. Stop

**Question No:44** **(Marks:1)** **Vu-Topper RM**

The MAR is connected directly to the_____

A. LIC

B. MBR

**C. CPU Internal bus** **Page 186+187**

D. CPU external bus

**Question No:45** **(Marks:1)** **Vu-Topper RM**

In the case of a constant, variable, an address or (label-PC) the jump ranges_____

A. From-64 to 63

**B. From -128 to 127** **Page 171**

C. From -256 to 255

D. From -32768 to 32767

**Question No:46** **(Marks:1)** **Vu-Topper RM**

In MC68000,_____register is used as stack pointer:

A. A0

**B. A7**

C. D0

D. D7

**Question No:47** **(Marks:1)** **Vu-Topper RM**

During the RESET operation of processor, control step counter is set to_____

A. 1

**B. 0** **Page 115**

C. 2

D. -1

**Question No:48** **(Marks:1)** **Vu-Topper RM**

In a processor, _____is responsible for the synchronization of internal as well external events.

A. Data Unit

**B. Control Unit** **Page 198**

C. Memory Unit

D. Arithmetic & Logic Unit

**Question No:49** **(Marks:1)** **Vu-Topper RM**

CISC Stands for?

A. Complex internal system computer

B. Computer instruction set compiler

C. Complex instruction system compiler

**D. Complex Instruction Set Computers** **Page 10**

**Question No:50** **(Marks:1)** **Vu-Topper RM**

SPARC uses a simple set of_____instruction format.

A. 64-bit

B. 12-bit

C. 16-bit

**D. 32-bit**

**Question No:51** **(Marks:1)** **Vu-Topper RM**

Which of the following register(s) is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

A. Registers A and C
B. Instruction Register
C. Memory Buffer Register
**D. Memory address register** **Page 152**

**Question No:52** **(Marks:1)** **Vu-Topper RM**

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC _____wide.

A. 8-bits
B. 16-bits
**C. 32-bits** **Page 157**
D. 64-bits

**Question No:53** **(Marks:1)** **Vu-Topper RM**

For any of the instructions that are a part of the instruction set of the SRC, there are cerain_____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

A. Register
**B. Control signals** **Page 171**
C. Memory
D. None of the given

**Question No:54** **(Marks:1)** **Vu-Topper RM**

What is the instruction length of the FALCON-A processor?

A. 8-bits
**B. 16-bits** **Page 134**
C. 32-bits
D. 64-bits

**Question No:55** **(Marks:1)** **Vu-Topper RM**

_____control signals enable the input to the PC for receiving a value that is currently on the internal processor bus.

**A. LPC** **Page 172**

B. INC4

C. LC

D. I

**Question No:56** **(Marks:1)** **Vu-Topper RM**

Which instruction is used to store register to memory using relative address?

A. ld instruction

B. ldr instruction

C. lar instruction

**D. str instruction** **Page 48**

**Question No:57** **(Marks:1)** **Vu-Topper RM**

The instruction _____ will load the register R3 with the contenets of the m\emory location M [PC+56]

A. Add R3, 56

B. lar R3, 56

**C. ldr R3, 56** **Page 56**

D. str R3, 56

**Question No:58** **(Marks:1)** **Vu-Topper RM**

Which one of the following registers holds the address of the next instruction to be executed?

A. Accumulator

B. Address Mask

C. Instruction Register

**D. Program Counter** **Page 151**

**Question No:59** **(Marks:1)** **Vu-Topper RM**

Which one of the following is the memory organization of EAGLE processor?

**A. 8-bits** **Page 112**

B. 16-bits

C. 32-bit

D. 64-bits

**Question No:60** **(Marks:1)** **Vu-Topper RM**

Type A of SRC has which of the following instructions? A) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction

A. & (b)

B. (b) & (c)

C. & (e)

**D. (b) & (e)** **Page 47**

**Question No:61** **(Marks:1)** **Vu-Topper RM**

What is the instruction length of the SRC processor?

A. 8 bits

B. 16 bits

**C. 32 bits** **Page 134**

D. 64 bits

**Question No:62** **(Marks:1)** **Vu-Topper RM**

Which one of the following is the memory organization of FALCON-E processor?

A. 28 * 8 bits

B. 216 * 8 bits

**C. 232 * 8 bits** **Page 124**

D. 264 * 8 bits

**Question No:63** **(Marks:1)** **Vu-Topper RM**

----------are faster than cache memory

**A. CPU registers** **Page 33**

B. I/O devices
C. ROM
D. Accumulator register

**Question No:64** **(Marks:1)** **Vu-Topper RM**

P: R3 ¬ R5 MAR ¬ IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

A. Arrow ¬
B. Colon :
**C. Comma , Page 69**
D. Parentheses ()

**Question No:65** **(Marks:1)** **Vu-Topper RM**

Prefetching can be considered a primitive form of----------

A. Multi-processing
B. Self-execution
C. Exception
**D. Pipelining Page 42**

**Question No:66** **(Marks:1)** **Vu-Topper RM**

Which one of the following circuit design levels is called the gate level?

A. Circuit Level
B. Mask Level
C. None of the given
**D. Logic Design Level Page 22**

**Question No:67** **(Marks:1)** **Vu-Topper RM**

_____ controller controls the sequence of the flow of microinstructions.

A. Multiplexer
**B. Microprogram** **Page 225**
C. ALU
D. None of the given

**Question No:68** **(Marks:1)** **Vu-Topper RM**
The code size of 2-address instruction is _____.
A. 5 bytes
**B. 7 bytes** **Page 36**
C. 3 bytes
D. 2 bytes

**Question No:69** **(Marks:1)** **Vu-Topper RM**
Register-register instructions use _____ memory operands out of a total of 3 operands
A. 1
B. 3
**C. 0** **Page 37**
D. 2

**Question No:70** **(Marks:1)** **Vu-Topper RM**
Flip-flop is a _____device, capable of storing one bit of Information
**A. Bi-stable** **Page 76**
B. Unit-stable
C. Stable
D. Storage

**Question No:71** **(Marks:1)** **Vu-Topper RM**
Execution time of a program with respect to the processor is calculated as:
A. Execution Time = IC x CPI x MIPS

**B. Execution Time = IC x CPI x T** **Page 254**

C. Execution Time = CPI x T x MFLOPS

D. Execution Time = IC x T

**Question No:72** **(Marks:1)** **Vu-Topper RM**

An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------

A. compiler

**B. cross assembler** **Page 26**

C. debugger

D. linker

**Question No:73** **(Marks:1)** **Vu-Topper RM**

What functionality is performed by the instruction "lar R3, 36" of SRC?

A. It will load the register R3 with the contents of the memory location M [PC+36]

**B. It will load the register R3 with the relative address itself (PC+36). Page 48**

C. It will store the register R3 contents to the memory location M [PC+36]

D. No operation

**Question No:74** **(Marks:1)** **Vu-Topper RM**

Which operator is used to „name" registers, or part of registers, in the Register Transfer Language?

**A. :=** **Page 66**

B. &

C. %

D. ©

**Question No:75** **(Marks:1)** **Vu-Topper RM**

What is the working of Processor Status Word (PSW)?

**A. To hold the current status of the processor.** **Page 28**

B. To hold the address of the current process

C. To hold the instruction that the computer is currently processing

D. To hold the address of the next instruction in memory that is to be executed

**Question No:76** **(Marks:1)** **Vu-Topper RM**

Almost every commercial computer has its own particular _____ language.

A. 3GL

B. English language

C. Higher level language

**D. assembly language** **Page 25**

**Question No:77** **(Marks:1)** **Vu-Topper RM**

In which of the following instructions, the data moves between a register in the processor and a memory location?

A. Arithmetic/logic

**B. Load/store** **Page 141**

C. Test/branch

D. None of the given

**Question No:78** **(Marks:1)** **Vu-Topper RM**

What functionality is performed by the instruction "str R8, 34" of SRC?

A. It will load the register R8 with the contents of the memory location M [PC+34]

B. It will load the register R8 with the relative address itself (PC+34).

**C. It will store the register R8 contents to the memory location M [PC+34]** **Page 48**

D. No operation



بری صحبت سے تنہائی بہتر ہے اور تنہائی سے نیک صحبت بہتر ہے

**Question No:79** **(Marks:1)** **Vu-Topper RM**

What does the instruction "ldr R3, 58" of SRC do?

**A. It will load the register R3 with the contents of the memory location M [PC+58] Page 47**

B. It will load the register R3 with the relative address itself (PC+58).

C. It will store the register R3 contents to the memory location M [PC+58]

D. No operation

**Question No:80** **(Marks:1)** **Vu-Topper RM**

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

**A. Processor-Memory-Switch level (PMS level) Page 22**

B. Instruction Set Level

C. Register Transfer Level

D. None of the given

**Question No:81** **(Marks:1)** **Vu-Topper RM**

What is the size of the memory space that is available to FALCON-A processor?

A. 2^8 bytes

**B. 2^16 bytes Page 90**

C. 2^32 bytes

D. 2^64 bytes

**Question No:82** **(Marks:1)** **Vu-Topper RM**

How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?

A. IR<16..0>

**B. IR<15..0> Page 105**

C. IR<16..1>

D. IR <15..1>

**Question No:83** **(Marks:1)** **Vu-Topper RM**

Which one of the following portions of an instruction represents the operation to be performed?

A. Address
B. Instruction code
C. Opcode
**D. Operand** **Page 134**

**Question No:84** **(Marks:1)** **Vu-Topper RM**

Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3

A. Opcode= R1, DR=ADD, SA=R2, SB=R3
**B. Opcode= ADD, DR=R1, SA=R2, SB=R3** **Page 34**
C. Opcode= R2, DR=ADD, SA=R1, SB=R3
D. Opcode= ADD, DR=R3, SA=R2, SB=R1

**Question No:85** **(Marks:1)** **Vu-Topper RM**

Which one of the following is the code size and the Number of memory bytes respectively for a 2-address instruction?

A. 4 bytes, 7 bytes
**B. 7 bytes, 16 bytes** **Page 36**
C. 10 bytes, 19 bytes
D. 13 bytes, 22 bytes

**Question No:86** **(Marks:1)** **Vu-Topper RM**

The external interface of FALCON-A consists of a _____ data bus.

A. 8-bit
**B. 16-bit** **Page 167**
C. 24-bit
D. 32-bit

**Question No:87** **(Marks:1)** **Vu-Topper RM**

The multiplexer----------is used to decide which value is transferred to be written back to the register file.

A. MP2
B. MP3
C. MP4
**D. MP5**

**Question No:88** **(Marks:1)** **Vu-Topper RM**

Which of the following condition is evaluated when executing the branch instruction "brzr R2, R1"?

A. If(R2==0)
B. If( R1 >0 )
**C. If( R1==0)**
D. If( R1 < 0)

**Question No:89** **(Marks:1)** **Vu-Topper RM**

In case of SRC processor, bits---------of IR (instruction register) are reserved for the opcode.

A. 0 to 4
B. 11 to 15
**C. 27 to 31**
D. 59 to 63

**Question No:90** **(Marks:1)** **Vu-Topper RM**

Which of the given RTL description is used to represent "load instruction register" (ldr) instruction?

A. (op=6): R[ra] rel
**B. (op=2): R[ra] M [rel]**
C. (op=2): M[disp] R [ra]
D. (op=2): M[rel] R [ra]

**Question No:91** **(Marks:1)** **Vu-Topper RM**

-------- Instruction is used to divide a register value by immediate value in FALCON-E processor.

A. div
B. idiv
**C. divi**
D. divim

**Question No:92** **(Marks:1)** **Vu-Topper RM**

Which field of machine language instruction is the “type of operation” that is to be performed.

**A. Op-code(or the operation code)**
B. CPU register
C. Memory Cells
D. I/O Location

**Question No:93** **(Marks:1)** **Vu-Topper RM**

Which of the following control signal is NOT activated during instruction fetch operation?

A. PCout
B. LC
**C. LMAR**
D. Cout

**Question No:94** **(Marks:1)** **Vu-Topper RM**

In case of FALCON-A---------- instruction are present which are not present in SRC processor.

A. create and destroy
**B. in and out**
C. open and close
D. read and write

**Question No:95** **(Marks:1)** **Vu-Topper RM**

---------- provides a temporary storage for the address of memory location to be accessed.

**A. MAR**
B. MBR
C. PC
D. LPC

**Question No:96** **(Marks:1)** **Vu-Topper RM**

Which of the following register is used to enable the tri-stable buffers with the MBR?

**A. MBRout**
B. MARout
C. LMBR
D. INC4

**Question No:97** **(Marks:1)** **Vu-Topper RM**

mul is the example of a(n)---------- operation.

A. Logic
B. Shift
**C. Arithmetic**
D. Data transfer

**Question No:98** **(Marks:1)** **Vu-Topper RM**

Control Signal for RTL "IR< ---MBR" will be---------

**A. MBRout,LIR**
B. PC< --C
C. PC< --MBR
D. PC< --IR

**Question No:99** **(Marks:1)** **Vu-Topper RM**

The status register of the 68000 has -------- condition codes.

A. 2
B. 3

**C. 5**
D. 8

**Question No:100** **(Marks:1)** **Vu-Topper RM**
In ---------- instruction format of EAGLE processor, there is no field reserved for the operands.
A. Type V
B. Type Y
C. Type X
**D. Type Z**

**Question No:101** **(Marks:1)** **Vu-Topper RM**
A general purpose digital computer has --------- main components.
A. 2
B. 3
**C. 4**
D. 5

**Question No:102** **(Marks:1)** **Vu-Topper RM**
The instruction ---------- will load the register R3 with the contents of the memory location M[PC+56].
A. lar R3,M[56]
B. ldr R3,M[56]
**C. ldr R3,56**
D. lr R3,[56]

**Question No:103** **(Marks:1)** **Vu-Topper RM**
In FALCON-A instruction format of Type-2 constants and variable should be in the range of.
A. -132 to +131
B. -164 to + 163

C. -32 to + 31
**D. -128 to + 127**

**Question No:104** **(Marks:1)** **Vu-Topper RM**
In a FALCON-A assembly program, labels are used to implement-------- jump.
A. Direct
B. Indirect
**C. Relative**
D. Displacement

**Question No:105** **(Marks:1)** **Vu-Topper RM**
In "Jump [8]" instruction, the size of the constant fields is -------- bits.
A. 4
B. 5
**C. 8**
D. 16

**Question No:106** **(Marks:1)** **Vu-Topper RM**
Which of the following registers is used as an implicit operand in MUL/DIV instruction of FALCON-A?
**A. R0**
B. PC
C. IR
D. SP

**Question No:107** **(Marks:1)** **Vu-Topper RM**
To set the value of micro-PC from branch address, the value of 4 to 1 multiplexer is----------
A. 00
B. 01

C. 10
**D. 11**

**Question No:108 (Marks:1) Vu-Topper RM**
The instruction "PUSH A" is an example of ----------
**A. 0-address instruction**
B. 1-address instruction
C. 2-address instruction
D. 3-address instruction

**Question No:109 (Marks:1) Vu-Topper RM**
Which of the following branch instruction has a condition which is always executed?
A. JZ
**B. JUMP**
C. JPL
D. JMI

**Question No:110 (Marks:1) Vu-Topper RM**
---------- hazard occurs when attempting to access same resource in different ways at the same time.
A. Branch
B. Data
**C. Structural**
D. Instruction

**Question No:111 (Marks:1) Vu-Topper RM**
_____ is an example of Miscellaneous instruction.
A. Shift
B. Store
C. **Halt**

D. Call

**Question No:112** **(Marks:1)** **Vu-Topper RM**

Which type of instructions enables mathematical computations?

**A. Arithmetic**
B. Control
C. Data transfer
D. Numeric

**Question No:113** **(Marks:1)** **Vu-Topper RM**

VLIW Stands for----------

A. Variable Length Instruction Word
**B. Very Long Instruction Word**
C. Very Long Instruction Width
D. Variable Length Instruction Width

**Question No:114** **(Marks:1)** **Vu-Topper RM**

In SRC, the general-purpose register file includes---------- registers, each 32 bit wide.

A. 6 Registers R0 to R15
B. 24 Registers R0 to R23
**C. 32 Registers R0 to R31**
D. 64 Registers R0 to R63

**Question No:115** **(Marks:1)** **Vu-Topper RM**

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?

A. Jump and branch format instructions
B. Immediate format instructions
**C. Register format instructions**
D. All of the above

**Question No:116** **(Marks:1)** **Vu-Topper RM**

What does the word 'D' in the 'D-flip-Flop' stands for?

A. Data

**B. Digital**

C. Dynamic

D. Double

**Question No:117** **(Marks:1)** **Vu-Topper RM**

The instruction _____ will load the register R3 with the contents of the memory location M [PC+56]

A. Add R3, 56

B. lar R3, 56

**C. ldr R3, 56**

D. str R3, 56

**Question No:118** **(Marks:1)** **Vu-Topper RM**

Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?

A. Base address

B. Binary address

**C. Effective address**

D. All of the given

**Question No:119** **(Marks:1)** **Vu-Topper RM**

Which of the following statements is/are true about RISC processors' claimed advantages over CISC processors? (a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution. (b) RISC CPUs outperform CISC CPU's in procedural programming environments. (c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction. (d) It is easier to maintain the "family concept" in RISC CPU.

A. (a), (b) &(c)

B. (b), (c) & (e)
C. (c), (d) & (e)
**D. (a), (c) & (d)**

**Question No:120 (Marks:1) Vu-Topper RM**
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimize
**A. Perfecting**
B. Pipelining
C. Superscalar operation
D. Speedup

**Question No:121 (Marks:1) Vu-Topper RM**
The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------
**A. Exception**
B. Function
C. Thread
D. Stack

**Question No:122 (Marks:1) Vu-Topper RM**
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
A. Backward compatibility
B. Data migration
C. Reverse engineering
**D. Upward compatibility**

**Question No:123 (Marks:1) Vu-Topper RM**
Computer system performance is usually measured by the ----------
A. Time to execute a program or program mix
B. The speed with which it executes programs

C. Processor's utilization in solving the problems

**D. Instructions that can be carried out simultaneously**

**Question No:124** **(Marks:1)** **Vu-Topper RM**

The external interface of FALCON-A consists of a _____address bus and a _____ data bus.

A. 8-bit , 8-bit

**B. 16-bit , 16-bit**

C. 16-bit , 24-bit

D. 16-bit , 32-bit

**Question No:125** **(Marks:1)** **Vu-Topper RM**

Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?

A. Instruction Register

**B. Memory address register**

C. Memory Buffer Register

D. Registers A and C

**Question No:126** **(Marks:1)** **Vu-Topper RM**

Among the two approaches available to design a control unit, hardware approach is relatively---------- as compared to micro-programming.

A. Slow

**B. Fast**

C. Average

D. Better

**Question No:127** **(Marks:1)** **Vu-Topper RM**

Which of the following is not a part of processor state?

A. IR

B. PC
C. Stacks
**D. Registers**

**Question No:128** **(Marks:1)** **Vu-Topper RM**
---------- form the branch control field in the micro instruction.
A. C Bits
B. M Bits
C. B BITS
**D. M Bits**

**Question No:129** **(Marks:1)** **Vu-Topper RM**
In FALCON-A ISA, which of the following opcodes is used to perform "No Operation"?
A. 20
**B. 21**
C. 22
D. 23

**Question No:130** **(Marks:1)** **Vu-Topper RM**
To apply two shifts to an input number using the barrel shifter, the control signals S1 and S0 of the shifter should be _____.
A. S1 = 1 and S0 = 1
B. S1 = 0 and S0 = 1
**C. S1 = 1 and S0 = 0**
D. S1 = 2 and S0 = 0

**Question No:131** **(Marks:1)** **Vu-Topper RM**
Which one of the following operations is NOT performed by using miscellaneous instructions?
A. Clearing all registers
B. Stopping the processor

**C. NOP**
D. Returning from a procedure

**Question No:132** **(Marks:1)** **Vu-Topper RM**
RISC stands for?
A. Registers internal system cache
**B. Reduced instruction set computer**
C. Registers instruction set computer
D. Reduced internal system computers

**Question No:133** **(Marks:1)** **Vu-Topper RM**
Which of the followings is not an example of super-scalar processors?
A. PowerPC601
**B. IAPX88**
C. Intel P6
D. DEC Alpha 21164

**Question No:134** **(Marks:1)** **Vu-Topper RM**
What does the instruction "idr R3, 58" of SRC do?
**A. It will load register R3 with the contents of the memory location M[PC+58]**
B. It will load register R3 with the relative address itself (PC+58)
C. It will store register R3 contents to the memory location M[PC+58]
D. It will store the value of register R3 at the relative address itself (PC+58)

**Question No:135** **(Marks:1)** **Vu-Topper RM**
For a processor having 32 general purpose registers, _____ bits are required for each register field in the instruction.
**A. 32**
B. 3
C. 8

D. 5

**Question No:136** **(Marks:1)** **Vu-Topper RM**

In SRC which of the following is a notation which is used to repeat 32-bit memory word stored at address starting from 56?

A. M[56]<31..0>:=M[56]M[57]M[58]M[59]
**B. M[56]<o..31>:=M[56]M[57]M[58]M[59]**
C. M[56]<0..31>:=M[59]M[58]M[57]M[56]
D. M[56]<0.31..>:=M[59]M[58]M[57]M[56]

**Question No:137** **(Marks:1)** **Vu-Topper RM**

Which of the following EAGLE instructions is used to initialize all the registers by setting them to 0?

A. NOP
B. HALT
**C. INIT**
D. RESET

**Question No:138** **(Marks:1)** **Vu-Topper RM**

The ALSU function "INC2" increments the ---------- by 2 and the output is stored in the buffer register

A. PC,A
B. IR,A
**C. PC,C**
D. IR,C

**Question No:139** **(Marks:1)** **Vu-Topper RM**

Which temporary register is loaded with either a register value from the register file or a constant from the instruction?

**A. Y3**
B. X3
C. Z4

D. Z5

**Question No:140** **(Marks:1)** **Vu-Topper RM**

_____ instruction is used to load a register with an immediate data value.

**A. La** **Page 46**

B. lar

C. ld

D. ldr

**Question No:141** **(Marks:1)** **Vu-Topper RM**

A computer belongs to which of the following subset of the systems?

A. Mechanical system

**B. Electrical system**

C. Optical system

D. Magnetic system

**Question No:142** **(Marks:1)** **Vu-Topper RM**

Which of the following code size and the number of memory bytes respectively for a 2-address instruction.

A. 4 bytes, 7 bytes

**B. 7 bytes ,16 bytes**

C. 10 bytes , 19 bytes

D. 13 bytes, 19 bytes

**Question No:143** **(Marks:1)** **Vu-Topper RM**

Which of the the given below measures is/are used for comparison of performance of various machine?

A. Execution time

B. MFLOPS

C. MIPS

**D. All of the given**

**Question No:144** **(Marks:1)** **Vu-Topper RM**

There are ---------- type of RESET operation in SRC.

A. Three
B. Four
**C. Two**
D. five

**Question No:145** **(Marks:1)** **Vu-Topper RM**

Type checking allows the _____ to determine memory requirements for variables.

**A. Compiler** **Page 25**
B. Debugger
C. Linker
D. loader

**Question No:146** **(Marks:1)** **Vu-Topper RM**

In FALCON-A processor, memory word size is----------

A. 1 byte
**B. 4 bytes**
C. 8 bytes
D. 2 bytes

**Question No:147** **(Marks:1)** **Vu-Topper RM**

To connect together five (5) m-bit registers in a point-to-point scheme, _____ connections are required.

A. 25
B. 30
**C. 20**
D. 24

**Question No:148** **(Marks:1)** **Vu-Topper RM**

What does the instruction"ldr R3, 58" of SRC do?

A. It will load the register R3 with the contents of the memory location M[PC+58]

**B. It will load the register R3 with the relative address itself(PC+58)**

C. It will store register R3 contents to the memory location M[PC+58]

D. It will store the value of register R3 at the relative address itself(PC+58)

**Question No:149** **(Marks:1)** **Vu-Topper RM**

Which of the following operations is NOT performed by using miscellaneous instruction?

A. Clearing all registers

B. Stopping the processor

C. NOP

**D. Returning from a procedure**

**Question No:150** **(Marks:1)** **Vu-Topper RM**

Which of the following RTL description is used for specifying the operation of an SRC instruction?

A. IR<31..27>

**B. IR<22..26>**

C. IR<21..17>

D. IR<21..0>

**Question No:151** **(Marks:1)** **Vu-Topper RM**

Which one of the following registers holds the instruction that is being executed?

A. Accumulator

B. Address Mask

**C. Instruction Register**

D. Program Counter

**Question No:152** **(Marks:1)** **Vu-Topper RM**
which it was originally developed.

A. Backward compatibility
**B. Data migration**
C. Reverse engineering
D. Upward compatibility

**Question No:153** **(Marks:1)** **Vu-Topper RM**
Which of the given RTL description is used to represent store register relative (str) instruction?
**(op<4..0>=4):M[rel]<-R[ra]**

**Question No:154** **(Marks:1)** **Vu-Topper RM**
Which of the given RTL description is used to represent load displacement address (Ia) instruction?
**(op<4..0>=5):R[ra]<-disp**

**Question No:155** **(Marks:1)** **Vu-Topper RM**
Which of the given RTL description is used to represent load relative address (Iar) instruction?
**(op<4..0=6):R[ra]<-rel**

**Question No:156** **(Marks:1)** **Vu-Topper RM**
Which of the given RTL description is used to represent conditional branch (br) instruction?
**(op<4..0>=8): (cond : PC<- R[rb]),**

**Question No:157** **(Marks:1)** **Vu-Topper RM**
Which of the given RTL description is used to represent branch and bank (brl) instruction?
**Cond : (PC <- R [rb]))**

**Question No:158** **(Marks:1)** **Vu-Topper RM**

Which of the given RTL description is used to represent store register (st) instruction?
**(op<4..0>=3):M[disp]<-R[ra]**

**Question No:159** **(Marks:1)** **Vu-Topper RM**
Which of the given RTL description is used to represent load register relative (Idr) instruction?
**(op<4..0>=2) : R[ra] <- M[rel]**

**Question No:160** **(Marks:1)** **Vu-Topper RM**
Which of the given RTL description is used to represent load register (Id) instruction?
**(op<4.00>=1):R[ra]<-M[disp]**

**Question No:161** **(Marks:1)** **Vu-Topper RM**
In a simple RISC computer the size of each register is _____.
**32 bits**

**Question No:162** **(Marks:1)** **Vu-Topper RM**
A _____ is a device that provides a shared data path to a number of devices that are connected to it.
**Bus**

**Question No:163** **(Marks:1)** **Vu-Topper RM**
_____ instruction is used to store register contents to memory
**St**

**Question No:164** **(Marks:1)** **Vu-Topper RM**
Which type of instructions load data from memory into register or store data from register into memory and transfer into memory and transfer data between different kinds of special-purpose registers?
**Data transfer**

**Question No:165** **(Marks:1)** **Vu-Topper RM**
A stack based machine is also called _____.
**0-address machine**

**Question No:166** **(Marks:1)** **Vu-Topper RM**
Which of the following bits of SRC instruction are used to hold the instruction register, used to hold the current instruction
**The bits 31 through 0**

**Question No:167** **(Marks:1)** **Vu-Topper RM**
Which of the following bits of SRC instruction are used to hold program counter(it holds the memory address of next instruction to be executed)?]
**The bits 31 through 0**

**Question No:168** **(Marks:1)** **Vu-Topper RM**
Which of the following bits of SRC instruction are used to hold short displacement or immediate field?
**The bits 16 through 0**

**Question No:169** **(Marks:1)** **Vu-Topper RM**
Which of the following bits of SRC instruction are used to hold count or modifier field?
**The bits 16 through 0**

**Question No:170** **(Marks:1)** **Vu-Topper RM**
Which of the following bits of SRC instruction are used to hold a second operand, conditional test, or a shift count register?
**The bits 16 through 12**

**Question No:171** **(Marks:1)** **Vu-Topper RM**
Which of the following bits of SRC instruction are used to hold long displacement field?

**The bits 21 thorugh 0**

**Question No:172** **(Marks:1)** **Vu-Topper RM**
Which of the following is example of direct indirect addressing mode?
A. M[R6]
B. M[R5]
C. M[R1+25]
**D. M[[R5] + [R6]]**

**Question No:173** **(Marks:1)** **Vu-Topper RM**
Which of the following RTL description is used to represent the target register of Falcon-A instruction
**Ra<2..0>:=IR<10..8>**

**Question No:174** **(Marks:1)** **Vu-Topper RM**
Which of the following RTL description is used to represent the operation code of Falcon-A instruction
**Op<4..0>:= IR<15..11>:**

**Question No:175** **(Marks:1)** **Vu-Topper RM**
Which of the following RTL description is used to represent the operand or address index of Falcon-A instruction
**Rb<2..0>:=IR<7..5>:**

**Question No:176** **(Marks:1)** **Vu-Topper RM**
Which of the following RTL description is used to represent the second operand of Falcon-A instruction
**Rc<2..0>:=IR<4.2>**

**Question No:177** **(Marks:1)** **Vu-Topper RM**

Which of the following RTL description is used to represent the short displacement field of Falcon-A instruction

**C1<4..0>:=IR<4..0>**

**Question No:178** **(Marks:1)** **Vu-Topper RM**

Which of the following RTL description is used to represent the long displacement or the immediate field of Falcon-A instruction

**C2<7..0>:=IR<7..0>:**

**Question No:179** **(Marks:1)** **Vu-Topper RM**

The instruction Load R1, [R3 + 20] is an example of which of the following addressing modes?

**Register**

**Question No:180** **(Marks:1)** **Vu-Topper RM**

In SRC, the op-code for NOP operation is _____.

**0**

**Question No:181** **(Marks:1)** **Vu-Topper RM**

Which of the following RTL description is used to represent all general purpose register of SRC?

**R[0..31]<31..0>;**

**Question No:182** **(Marks:1)** **Vu-Topper RM**

_____ instruction is used to push the contents of a specified general purpose register to the stack in FALCON-E processor

**Push**

**Question No:183** **(Marks:1)** **Vu-Topper RM**

_____ instruction is used to pop the value that is at the top of the stack in FALCON-E processor

**Pop**

**Question No:184** **(Marks:1)** **Vu-Topper RM**

_____ instruction is used to branch if source operand is less than target address in FALCON-E processor

**Bl**

**Question No:185** **(Marks:1)** **Vu-Topper RM**

_____ instruction is used to branch if source operand is greater than target address in FALCON-E processor

**Bg**

**Question No:186** **(Marks:1)** **Vu-Topper RM**

_____ instruction is used to multiply an immediate value with a value stored in a register in FALCON-E processor

**Muli**

**Question No:187** **(Marks:1)** **Vu-Topper RM**

_____ instruction is used to evaluate logical exclusive or in FALCON-E processor

**Xor, xori**

**Question No:188** **(Marks:1)** **Vu-Topper RM**

Which of the following measure can be best used for calculating the performance of computation intensive application

**MFLOPS**

**Question No:189** **(Marks:1)** **Vu-Topper RM**

All of the below given processors employ Little-Endian storage format except_____.

A. EAGLE

**B. Falcon-A**

C. Falcon-E

D. Modified EAGLE

**Question No:190** **(Marks:1)** **Vu-Topper RM**

he instruction shifti R1, R2, 20 is an example of which of the following addressing modes?

**Immediate**

**Question No:191 (Marks:1) Vu-Topper RM**

All of the given are examples of register-to-memory data transfer instructions except _____.

**A. Id**

B. St

C. Lar

D. idacc

**Question No:192 (Marks:1) Vu-Topper RM**

Which of the given techniques is used for overlapping the multiple instructions at one time?

**Piping**

**Question No:193 (Marks:1) Vu-Topper RM**

A relative address is calculated by adding the displacement to the contents of the _____.

A. Flags Register

**B. Program Counter**

C. Instruction Register

D. General Purpose Register

**Question No:194 (Marks:1) Vu-Topper RM**

In MC68000, only the last _____ bits of 32-bit program counter (PC) register are used to store memory addresses.

**The last 24 bits of the 32-bit Program**

**Question No:195 (Marks:1) Vu-Topper RM**

15. In RTL, which of the following symbols is used to store some data into a register?

A. <-

B. ;
**C. :=**
D. = =

**Question No:196** **(Marks:1)** **Vu-Topper RM**
An _____ is a program that takes basic computer instructions and converts them into a pattern of bits that the computer's processor can use to perform its basic operations.
**Assembler**

**Question No:197** **(Marks:1)** **Vu-Topper RM**
In this figure, the constant value specified by the immediate field is added to the register value, and the resultant is the index of memory location that is referred i.e. Effective Address = A + (content of R) . Identify the addressing mode.
**Displacement**

**Question No:198** **(Marks:1)** **Vu-Topper RM**
In _____ address mode, the actual data is stored in the instruction.
A. Direct
B. Indirect
C. Relative
**D. Immediate**

**Question No:199** **(Marks:1)** **Vu-Topper RM**
Which one of the following registers store a previously calculated value or a value loaded from the main memory?
**Accumulator**

**Question No:200** **(Marks:1)** **Vu-Topper RM**
An instruction that specifies one operand in memory and one operand in a register would be known as a _____ address instruction.
**1-1/2**

**Question No:201** **(Marks:1)** **Vu-Topper RM**
Which one of the following instructions is used to load register from memory using a relative address?
**ldr**

**Question No:202** **(Marks:1)** **Vu-Topper RM**
Which one of the following is an address (binary bit pattern) issued by CPU?
**Effective**

**Question No:203** **(Marks:1)** **Vu-Topper RM**
Which one of the following languages presents a simple, human-oriented language to specify the operations, register communication and timing of the steps that take place within a CPU to carry out higher level (user programmable) instructions?
**RTL (Register Transfer Language)**

**Question No:204** **(Marks:1)** **Vu-Topper RM**
What does the RTL expression [M(1234)] means?
**The contents of memory whose address is 1234.**

**Question No:205** **(Marks:1)** **Vu-Topper RM**
Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?
**Data transfer**

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