



CS-501 Advanced Computer Architecture Update MCQS For Quiz-3 File Solve By Vu Topper RM



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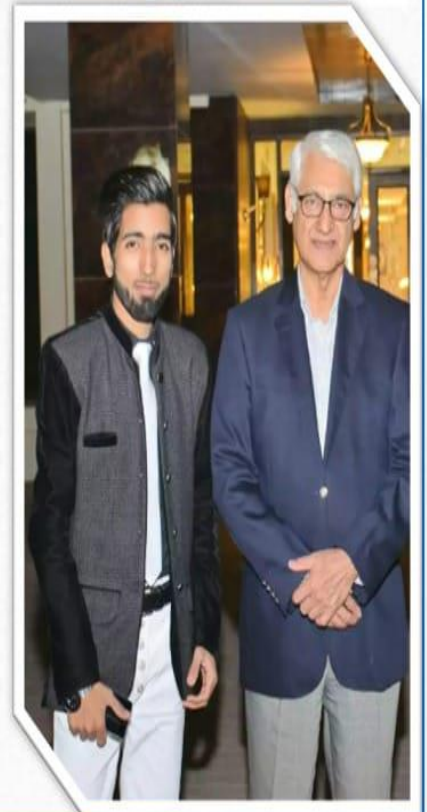
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_____ form the control signal field in the micro instruction.

- A. A bits
- B. B bits
- C. C bits**
- D. D bits

Page 206

A combination of parallel and sequential hardware used to build a multiplier is known as _____

- A. Booth Recording
- B. Parallel Array Multiplier
- C. Series Parallel Multiplier**
- D. None of the these

Page 379

The cache contains a copy of portions of the _____.

- A. ROM
- B. EPROM
- C. Flash Memory
- D. Main memory**

Page 398

When _____ signal is high, this would correspond to a read operation equivalent to having an input data to the CPU and output from the memory.

- A. R/W**
- B. REQUEST
- C. COMPLETE
- D. None of the given

Page 316

Every interrupt handler has an interrupt return (IRET) instruction, this instruction is an example of _____ return.

- A. FAR**
- B. NEAR
- C. SHORT
- D. RELATIVE

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In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?

- A. Daisy chain
- B. Software poll**
- C. Multiple interrupt lines
- D. All of given option

_____ are computed by the ALU and stored in processor status register.

- A. Condition codes** **Page 382**
- B. Fraction Division
- C. Conditional Branches
- D. None of the given

Raid Level _____ is not a true member of the RAID family.

- A. 0** **Page 365**
- B. 1
- C. 2
- D. 3

A very large page size results in increased _____.

- A. Delay
- B. Through put
- C. Access time** **Page 441**
- D. Execution time

Every time you press a key, an interrupt is generated.

- A. Software interrupt
- B. Hardware interrupt** **Page 275**
- C. None of the given
- D. All of the given

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What is the status of the ACKNLG# signal when a character is completely received by the printer?

- A. It toggles its state
- B. It remains unaffected
- C. It goes from low to high
- D. It goes from high to low**

Page 239

A _____ signal decides whether the input word should be shifted or bypassed.

- A. Shift/bypass**
- B. Control Read
- C. Control Write
- D. None of the given

Page 384

In virtual memory mechanism, pages are formulated in the _____ memory and brought into the _____ memory.

- A. Main, cache
- B. Main, secondary
- C. Secondary, main**
- D. Secondary, cache

Page 328

Along with information bits we add up another bit which is called the _____ bit.

- A. CRC
- B. Parity**
- C. Hamming
- D. Error Detection

Page 328

Select the parts of a hard disk.

- A. Header only
- B. Data section only
- C. Data section and a trailer
- D. Header, data section and a trailer**

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If a character is not available at the beginning of an interval, an _____ is said to occur.

- A. Parity Error
- B. Framing Error
- C. Overrun Error

D. Under-run Error **Page 262**

In which technique does the hardware directly access host memory for reading or writing independent of CPU?

- A. Polling
- B. Programmed I/O
- C. Interrupt driven I/O

D. Direct Memory Access (DMA)

Most parallel I/O ports used with peripheral devices are mapped on a range of _____.

- A. Cache
- B. Bus addresses
- C. Contiguous addresses
- D. Direct memory access

Page 287

How does DMA saves CPU time?

- A. By periodically polling
- B. By issuing a interrupt request to the CPU to request attention
- C. By storing all data in a buffer to be later transferred to the CPU

D. By controlling transfer between I/O devices and memory directly

_____ form the branch control field in the micro instruction.

- A. A bits
- B. B bits
- C. M bits
- D. D bits

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A parallel port can be considered to be a big _____ gate.

- A. OR
- B. AND**
- C. NOR
- D. NOT

_____ lets the user execute the program, one instruction at a time.

- A. Execute
- B. List File
- C. Change PC
- D. Single Step**

Page 7

For input ports, the incoming data should be placed on the data bus only during the I/O read bus cycle. For this purpose, are used.

- A. Flip Flops
- B. Registers
- C. AND Gates
- D. Tri-state Buffers**

At the start of the transfer operation in synchronous communication, the master activates the _____ signal.

- A. Data
- B. Read**
- C. Enable
- D. Acknowledge

The directive _____ is used to define variables.

- A. .db
- B. .exe
- C. .org
- D. .equ**

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----- is the time needed by the CPU to recognize (not service) an interrupt request.

- A. Throughput
- B. Timer delay

C. Interrupt Latency

Page 256

- D. Response Deadline

_____ hazard occurs when an instruction attempts to access some data value that has not yet been updated by the previous instruction.

A. Data

Page 198

- B. Branch
- C. Structural
- D. Instruction

In _____, a separate address space of the CPU is reserved for I/O operations.

- A. All of above

B. Isolated I/O

Page 217

- C. None of above
- D. Memory Mapped I/O

The Pentium does allow the use of some part of its _____ accumulator register EAX

- A. 8 bits
- B. 16 bits

C. 32 bits

Page 230

- D. 64 bits

A collection of -----is called a micro program.

- A. program memory
- B. control unit

C. both

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_____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.

- A. DISK
- B. Hazard
- C. Memory
- D. Computer Bus**

Where does the processor store the address of the first instruction of the ISR?

- A. Interrupt handler
- B. Interrupt request
- C. Interrupt vector**
- D. All of the given options

Page 277

_____ signal has input direction with respect to printer

- A. PE#
- B. BUSY
- C. ACKNLG#
- D. STROBE#**

Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.

- A. Parity error
- B. Overrun error
- C. Framing error
- D. Under-run error**

Page 240

_____ form the branch address field in the micro instruction.

- A. A bits
- B. B bits
- C. M bits**
- D. D bits

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_____ is/are example(s) of synchronous communication.

- A. All of the given
- B. Register to Memory
- C. Memory to Memory
- D. Register to Register**

ET = _____.

- A. $CPI \times IC / T$
- B. $CPI / IC \times T$
- C. $CP \times IC \times T$
- D. $CPI \times IC \times T$**

Page 118

To set the value of micro-PC from branch address, the value of 4 to 1 multiplexer is _____.

- A. 00
- B. 01
- C. 10
- D. 11**

Tri-state buffers are used for removing _____.

- A. bus collision
- B. bus contention**
- C. Instruction collision
- D. Instruction contention

Which of the following pins of processor is designated for maskable interrupts?

- A. MI
- B. NMI
- C. RINT
- D. INTR**

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Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?

- A. Virtual Memory** **Page 268**
- B. Programmed I/O
- C. Interrupt driven I/O
- D. Direct Memory Access (DMA)

Which is the last instruction of the ISR that is to be executed when the ISR terminates?

- A. INT
- B. IRQ
- C. NMI
- D. IRET** **Page 255**

In the little-endian format exchanging data between computers, the data transmitted by one will be received in a "swapped" form by the other.

- A. Signals
- B. Swapped** **Google**
- C. Arranged
- D. Organized

Identify the type of serial communication error condition in which "0" is received instead of a stop bit (which is always a "1")?

- A. Parity error
- B. Overrun error
- C. Framing error** **Page 240**
- D. Under-run error

_____ means that the CPU should input data from an input device only when the device is ready to provide data and send data to an output device only when it is ready to receive data.

- A. Data transfer
- B. Data location
- C. Data synchronization** **Page 218**

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D. Asynchronous transmission

The third stage of the Pipelined version of SRC is;

A. Register write

B. ALU operation Page 190

C. Memory access

D. Instruction Fetch

A _____ processor is based on a very long instruction word.

A. SRC

B. VLIW Page 202

C. FALCON-E

D. FALCON-A

In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?

A. Parallel

B. Asynchronous

C. Semi-synchronous

D. Daisy-Chaining Priority

_____ signal has Output direction with respect to printer

A. INIT#

B. D<7..0>

C. STROBE#

D. ACKNLG#

Interrupt driven I/O is better than _____.

A. Stall

B. Polling Page 259

C. First In First Out

D. Data Forwarding

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From an n bit control word we may have _____ bit signal values.

- A. $N \times n$
- B. n^2
- C. 2^n**
- D. $2 \times n$

Page 210

The source file of FALSIM should contain _____ text only.

- A. UFT
- B. ANSI
- C. ASCII**
- D. Unicode

Google

_____ usually involves calculating the target address and evaluating a condition.

- A. Pipelined SRC
- B. ALU instructions
- C. Branch Instructions**
- D. Load/Store instructions

Page 193

The SRC uses a hazard detection unit. The hazard can be resolved using either pipeline stalls or by _____.

- A. Data forwarding**
- B. Data compressing
- C. Instruction handling
- D. Instruction forwarding

Page 199

Connection to a CPU that provides a data path between the CPU and external devices, such as a keyboard, display, or reader is called-----

- A. Buses**
- B. Program
- C. Processor
- D. Memory address

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Which temporary register is loaded with either a register value from the register file or a constant from the instruction?

- A. Z4
- B. X3
- C. Y3**
- D. Z5

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Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?

- A. Parallel Priority**
- B. Asynchronous Priority
- C. Daisy-Chaining Priority
- D. Semi-synchronous Priority

VLIW stands for _____.

- A. Very Long Instruction Word
- B. Very Long Instruction Width
- C. Variable Length Instruction Width
- D. Variable Length Instruction Word**

Page 202

Which of the following is not True regarding serial communication?

- A. Slow
- B. High cost**
- C. Inefficient
- D. Easy to implement.

In a printer with DB-25 interface, _____ signal is better for edge triggered systems.

- A. PE#
- B. BUSY#
- C. STROB#
- D. ACKNLG#**

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Which of the followings is not an example of super-scalar processors?

- A. Intel P6
- B. IAPX88**
- C. PowerPC 601
- D. DEC Alpha 21164

A software routine performed when an interrupt is received by the computer is called as -----

- A. Trap
- B. Interrupt
- C. Exception
- D. Interrupt handler**

An interface that can be used to connect the microcomputer bus to _____ is called an I/O Port.

- A. Memory
 - B. Flip Flops
 - C. Multiplexers
 - D. Peripheral devices**
- Page 216**

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