Cs-501 Important Mcq's For Final Term
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Paid Tasks = LMS Handling + Online Classes + Project

Q 1 **For any of the instructions that are a part of the instruction set of the SRC, there are cerain_____required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.**

- Register
- **Control signals**
- Memory
- None of the given

Q 2 **FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC _____wide.**

- 8-bits
- 16-bits
- **32-bits**
- 64-bits

Q 3 **What is the instruction length of the FALCON-A processor**

- 8-bits
- **16-bits**
- 32-bits
- 64-bits

Q 4 **_____control signals enable the input to the PC for receiving a value that is currently on the internal processor bus.**

- **LPC**
- INC4
- LC
- I

Q 5 **Which one of the following is a bi-stable device, capable of storing one bit of information?**

- Decoder
- **Flip-Flop**
- Multiplexer
- Diplexer

Q 6 **Which instruction is used to store register to memory using relative address?**

- ld instruction
- ldr instruction
- lar instruction
- **str instruction**

Q 7 **Which field of the machine language instruction is the "type of operation" that is to be performed?**

- **Op-code (or the operation code)**
- CPU registers
- Momory cells
- I/O locations

Q 8 **The instruction _____ will load the register R3 with the contenets of the m\emory location M [PC+56]**

___Add R3, 56

___lar R3, 56

___ldr R3, 56

___str R3, 56

Q 9 **_____ operation is required to change the processor's state to a known, defined value.**

- Change
- **Reset**
- Update
- None of the given

Q 10 **which type of instructions help in changing the flow of the program as and when required?**

- Arithmetic
- **Control**
- Data transfer
- Floating point

- Question # 1 of 10 (Start time: 10:02:48 PM) Total Marks: 1
  What is the size of the memory space that is available to FALCON-A processor?
  Select correct option:

  2^8 bytes
  2^16 bytes
  2^32 bytes
  2^64 bytes
-
- Question # 2 of 10 (Start time: 10:03:58 PM) Total Marks: 1
  How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
  Select correct option:

  IR<16..0>
  IR<15..0>
  IR<16..1>
  IR<15..1>
-
- Question # 3 of 10 (Start time: 10:04:28 PM) Total Marks: 1
  What is the working of Processor Status Word (PSW)?
  Select correct option:

  To hold the current status of the processor.
  To hold the address of the current process
  To hold the instruction that the computer is currently processing
  To hold the address of the next instruction in memory that is to be executed
-
- Question # 4 of 10 (Start time: 10:05:10 PM) Total Marks: 1
  What does the instruction "ldr R3, 58" of SRC do?
  Select correct option:

  It will load the register R3 with the contents of the memory location M [PC+58]
  It will load the register R3 with the relative address itself (PC+58).
  It will store the register R3 contents to the memory location M [PC+58]
  No operation
-
- Question # 5 of 10 (Start time: 10:06:34 PM) Total Marks: 1
  What is the instruction length of the FALCON-E processor?
  Select correct option:

  8 bits
  16 bits
  32 bits
  64 bits
-

- Question # 6 of 10 (Start time: 10:06:57 PM) Total Marks: 1
  Which one of the following portions of an instruction represents the operation to be performed?
  Select correct option:

  Address
  Instruction code
  Opcode
  Operand
-
- Question # 8 of 10 (Start time: 10:07:36 PM) Total Marks: 1
  For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory
  Select correct option:

  Jump
  Control
  load/store
  None of the given
-
- Question # 9 of 10 (Start time: 10:08:08 PM) Total Marks: 1
  Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
  Select correct option:

  Processor-Memory-Switch level (PMS level)
  Instruction Set Level
  Register Transfer Level
  None of the given
-
- Question # 10 of 10 (Start time: 10:08:50 PM) Total Marks: 1
  Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3
  Select correct option:

  Opcode= R1, DR=ADD, SA=R2, SB=R3
  Opcode= ADD, DR=R1, SA=R2, SB=R3
  Opcode= R2, DR=ADD, SA=R1, SB=R3
  Opcode= ADD, DR=R3, SA=R2, SB=R1
-
- Question # 1 of 10 (Start time: 10:20:53 PM) Total Marks: 1
  Which one of the following circuit design levels is called the gate level?
  Select correct option:

  Logic Design Level
  Circuit Level
  Mask Level
  None of the given
-
- Question # 2 of 10 (Start time: 10:21:17 PM) Total Marks: 1
  The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
  Select correct option:

  Jump and branch format instructions
  Immediate format instructions
  Register format instructions
  All of the above

-
- Question # 5 of 10 (Start time: 10:24:08 PM) Total Marks: 1
  P: R3 <- R5 MAR <- IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
  Select correct option:

  Parentheses ()
  Arrow <-
  Colon :
  Comma ,
-
- Question # 6 of 10 (Start time: 10:25:09 PM) Total Marks: 1
  In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
  Select correct option:

  Arithmetic/logic
  Load/store
  Test/branch
  None of the given
-
- What does the word 'D' in the 'D-flip-Flop' stands for?
  Select correct option:

  Data
  Digital
  Dynamic
  Double
-
- Question # 9 of 10 (Start time: 10:27:24 PM) Total Marks: 1
  The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]
  Select correct option:

  Add R3, 56
  lar R3, 56
  ldr R3, 56
  str R3, 56
-
- Question # 10 of 10 (Start time: 10:28:07 PM) Total Marks: 1
  What is the instruction length of the FALCON-E processor?
  Select correct option:

  8 bits
  16 bits
  32 bits
  64 bits
-
- Question # 2 of 10 (Start time: 10:41:07 PM) Total Marks: 1
  Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
  Select correct option:

  4 bytes, 7 bytes
  7 bytes, 16 bytes
  10 bytes, 19 bytes

13 bytes, 22 bytes

Question # 3 of 10 (Start time: 10:41:57 PM) Total Marks: 1
Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:

Address
Instruction code
Opcode
Operand

Question # 4 of 10 (Start time: 10:42:17 PM) Total Marks: 1
Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?
Select correct option:

:=
&
%
©

Question # 5 of 10 (Start time: 10:42:37 PM) Total Marks: 1
What is the size of the memory space that is available to FALCON-A processor?
Select correct option:

2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes

Question # 7 of 10 (Start time: 10:43:25 PM) Total Marks: 1
An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------
Select correct option:

compiler
cross assembler
debugger
linker

Question # 8 of 10 (Start time: 10:43:59 PM) Total Marks: 1
Which instruction is used to store register to memory using relative address?
Select correct option:

ld instruction
ldr instruction
lar instruction
str instruction

Question # 9 of 10 (Start time: 10:44:37 PM) Total Marks: 1
What does the instruction "ldr R3, 58" of SRC do?
Select correct option:

It will load the register R3 with the contents of the memory location M [PC+58]

It will load the register R3 with the relative address itself (PC+58).
It will store the register R3 contents to the memory location M [PC+58]
No operation
Question # 1 of 10 (Start time: 11:06:09 PM) Total Marks: 1
Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?
Select correct option:
Base address
Binary address
Effective address
All of the given

- Quiz Start Time: 11:06 PM
  Time Left 88
  sec(s)
  Question # 2 of 10 (Start time: 11:06:53 PM) Total Marks: 1
  How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
  Select correct option:
  IR<16..0>
  IR<15..0>
  IR<16..1>
  IR<15..1>
-
- Question # 3 of 10 (Start time: 11:07:32 PM) Total Marks: 1
  What functionality is performed by the instruction "str R8, 34" of SRC?
  Select correct option:
  It will load the register R8 with the contents of the memory location M [PC+34]
  It will load the register R8 with the relative address itself (PC+34).
  It will store the register R8 contents to the memory location M [PC+34]
  No operation
-
- Question # 4 of 10 (Start time: 11:08:39 PM) Total Marks: 1
  Which type of instructions help in changing the flow of the program as and when required?
  Select correct option:
  Arithmetic
  Control
  Data transfer
  Floating point
-
- Question # 5 of 10 (Start time: 11:09:24 PM) Total Marks: 1
  Whic of the following statements is/are true about RISC processors' claimed advantages over CISC processors? (a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution. (b) RISC CPUs outperform CISC CPU's in procedural programming environments. (c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction. (d) It is easier to maintain the "family concept" in RISC CPUs.
  Select correct option:
  (a), (b) &(c)
  (b), (c) & (e)
  (c), (d) & (e)
  (a), (c) & (d)
-
- Question # 8 of 10 (Start time: 11:11:44 PM) Total Marks: 1
  Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
  Select correct option:
  Processor-Memory-Switch level (PMS level)

Instruction Set Level
Register Transfer Level
None of the given

- Question # 9 of 10 (Start time: 11:12:32 PM) Total Marks: 1
  Which one of the following is/are the features of Register Transfer Language? a) It is a symbolic language b) It is describing the internal organization of digital computers c) It is an elementary operation performed (during one clock pulse), on the information stored in one or more registers d) It is high level language
  Select correct option:
  (b) only
  (a) & (b) only
  (a) ,(b) & (d)
  (b),(c) & (d)

Question # 10 of 10 (Start time: 11:14:04 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

- Question # 3 of 10 (Start time: 08:03:34 PM) Total Marks: 1
  Motorola MC68000 is an example of ---------microprocessor.
  Select correct option:

  CISC
  RISC
  SRC
  FALCON

Question # 5 of 10 (Start time: 08:05:09 PM) Total Marks: 1
Which one of the following registers holds the instruction that is being executed?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 9 of 10 (Start time: 08:08:13 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:

Registers
Control signals
Memory
None of the given

Question # 10 of 10 (Start time: 08:09:02 PM) Total Marks: 1

The external interface of FALCON-A consists of a _____ data bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 1 of 10 (Start time: 08:18:13 PM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 2 of 10 (Start time: 08:18:29 PM) Total Marks: 1
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?
Select correct option:

Perfecting
Pipelining
Superscalar operation
Speedup

Question # 3 of 10 (Start time: 08:18:52 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC
INC4
LC
Cout

Question # 4 of 10 (Start time: 08:19:03 PM) Total Marks: 1
The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------
Select correct option:

Exception
Function
Thread
Stack

Question # 5 of 10 (Start time: 08:20:13 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 6 of 10 (Start time: 08:20:40 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:

INC4
LPC
PCout
LC

Question # 7 of 10 (Start time: 08:21:15 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 8 of 10 (Start time: 08:21:49 PM) Total Marks: 1
Computer system performance is usually measured by the ----------
Select correct option:

Time to execute a program or program mix
The speed with which it executes programs
Processor's utilization in solving the problems
Instructions that can be carried out simultaneously I use here double dip :d

Question # 9 of 10 (Start time: 08:22:09 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ address bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:22:19 PM) Total Marks: 1
Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?
Select correct option:

Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 1 of 10 (Start time: 08:24:34 PM) Total Marks: 1
---------- performs the data operations as commanded by the program instructions.
Select correct option:

Control

Datapath
Structural RTL
Timing

Question # 2 of 10 (Start time: 08:25:17 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:

INC4
LPC
PCout
LC

Question # 3 of 10 (Start time: 08:25:30 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____address bus and a _____ data bus.
Select correct option:

8-bit , 8-bit
16-bit , 16-bit
16-bit , 24-bit
16-bit , 32-bit

Question # 4 of 10 (Start time: 08:25:50 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 5 of 10 (Start time: 08:26:02 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 6 of 10 (Start time: 08:26:41 PM) Total Marks: 1
Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?
Select correct option:

Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 7 of 10 (Start time: 08:27:38 PM) Total Marks: 1
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
Select correct option:

8-bits

16-bits
32-bits
64-bits

Question # 8 of 10 (Start time: 08:27:54 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC
INC4
LC
Cout

Question # 9 of 10 (Start time: 08:28:10 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ data bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:28:29 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:

Registers
Control signals
Memory
None of the given

Which one of the following is the memory organization of EAGLE processor?

- 2^8 * 8 bits
- 2^16 * 8 bits
- 2^32 * 8 bits
- 2^64 * 8 bits
-
-

Which instruction is used to store register to memory using relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction

What is the working of Processor Status Word (PSW)?
Select correct option:
To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing
To hold the address of the next instruction in memory that is to be executed

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

What functionality is performed by the instruction "lar R3, 36" of SRC?
Select correct option:
It will load the register R3 with the contents of the memory location M [PC+36]
It will load the register R3 with the relative address itself (PC+36).
It will store the register R3 contents to the memory location M [PC+36]
No operation

In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

Which field of the machine language instruction is the "type of operation" that is to be performed?
Select correct option:
Op-code (or the operation code)
CPU registers
Memory cells
I/O locations

What functionality is performed by the instruction "str R8, 34" of SRC?
Select correct option:
It will load the register R8 with the contents of the memory location M [PC+34]
It will load the register R8 with the relative address itself (PC+34).
It will store the register R8 contents to the memory location M [PC+34]
No operation

Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction
Select correct option:
(a)& (b)
(b)&(c)
(a)&(e)
(b)&(e)

Which of the instruction is used to load register from memory using a relative address?
Select correct option:
ld instruction note Sure
ldr instruction
lar instruction
str instruction

Execution time of a program with respect to the processor is calculated as:
Select correct option:
Execution Time = IC x CPI x MIPS
Execution Time = IC x CPI x T
Execution Time = CPI x T x MFLOPS
Execution Time = IC x T

Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction
(a)& (b)
(b)&(c)
(a)&(e)
(b)&(e)

What functionality is performed by the instruction "lar R3, 36" of SRC?
It will load the register R3 with the contents of the m
It will load the register R3 with the relative address itself (PC+36).
It will store the register R3 contents to the memory
No operation

Which one of the following is a bi-stable device, capable of storing one bit of Information?
Decoder
Flip-flop
Multiplexer
Diplexer

Which instruction is used to store register to memory using relative address?
ld instruction
ldr instruction
lar instruction
str instruction

Almost every commercial computer has its own particular ———- language
3GL
English language
Higher level language
assembly language

For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory
Jump
Control
load/store
None of the given

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
Jump and branch format instructions
Immediate format instructions
Register format instructions

_____ operation is required to change the processor's state to a known, defined value.
Change
Reset
Update
None of the given

- 1.In the little-endian format exchanging data between computers, the data transmitted by one will be received in a "swapped" form by the other
- ans: on page247

- 6. _____ means that the CPU should input data from an input device only when the device is ready to provide data and send data to an output device only when it is ready to receive data.
- **Ans: Data synchronization (page 237)**

Which is the last instruction of the ISR that is to be executed when the ISR terminates?

Select correct option:

- iret

irq

int

nmi

Question 2 of 10

Identify the following type of serial communication error condition in which no character is

available at the beginning of an interval.

Select correct option:

Framing error

Parity error

- Overrun error

Under-run error

Question 3 of 10

In which one of the following methods, does the CPU poll to identify the interrupting module

and branches to an interrupt service routine on detecting an interrupt?

Select correct option:

Daisy Chain

- Software Poll

Multiple interrupt lines

All of the given options

Question 4 of 10

In which one of the following methods for resolving the priority, the device with the highest

priority is placed in the first position, followed by lower-priority devices up to the device with

the lowest priority, which is placed last in the series?

Select correct option:

Asynchronous

Daisy-Chaining Priority
- Parallel

Semi-synchronous

Question 5 of 10

Where does the processor store the address of the first instruction of the ISR?

Select correct option:
- Interrupt vector

Question 6 of 10

_____ is an electrical pathway through which the processor communicates with the internal and

external devices attached to the computer.

Select correct option:
- Computer Bus

Hazard

Memory

Disk

Question 7 of 10

----------the device usually means reading its status register every so often until the device's

status changes to indicate that it has completed the request.

Select correct option:

- Executing

Interrupting

Masking

Polling

Question 8 of 10

A software routine performed when an interrupt is received by the computer is called as ---------

Select correct option:

Interrupt

- Interrupt handler

Exception

Trap

Question 9 of 10

Which one of the following is NOT a technique used when the CPU wants to exchange data

with a peripheral device?

Select correct option:

Direct Memory Access (DMA)

Interrupt driven I/O

Programmed I/O

- Virtual Memory

Question 10 of 10

Which is the last instruction of the ISR that is to be executed when the ISR terminates?

(Repeated this question)

Select correct option:

- IRET

IRQ

INT

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
=>**Interrupt vector**
Interrupt request
Interrupt handler
All of the given options

In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
=>**Isolated I/O**
Memory Mapped I/O
All of above
None of above

---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
=>**Interrupt Latency**
Response Deadline
Timer delay
Throughput

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
=>**Partial decoding**

1. A collection of ----------is called a micro program.
A. large scale operations
B. Registers
C. DMA
D. Microinstructions
Microinstructions.

2. ____is the time needed by the CPU to recognize (not service) an interrupt request
A. Interrupt Latency
B. Response Deadline
C. Timer delay
D. Throughput
Interrupt Latency.

3. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller

C. DMA Controller
D. Virtual Memory
Micro program controller.

4. Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
A. Direct Memory Access (DMA)
B. Interrupt driven I/O
C. Programmed I/O
D. Virtual Memory
Virtual Memory .

5. Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error
Overrun error.

6. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll
C. Multiple interrupt lines
D. All of the given options
Software Poll.

7. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices
D. Multiplexers
Peripheral devices.

8. In _____, a separate address space of the CPU is reserved for I/O operations.
A. Isolated I/O
B. Memory Mapped I/O
C. All of above
D. None of above
Isolated I/O.

9. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel

D. Semi-synchronous
Parallel.

10. _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
A. Microprogramming
B. Instruction pre-fetching
C. Pipelining
D. Partial decoding
Partial decoding.

11. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops

B. Memory
C. Peripheral devices
D. Multiplexers
Peripheral devices.

12. _____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.

A. Computer Bus
B. Hazard
C. Memory
D. Disk
Computer Bus.

13. Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?

A. Framing error
B. Parity error
C. Overrun error
D. Under-run error
Framing error.

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
Hardware interrupt
Software interrupt
All of the given
None of the given

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
Interrupt vector
Interrupt request
Interrupt handler
All of the given options

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
Peripheral devices
Multiplexers

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
=>A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
=>Interrupt handler
Exception
Trap

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
=>Parallel Priority
Semi-synchronous Priority

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Microprogramming
Instruction pre-fetching
Pipelining
Partial Decoding

An Interface that can be used to connect the microcomputer bus to _____ is called an I/O port
Flip flops
Memory
Peripherals devices
Multiplexes

Connection to a CPU that provides a data path between the CPU and external devices, such as a keyboard, display, or reader is called----------
Buffer
I/O port
Memory mapping
Processor

In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority which is placed last in the series?
Asynchronous
Daisy-Chaining Priority
Parallel
Semi-synchronous

Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
Framing error
Parity error
Overrun error
Under-run error

Where does the processor store the address of the first instruction of the ISR?
Interrupt vector
Interrupt request
Interrupt handler

All of the given Options

Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Framing error
Parity error
Overrun error
Under-Run error

In _____ a separate address space of the CPU is reserved for I/O operations
Isolated I/O
Memory Mapped I/O
All of the above
None of above

Every time you press a key, an interrupts is generated. This is an example of
Hardware Interrupt
Software Interrupt
All of the given
None of the given

_____ is an electrical pathway through which the processor communication with the internal and external devices attached to the computer.
Computer Bus
Hazard
Memory
Disk

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
Interrupt vector
Interrupt request
Interrupt handler
All of the given options

In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
Isolated I/O
Memory Mapped I/O
All of above
None of above

---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
Interrupt Latency
Response Deadline
Timer delay
Throughput

_____ is a technique in which some of the CPU’s address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching

Pipelining
Partial decoding

The _____ can be determined from the number of platters and the number of tracks.
Select correct option:
Speed of processing
execution time
storage capacity
Latency

A component connected to the _____ and with which the master component can communicate during a particular bus cycle. Normally the CPU with its bus control logic is the master component.
Select correct option:
Slave component
System bus
Master component
Bus component

The average latency to the desired data is halfway round the disk so, what will be the average rotational latency if the disk rotates at 20,000 rpm.
Select correct option:
1.25ms
1.5ms324
1.0ms
2.0ms

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
Partial decoding

Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Which is the last instruction of the ISR that is to be executed when the ISR terminates?
Select correct option:
IRET
IRQ
INT
NMI

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
Hardware interrupt
Software interrupt
All of the given
None of the given

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
Interrupt vector
Interrupt request
Interrupt handler
All of the given options

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
Peripheral devices
Multiplexers

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
Interrupt vector
Interrupt request
Interrupt handler
All of the given options

In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
Isolated I/O
Memory Mapped I/O
All of above
None of above

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---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
Interrupt Latency
Response Deadline
Timer delay
Throughput

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining

Partial decoding

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor (page 198,223, 273)
A process where input devices can takeover the working of the microprocessor

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
Peripheral devices
Multiplexers

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
Hardware interrupt
Software interrupt
All of the given
None of the given

Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
=>Overrun error
Under-run error

Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
Interrupt handler
Exception
Trap

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority

Asynchronous Priority
Parallel Priority
Semi-synchronous Priority

1. A collection of ----------is called a micro program.
A. large scale operations
B. Registers
C. DMA
D. Microinstructions
Microinstructions.

2. ____is the time needed by the CPU to recognize (not service) an interrupt request
A. Interrupt Latency
B. Response Deadline
C. Timer delay
D. Throughput
Interrupt Latency.

3. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller
C. DMA Controller
D. Virtual Memory
Micro program controller.

4. Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
A. Direct Memory Access (DMA)
B. Interrupt driven I/O
C. Programmed I/O
D. Virtual Memory
Virtual Memory .

5. Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error
Overrun error.

6. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll
C. Multiple interrupt lines
D. All of the given options
Software Poll.

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7. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices
D. Multiplexers
Peripheral devices.

8. In _____, a separate address space of the CPU is reserved for I/O operations.

A. Isolated I/O
B. Memory Mapped I/O
C. All of above
D. None of above
Isolated I/O.

9. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel
D. Semi-synchronous
Parallel.

10. _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
A. Microprogramming
B. Instruction pre-fetching
C. Pipelining
D. Partial decoding
Partial decoding.
Where does the processor store the address of the first instruction of the ISR?
Select correct option:
=>**Interrupt vector**
Interrupt request
Interrupt handler
All of the given options

In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
=>**Isolated I/O**
Memory Mapped I/O
All of above
None of above

---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
=>**Interrupt Latency**
Response Deadline
Timer delay
Throughput

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
=>**Partial decoding**

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
=>A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

Question # 6
An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
=>Peripheral devices
Multiplexers

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
=>Hardware interrupt
Software interrupt
All of the given
None of the given

Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
=>Overrun error
Under-run error

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
=>Interrupt handler
Exception
Trap

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
=>Parallel Priority
Semi-synchronous Priority

In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
Select correct option:
Daisy Chain

- Software Poll

Multiple interrupt lines
All of the given options

In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
Select correct option:
Asynchronous
Daisy-Chaining Priority
- Parallel

Semi-synchronous

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
- Interrupt vector

_____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.
Select correct option:
- Computer Bus

Hazard
Memory
Disk

----------the device usually means reading its status register every so often until the device's status changes to indicate that it has completed the request.
Select correct option:
- Executing

Interrupting
Masking
Polling

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
- Interrupt handler

Exception
Trap

Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
Select correct option:
Direct Memory Access (DMA)
Interrupt driven I/O
Programmed I/O
- Virtual Memory

Question 10 of 10
Which is the last instruction of the ISR that is to be executed when the ISR terminates? (Repeated this question)
Select correct option:
- IRET

IRQ
I

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
Peripheral devices
Multiplexers

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
Hardware interrupt
Software interrupt
All of the given
None of the given

Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
Interrupt handler
Exception
Trap

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
Semi-synchronous Priority

In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
Select correct option:

Asynchronous
Daisy-Chaining Priority
Parallel
Semi-synchronous

In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
Isolated I/O
Memory Mapped I/O
All of above
None of above

Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
Semi-synchronous Priority

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
Interrupt handler
Exception
Trap

_____ is a technique in which some of the CPU’s address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
Partial decoding

Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
Interrupt vector
Interrupt request
Interrupt handler
All of the given options

Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
Select correct option:
Direct Memory Access (DMA)
Interrupt driven I/O
Programmed I/O
Virtual Memory

A software routine performed when an interrupt is received by the computer is called as ---------
InterruptC
Interrupt handler
Exception
Trap

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
Semi-synchronous Priority

---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Interrupt Latency
Response Deadline
Timer delay
Throughput

_____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.
Computer Bus
Hazard
Memory
Disk

Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
Direct Memory Access (DMA). •
Interrupt driven I/O •
Programmed I/O •
Virtual Memory

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
Semi-synchronous Priority
The Pentium does allow the use of some part of its _____ accumulator register EAX
32 bits (not sure)

In the little-endian format exchanging data between computers, the data transmitted by one will be received in a "swapped" form by the other.
swapped (not sure)
A collection of ----------is called a micro program.
Microinstructions
_____ form the branch control field in the micro instruction.

B Bits

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
=>Peripheral devices
Multiplexers

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
=>Hardware interrupt
Software interrupt
All of the given
None of the given

Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
Select correct option:
Framing error
Parity error
=>Overrun error
Under-run error
In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?

Asynchronous
Daisy-Chaining Priority Click here for detail
Parallel
Semi-synchronous

Interrupt driven I/O is better than _____.
polling

Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
choose correct one:
Framing error
Parity error
Overrun error
Under-run error

The _____ can be determined from the number of platters and the number of tracks.
Select correct option:

Speed of processing
execution time
storage capacity
Latency

A component connected to the _____ and with which the master component can communicate during a particular bus cycle. Normally the CPU with its bus control logic is the master component.
Select correct option:
Slave component
System bus
Master component
Bus component

The average latency to the desired data is halfway round the disk so, what will be the average rotational latency if the disk rotates at 20,000 rpm.

Select correct option:
1.25ms
1.5ms324
1.0ms
2.0ms

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
Partial decoding

Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Which is the last instruction of the ISR that is to be executed when the ISR terminates?
Select correct option:
IRET
IRQ
INT
NMI

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
Hardware interrupt
Software interrupt
All of the given
None of the given

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
Interrupt vector
Interrupt request
Interrupt handler
All of the given options

Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
Select correct option:
Daisy Chain
Software Poll
Multiple interrupt lines
All of the given options

In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
Select correct option:
Asynchronous
Daisy-Chaining Priority
Parallel
Semi-synchronous

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Where does the processor store the address of the first instruction of the ISR?
Select correct option:
Interrupt vector

_____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.
Select correct option:
Computer Bus
Hazard

Memory
Disk

----------the device usually means reading its status register every so often until the device's status changes to indicate that it has completed the request.
Select correct option:
Executing
Interrupting
Masking
Polling

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
Interrupt handler
Exception
Trap

Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
Select correct option:
Direct Memory Access (DMA)
Interrupt driven I/O
Programmed I/O
Virtual Memory

Which is the last instruction of the ISR that is to be executed when the ISR terminates? (Repeated this question)
Select correct option:
IRET
IRQ
INT

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Where does the processor store the address of the first instruction of the ISR?
Select correct option:
=>Interrupt vector
Interrupt request
Interrupt handler
All of the given options

1. A collection of ----------is called a micro program.
A. large scale operations
B. Registers
C. DMA
D. Microinstructions
Microinstructions.

2. ____is the time needed by the CPU to recognize (not service) an interrupt request
A. Interrupt Latency
B. Response Deadline
C. Timer delay
D. Throughput
Interrupt Latency.

3. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller
C. DMA Controller
D. Virtual Memory
Micro program controller.

4. Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
A. Direct Memory Access (DMA)
B. Interrupt driven I/O
C. Programmed I/O
D. Virtual Memory
Virtual Memory .

5. Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error
Overrun error.

6. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll
C. Multiple interrupt lines
D. All of the given options
Software Poll.

7. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices
D. Multiplexers
Peripheral devices.

8. In _____, a separate address space of the CPU is reserved for I/O operations.
A. Isolated I/O
B. Memory Mapped I/O
C. All of above
D. None of above
Isolated I/O.

9. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel
D. Semi-synchronous
Parallel.

10. _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
A. Microprogramming
B. Instruction pre-fetching
C. Pipelining
D. Partial decoding
Partial decoding.

11. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices
D. Multiplexers
Peripheral devices.
12. _____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.
A. Computer Bus
B. Hazard
C. Memory
D. Disk
Computer Bus.

13. Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error
Framing error.

14. How can you define an interrupt?
A. A process where an external device can speedup the working of the microprocessor
B. A process where memory can speed up programs execution speed
C. A process where an external device can get the attention of the microprocessor
D. A process where input devices can takeover the working of the microprocessor
A process where an external device can get the attention of the microprocessor.

15. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel
D. Semi-synchronous
Parallel.

16. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll
C. Multiple interrupt lines
D. All of the given options
Software Poll.

17. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller
C. DMA Controller
D. Virtual Memory
Micro program controller.

18. Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error
Overrun error.

In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
=>Isolated I/O
Memory Mapped I/O
All of above
None of above

---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
=>Interrupt Latency
Response Deadline
Timer delay
Throughput

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
=>Partial decoding

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
=>A process where an external device can get the attention of the microprocessor (p198, 223, 273)
A process where input devices can takeover the working of the microprocessor

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
=>Peripheral devices
Multiplexers

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
=>Hardware interrupt
Software interrupt
All of the given
None of the given

Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
Select correct option:
Framing error
Parity error
=>Overrun error
Under-run error

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
=>Interrupt handler
Exception
Trap

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
=>Parallel Priority
Semi-synchronous Priority

1_ Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
Direct Memory Access (DMA). •
Interrupt driven I/O •
Programmed I/O •
Virtual Memory

2_Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority

Semi-synchronous Priority
3_ The Pentium does allow the use of some part of its _____ accumulator register EAX
32 bits (not sure)

4_In the little-endian format exchanging data between computers, the data transmitted by one will be received in a "swapped" form by the other.
swapped (not sure)

5_A collection of ----------is called a micro program.
Microinstructions

6_ _____ form the branch control field in the micro instruction.

B Bits

7_In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?

Asynchronous
Daisy-Chaining Priority Click here for detail
Parallel
Semi-synchronous

8_signal has input direction with respect to printer

PE#

9_Interrupt driven I/O is better than _____.
polling

10_Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
choose correct one:
Framing error
Parity error
Overrun error
Under-run error
Q:1 How can you define an interrupt?

A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

Q:2 Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?

Framing error
Parity error
Overrun error
Under-run error

Q:3 In the little-endian format exchanging data between computers, the data transmitted by one will be received in a "swapped" form by the other.

Organized
Signals
Swapped
Arranged

Q:4 Which is the last instruction of the ISR that is to be executed when the ISR terminates?

IRET
IRQ
INT
NMI

14. How can you define an interrupt?
A. A process where an external device can speedup the working of the microprocessor
B. A process where memory can speed up programs execution speed
C. A process where an external device can get the attention of the microprocessor
D. A process where input devices can takeover the working of the microprocessor
A process where an external device can get the attention of the microprocessor.

15. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel
D. Semi-synchronous
Parallel.

16. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll
C. Multiple interrupt lines
D. All of the given options
Software Poll.

1_ Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
Direct Memory Access (DMA). •
Interrupt driven I/O •
Programmed I/O •
Virtual Memory

2_Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority

Semi-synchronous Priority
3_ The Pentium does allow the use of some part of its _____ accumulator register EAX
32 bits (not sure)

4_In the little-endian format exchanging data between computers, the data transmitted by one will be received in a "swapped" form by the other.
swapped (not sure)

17. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller
C. DMA Controller
D. Virtual Memory
Micro program controller.

18. Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error

Overrun error.
Q:5 _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.

Microprogramming
Instruction pre-fetching
Pipelining
Partial decoding

Q:6 A software routine performed when an interrupt is received by the computer is called as ---------
Interrupt
Interrupt handler
Exception

Trap
Q:7 Every time you press a key, an interrupt is generated. This is an example of
Hardware interrupt
Software interrupt
All of the given
None of the given

5_A collection of ----------is called a micro program.
Microinstructions

6_ _____ form the branch control field in the micro instruction.

B Bits

7_In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?

Asynchronous
Daisy-Chaining Priority Click here for detail
Parallel
Semi-synchronous

8_signal has input direction with respect to printer
PE#

9_Interrupt driven I/O is better than _____.
polling

10_Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
choose correct one:
Framing error
Parity error
Overrun error
Under-run error
Q:1 How can you define an interrupt?

A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

Q:2 Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?

Framing error
Parity error
Overrun error
Under-run error

Q:3 In the little-endian format exchanging data between computers, the data transmitted by one will be received in a "swapped" form by the other.

Organized

Signals
Swapped
Arranged

Q:4 Which is the last instruction of the ISR that is to be executed when the ISR terminates?

IRET
IRQ
INT
NMI

Q:8 Where does the processor store the address of the first instruction of the ISR?

Interrupt vector
Interrupt request
Interrupt handler
All of the given options
Q:9 *Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?*
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
Semi-synchronous Priority

Q:10 ---------- is the time needed by the CPU to recognize (not service) an interrupt request.

Interrupt Latency
Response Deadline
Timer delay
Throughput
Where does the processor store the address of the first instruction of the ISR?
Select correct option:
Interrupt vector
Interrupt request
Interrupt handler
All of the given options
Question # 2
In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
Isolated I/O
Memory Mapped I/O
All of above
None of above
Question # 3
---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
Interrupt Latency
Response Deadline
Timer delay
Throughput

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
Partial decoding

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor (page 198,223, 273)
A process where input devices can takeover the working of the microprocessor

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
Peripheral devices
Multiplexers

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
Hardware interrupt
Software interrupt
All of the given
None of the given

Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
=>Overrun error
Under-run error

Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
Interrupt handler
Exception
Trap

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
Semi-synchronous Priority

A collection of ----------is called a micro program.
A. large scale operations
B. Registers
C. DMA
D. Microinstructions
Microinstructions.

2. ____is the time needed by the CPU to recognize (not service) an interrupt request
A. Interrupt Latency
B. Response Deadline
C. Timer delay
D. Throughput
Interrupt Latency.

3. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller
C. DMA Controller
D. Virtual Memory
Micro program controller.

4. Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
A. Direct Memory Access (DMA)
B. Interrupt driven I/O
C. Programmed I/O
D. Virtual Memory
Virtual Memory .

5. Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error
Overrun error.

6. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll
C. Multiple interrupt lines
D. All of the given options
Software Poll.

7. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices
D. Multiplexers
Peripheral devices.

8. In _____, a separate address space of the CPU is reserved for I/O operations.
A. Isolated I/O
B. Memory Mapped I/O
C. All of above
D. None of above
Isolated I/O.
9. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel
D. Semi-synchronous
Parallel.

10. _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
A. Microprogramming
B. Instruction pre-fetching
C. Pipelining
D. Partial decoding
Partial decoding.

Where does the processor store the address of the first instruction of the ISR?
Select correct option:
=>Interrupt vector
Interrupt request
Interrupt handler
All of the given options

In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
=>Isolated I/O
Memory Mapped I/O
All of above
None of above
Question # 3
---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
=>Interrupt Latency
Response Deadline
Timer delay
Throughput

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
=>Partial decoding

How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
=>A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
=>Peripheral devices
Multiplexers

Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
=>Hardware interrupt
Software interrupt
All of the given
None of the given

Identify the following type of serial communication error condition: "The prior character that was

received was not still read by the CPU and is over written by a new received character."
Select correct option:
Framing error
Parity error
=>Overrun error
Under-run error

A software routine performed when an interrupt is received by the computer is called as ---------
Select correct option:
Interrupt
=>Interrupt handler
Exception
Trap

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
=>Parallel Priority
Semi-synchronous Priority

Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.
v:shapes="imgAlertSelect">Select correct option:

v:shapes="imgAlertSave">

Question # 2 of 10 (Start time: 08:53:47 PM) Total Marks: 1
An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
v:shapes="_x0000_i1036"> Select correct option:

Question # 3 of 10 (Start time: 08:54:15 PM) Total Marks: 1
Connection to a CPU that provides a data path between the CPU and external devices, such as a keyboard, display, or reader is called----------
v:shapes="_x0000_i1044">Select correct option:

Question # 4 of 10 (Start time: 08:54:40 PM) Total Marks: 1
In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
v:shapes="_x0000_i1053"> Select correct option:

Question # 5 of 10 (Start time: 08:54:59 PM) Total Marks: 1
---------- is the time needed by the CPU to recognize (not service) an interrupt request.
v:shapes="_x0000_i1062"> Select correct option:

Question # 6 of 10 (Start time: 08:55:22 PM) Total Marks: 1
Where does the processor store the address of the first instruction of the ISR?
v:shapes="_x0000_i1071"> Select correct option:

Question # 7 of 10 (Start time: 08:55:40 PM) Total Marks: 1
_____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.
v:shapes="_x0000_i1080"> Select correct option:

100% correct and 100% same quiz no 2

Tri-state buffers are used for removing _____. Select correct option
Instruction collision
bus collision
Instruction contention
bus contention ok

Where does the processor store the address of the first instruction of the ISR? Select correct option
Interrupt vector
Interrupt request
Interrupt handler
All of the given options (not conform)

Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)? Select correct option
Framing error ok
Parity error
Overrun error
Under-run error

In _____, a separate address space of the CPU is reserved for I/O operations. Select correct option
Isolated I/O ok
Memory Mapped I/O
All of above
None of above

----------the device usually means reading its status register every so often until the device's status changes to indicate that it has completed the request. Select correct option
Interrupting
Masking
Polling ok
Executing

In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series? Select correct option
Asynchronous
Daisy-Chaining Priority
Parallel ok
Semi-synchronous

A software routine performed when an interrupt is received by the computer is called as --------- Select correct option
Interrupt
Interrupt handler ok
Exception
Trap

Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device? Select correct option
Direct Memory Access (DMA)
Interrupt driven I/O
Programmed I/O
Virtual Memory ok

A computer interface is an _____ circuit that matches the requirements of the two subsystems between which it is connected Select correct option
Digital
Electronic ok
Primary
Obituary

The information about interrupt vector is given in 8-bits, from bit 0 to 7, which is translated to bit _____ on the data bus. Select correct option
16 to 23 ok
11 to 18
0 to 7
8 to 15

1. A collection of ----------is called a micro program.
A. large scale operations
B. Registers
C. DMA
D. Microinstructions ok

2. ____is the time needed by the CPU to recognize (not service) an interrupt request
A. Interrupt Latency ok
B. Response Deadline
C. Timer delay
D. Throughput

3. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller ok
C. DMA Controller
D. Virtual Memory

4. Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?
A. Direct Memory Access (DMA)
B. Interrupt driven I/O
C. Programmed I/O
D. Virtual Memory ok

5. Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
A. Framing error
B. Parity error
C. Overrun error ok
D. Under-run error
Overrun error.

6. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll ok
C. Multiple interrupt lines
D. All of the given options
Software Poll.

7. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices ok
D. Multiplexers
Peripheral devices.

8. In _____, a separate address space of the CPU is reserved for I/O operations.
A. Isolated I/O ok
B. Memory Mapped I/O
C. All of above
D. None of above
Isolated I/O.

9. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel ok
D. Semi-synchronous
Parallel.

10. _____ is a technique in which some of the CPU’s address lines forming an input to the address decoder are ignored.
A. Microprogramming
B. Instruction pre-fetching
C. Pipelining

D. Partial decoding ok
Partial decoding.

11. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices ok
D. Multiplexers
Peripheral devices.
12. _____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.
A. Computer Bus ok
B. Hazard
C. Memory
D. Disk
Computer Bus.

13. Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
A. Framing error ok
B. Parity error
C. Overrun error
D. Under-run error
Framing error.

14. How can you define an interrupt?
A. A process where an external device can speedup the working of the microprocessor
B. A process where memory can speed up programs execution speed
C. A process where an external device can get the attention of the microprocessor ok
D. A process where input devices can takeover the working of the microprocessor
A process where an external device can get the attention of the microprocessor.

15. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel ok
D. Semi-synchronous
Parallel.

16. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll ok
C. Multiple interrupt lines
D. All of the given options
Software Poll.

17. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller ok
C. DMA Controller
D. Virtual Memory
Micro program controller.

18. Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
A. Framing error
B. Parity error
C. Overrun error ok
D. Under-run error
Overrun error.

-

Q 1 **For any of the instructions that are a part of the instruction set of the SRC, there are cerain_____required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.**

- Register
- **Control signals**
- Memory
- None of the given

Q 2 **FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC _____wide.**

- 8-bits
- 16-bits
- **32-bits**
- 64-bits

Q 3 **What is the instruction length of the FALCON-A processor**

- 8-bits
- **16-bits**
- 32-bits
- 64-bits

Q 4 **_____control signals enable the input to the PC for receiving a value that is currently on the internal processor bus.**

- **LPC**
- INC4
- LC
- I

Q 5 **Which one of the following is a bi-stable device, capable of storing one bit of information?**

- Decoder
- **Flip-Flop**
- Multiplexer
- Diplexer

Q 6 **Which instruction is used to store register to memory using relative address?**

- ld instruction
- ldr instruction
- lar instruction
- **str instruction**

Q 7 **Which field of the machine language instruction is the "type of operation" that is to be performed?**

- **Op-code (or the operation code)**
- CPU registers
- Momory cells
- I/O locations

Q 8 **The instruction _____ will load the register R3 with the contenets of the m\emory location M [PC+56]**

___Add R3, 56

___lar R3, 56

___ldr R3, 56

___str R3, 56

Q 9 **_____ operation is required to change the processor's state to a known, defined value.**

- Change
- **Reset**
- Update
- None of the given

Q 10 **which type of instructions help in changing the flow of the program as and when required?**

- Arithmetic
- **Control**
- Data transfer

- Floating point

- Question # 1 of 10 (Start time: 10:02:48 PM) Total Marks: 1
  What is the size of the memory space that is available to FALCON-A processor?
  Select correct option:

  2^8 bytes
  2^16 bytes
  2^32 bytes
  2^64 bytes

- Question # 2 of 10 (Start time: 10:03:58 PM) Total Marks: 1
  How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
  Select correct option:

  IR<16..0>
  IR<15..0>
  IR<16..1>
  IR<15..1>

- Question # 3 of 10 (Start time: 10:04:28 PM) Total Marks: 1
  What is the working of Processor Status Word (PSW)?
  Select correct option:

  To hold the current status of the processor.
  To hold the address of the current process
  To hold the instruction that the computer is currently processing
  To hold the address of the next instruction in memory that is to be executed

- Question # 4 of 10 (Start time: 10:05:10 PM) Total Marks: 1
  What does the instruction "ldr R3, 58" of SRC do?
  Select correct option:

  It will load the register R3 with the contents of the memory location M [PC+58]
  It will load the register R3 with the relative address itself (PC+58).
  It will store the register R3 contents to the memory location M [PC+58]
  No operation

- Question # 5 of 10 (Start time: 10:06:34 PM) Total Marks: 1
  What is the instruction length of the FALCON-E processor?
  Select correct option:

  8 bits
  16 bits
  32 bits
  64 bits

- Question # 6 of 10 (Start time: 10:06:57 PM) Total Marks: 1
  Which one of the following portions of an instruction represents the operation to be performed?
  Select correct option:

  Address
  Instruction code
  Opcode
  Operand

- Question # 8 of 10 (Start time: 10:07:36 PM) Total Marks: 1
  For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory

Select correct option:

Jump
Control
load/store
None of the given

- Question # 9 of 10 (Start time: 10:08:08 PM) Total Marks: 1
  Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
  Select correct option:

  Processor-Memory-Switch level (PMS level)
  Instruction Set Level
  Register Transfer Level
  None of the given

- Question # 10 of 10 (Start time: 10:08:50 PM) Total Marks: 1
  Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3
  Select correct option:

  Opcode= R1, DR=ADD, SA=R2, SB=R3
  Opcode= ADD, DR=R1, SA=R2, SB=R3
  Opcode= R2, DR=ADD, SA=R1, SB=R3
  Opcode= ADD, DR=R3, SA=R2, SB=R1

- Question # 1 of 10 (Start time: 10:20:53 PM) Total Marks: 1
  Which one of the following circuit design levels is called the gate level?
  Select correct option:

  Logic Design Level
  Circuit Level
  Mask Level
  None of the given

- Question # 2 of 10 (Start time: 10:21:17 PM) Total Marks: 1
  The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
  Select correct option:

  Jump and branch format instructions
  Immediate format instructions
  Register format instructions
  All of the above

- Question # 5 of 10 (Start time: 10:24:08 PM) Total Marks: 1
  P: R3 <- R5 MAR <- IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
  Select correct option:

  Parentheses ()
  Arrow <-
  Colon :
  Comma ,

- Question # 6 of 10 (Start time: 10:25:09 PM) Total Marks: 1
  In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
  Select correct option:

  Arithmetic/logic
  Load/store
  Test/branch
  None of the given
-
- What does the word 'D' in the 'D-flip-Flop' stands for?
  Select correct option:

  Data
  Digital
  Dynamic
  Double
-
- Question # 9 of 10 (Start time: 10:27:24 PM) Total Marks: 1
  The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]
  Select correct option:

  Add R3, 56
  lar R3, 56
  ldr R3, 56
  str R3, 56
-
- Question # 10 of 10 (Start time: 10:28:07 PM) Total Marks: 1
  What is the instruction length of the FALCON-E processor?
  Select correct option:

  8 bits
  16 bits
  32 bits
  64 bits
-
- Question # 2 of 10 (Start time: 10:41:07 PM) Total Marks: 1
  Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
  Select correct option:

  4 bytes, 7 bytes
  7 bytes, 16 bytes
  10 bytes, 19 bytes
  13 bytes, 22 bytes

  Question # 3 of 10 (Start time: 10:41:57 PM) Total Marks: 1
  Which one of the following portions of an instruction represents the operation to be performed?
  Select correct option:

  Address
  Instruction code
  Opcode
  Operand

  Question # 4 of 10 (Start time: 10:42:17 PM) Total Marks: 1

Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?
Select correct option:

:=
&
%
©

Question # 5 of 10 (Start time: 10:42:37 PM) Total Marks: 1
What is the size of the memory space that is available to FALCON-A processor?
Select correct option:

2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes

Question # 7 of 10 (Start time: 10:43:25 PM) Total Marks: 1
An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------
Select correct option:

compiler
cross assembler
debugger
linker

Question # 8 of 10 (Start time: 10:43:59 PM) Total Marks: 1
Which instruction is used to store register to memory using relative address?
Select correct option:

ld instruction
ldr instruction
lar instruction
str instruction

Question # 9 of 10 (Start time: 10:44:37 PM) Total Marks: 1
What does the instruction "ldr R3, 58" of SRC do?
Select correct option:

It will load the register R3 with the contents of the memory location M [PC+58]
It will load the register R3 with the relative address itself (PC+58).
It will store the register R3 contents to the memory location M [PC+58]
No operation
Question # 1 of 10 (Start time: 11:06:09 PM) Total Marks: 1
Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?
Select correct option:
Base address
Binary address
Effective address
All of the given

-

Quiz Start Time: 11:06 PM
Time Left 88

sec(s)
Question # 2 of 10 (Start time: 11:06:53 PM) Total Marks: 1
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
Select correct option:
IR<16..0>
IR<15..0>
IR<16..1>
IR<15..1>

- Question # 3 of 10 (Start time: 11:07:32 PM) Total Marks: 1
What functionality is performed by the instruction "str R8, 34" of SRC?
Select correct option:
It will load the register R8 with the contents of the memory location M [PC+34]
It will load the register R8 with the relative address itself (PC+34).
It will store the register R8 contents to the memory location M [PC+34]
No operation

- Question # 4 of 10 (Start time: 11:08:39 PM) Total Marks: 1
Which type of instructions help in changing the flow of the program as and when required?
Select correct option:
Arithmetic
Control
Data transfer
Floating point

- Question # 5 of 10 (Start time: 11:09:24 PM) Total Marks: 1
Whic of the following statements is/are true about RISC processors' claimed advantages over CISC processors? (a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution. (b) RISC CPUs outperform CISC CPU's in procedural programming environments. (c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction. (d) It is easier to maintain the "family concept" in RISC CPUs.
Select correct option:
(a), (b) &(c)
(b), (c) & (e)
(c), (d) & (e)
(a), (c) & (d)

- Question # 8 of 10 (Start time: 11:11:44 PM) Total Marks: 1
Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

- Question # 9 of 10 (Start time: 11:12:32 PM) Total Marks: 1
Which one of the following is/are the features of Register Transfer Language? a) It is a symbolic language b) It is describing the internal organization of digital computers c) It is an elementary operation performed (during one clock pulse), on the information stored in one or more registers d) It is high level language
Select correct option:
(b) only
(a) & (b) only
(a) ,(b) & (d)
(b),(c) & (d)

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Question # 10 of 10 (Start time: 11:14:04 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

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- Question # 3 of 10 (Start time: 08:03:34 PM) Total Marks: 1
Motorola MC68000 is an example of ---------microprocessor.
Select correct option:

CISC
RISC
SRC
FALCON

Question # 5 of 10 (Start time: 08:05:09 PM) Total Marks: 1
Which one of the following registers holds the instruction that is being executed?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 9 of 10 (Start time: 08:08:13 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:

Registers
Control signals
Memory
None of the given

Question # 10 of 10 (Start time: 08:09:02 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ data bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 1 of 10 (Start time: 08:18:13 PM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:

Accumulator

Address Mask
Instruction Register
Program Counter

Question # 2 of 10 (Start time: 08:18:29 PM) Total Marks: 1
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?
Select correct option:

Perfecting
Pipelining
Superscalar operation
Speedup

Question # 3 of 10 (Start time: 08:18:52 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC
INC4
LC
Cout

Question # 4 of 10 (Start time: 08:19:03 PM) Total Marks: 1
The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------
Select correct option:

Exception
Function
Thread
Stack

Question # 5 of 10 (Start time: 08:20:13 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 6 of 10 (Start time: 08:20:40 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:

INC4
LPC
PCout
LC

Question # 7 of 10 (Start time: 08:21:15 PM) Total Marks: 1

Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 8 of 10 (Start time: 08:21:49 PM) Total Marks: 1
Computer system performance is usually measured by the ----------
Select correct option:

Time to execute a program or program mix
The speed with which it executes programs
Processor's utilization in solving the problems
Instructions that can be carried out simultaneously I use here double dip :d

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Question # 9 of 10 (Start time: 08:22:09 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ address bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:22:19 PM) Total Marks: 1
Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?
Select correct option:

Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 1 of 10 (Start time: 08:24:34 PM) Total Marks: 1
---------- performs the data operations as commanded by the program instructions.
Select correct option:

Control
Datapath
Structural RTL
Timing

Question # 2 of 10 (Start time: 08:25:17 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:

INC4
LPC
PCout
LC

Question # 3 of 10 (Start time: 08:25:30 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____address bus and a _____ data bus.
Select correct option:

8-bit , 8-bit
16-bit , 16-bit
16-bit , 24-bit
16-bit , 32-bit

Question # 4 of 10 (Start time: 08:25:50 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 5 of 10 (Start time: 08:26:02 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 6 of 10 (Start time: 08:26:41 PM) Total Marks: 1
Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?
Select correct option:

Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 7 of 10 (Start time: 08:27:38 PM) Total Marks: 1
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
Select correct option:

8-bits
16-bits
32-bits
64-bits

Question # 8 of 10 (Start time: 08:27:54 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC
INC4
LC
Cout

Question # 9 of 10 (Start time: 08:28:10 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ data bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:28:29 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:

Registers
Control signals
Memory
None of the given

Which one of the following is the memory organization of EAGLE processor?

- 2^8 * 8 bits
- 2^16 * 8 bits
- 2^32 * 8 bits
- 2^64 * 8 bits
-
-

Which instruction is used to store register to memory using relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction

What is the working of Processor Status Word (PSW)?
Select correct option:
To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing
To hold the address of the next instruction in memory that is to be executed

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

What functionality is performed by the instruction "lar R3, 36" of SRC?
Select correct option:
It will load the register R3 with the contents of the memory location M [PC+36]
It will load the register R3 with the relative address itself (PC+36).
It will store the register R3 contents to the memory location M [PC+36]
No operation

In which of the following instructions the data move between a register in the

processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

Which field of the machine language instruction is the "type of operation" that is to be performed?
Select correct option:
Op-code (or the operation code)
CPU registers
Memory cells
I/O locations

What functionality is performed by the instruction "str R8, 34" of SRC?
Select correct option:
It will load the register R8 with the contents of the memory location M [PC+34]
It will load the register R8 with the relative address itself (PC+34).
It will store the register R8 contents to the memory location M [PC+34]
No operation

Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction
Select correct option:
(a)& (b)
(b)&(c)
(a)&(e)
(b)&(e)

Which of the instruction is used to load register from memory using a relative address?
Select correct option:
ld instruction note Sure
ldr instruction
lar instruction
str instruction

Execution time of a program with respect to the processor is calculated as:
Select correct option:
Execution Time = IC x CPI x MIPS
Execution Time = IC x CPI x T
Execution Time = CPI x T x MFLOPS
Execution Time = IC x T

Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr
instruction e) Stop operation or stop instruction
(a)& (b)
(b)&(c)
(a)&(e)
(b)&(e)

What functionality is performed by the instruction "lar R3, 36" of SRC?
It will load the register R3 with the contents of the m
It will load the register R3 with the relative address itself (PC+36).
It will store the register R3 contents to the memory
No operation

Which one of the following is a bi-stable device, capable of storing one bit of Information?
Decoder
Flip-flop
Multiplexer
Diplexer

Which instruction is used to store register to memory using relative address?
ld instruction
ldr instruction
lar instruction
str instruction

Almost every commercial computer has its own particular ———- language
3GL
English language
Higher level language
assembly language

For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory
Jump
Control
load/store
None of the given

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
Jump and branch format instructions
Immediate format instructions
Register format instructions

_____ operation is required to change the processor's state to a known, defined value.
Change
Reset
Update
None of the given