MIDTERM EXAMINATION
Spring 2009
CS302- Digital Logic Design (Session - 1)

Question No: 1 (Marks: 1) - Please choose one

In the binary number "10011" the weight of the most significant digit is ____

► 2^4 (2 raise to power 4)
► 2^3 (2 raise to power 3)
► 2^0 (2 raise to power 0)
► 2^1 (2 raise to power 1)

Question No: 2 (Marks: 1) - Please choose one

An S-R latch can be implemented by using _____ gates

► AND, OR
► **NAND, NOR**
► NAND, XOR
► NOT, XOR

Question No: 3 (Marks: 1) - Please choose one

A latch has _____ stable states

► One
► **Two**
► Three
► Four

Question No: 4 (Marks: 1) - Please choose one

Sequential circuits have storage elements

► **True**
► False

Question No: 5 (Marks: 1) - Please choose one

The ABEL symbol for “XOR” operation is

► **$**
► **#**
► !
► &

Question No: 6 (Marks: 1) - Please choose one

A Demultiplexer is not available commercially.

► **True**
► False

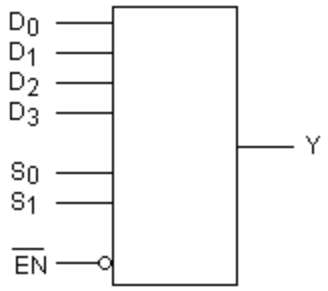
Question No: 7 (Marks: 1) - Please choose one

Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

► A parallel to serial converter circuit
► **A counter circuit**
► A BCD to Decimal decoder
► A 2-to-8 bit decoder

Question No: 8 (Marks: 1) - Please choose one

The device shown here is most likely a



► Comparator
► **Multiplexer**
► Demultiplexer
► Parity generator

Question No: 9 (Marks: 1) - Please choose one

The main use of the Multiplexer is to

► **Select data from multiple sources and to route it to a single Destination**
► Select data from Single source and to route it to a multiple Destinations
► Select data from Single source and to route to single destination
► Select data from multiple sources and to route to multiple destinations

Question No: 10 (Marks: 1) - Please choose one

A logic circuit with an output <PRIVATE "TYPE=PICT;ALT= mcq5_01700.gif"> $X = \overline{A}BC + A\overline{B}$ consists of _____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► **two AND gates, one OR gate, two inverters**
► two AND gates, one OR gate

Question No: 11 (Marks: 1) - Please choose one

The binary value of 1010 is converted to the product term $\bar{A}B\bar{C}D$

► True

► **False**

Question No: 12 (Marks: 1) - Please choose one

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8**
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one

Following is standard POS expression

$(A+\bar{B}+C+\bar{D})(A+\bar{B}+C+D)(A+B+\bar{C}+\bar{D})(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+D)$

► **True**
► False

Question No: 14 (Marks: 1) - Please choose one

The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

► Undefined

► **One**
► Zero
► 10 (binary)

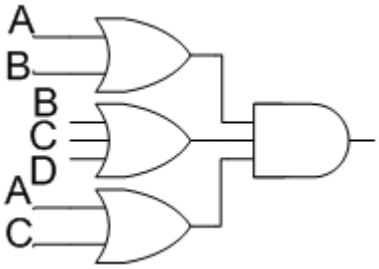
Question No: 15 (Marks: 1) - Please choose one

The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► **7-bit**
► 8-bit
► 16-bit

Question No: 16 (Marks: 1) - Please choose one

The diagram given below represents _____



► Demorgans law
► Associative law
► **Product of sum form**
► Sum of product form

Question No: 17 (Marks: 1)

How can a PLD be programmed?

PLDs are programmed with the help of computer which runs the programming software. The computer is connected to a programmer socket in which the PLD is inserted for programming. PLDs can also be programmed when they are installed on a circuit board

Question No: 18 (Marks: 1)

How many input and output bits do a Half-Adder contain?

The Half-Adder has a 2-bit input and a 2-bit output.

Question No: 19 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer 2-to-4 Binary Decoder?

The circuit of the 1-to-4 Demultiplexer is similar to the 2-to-4 Binary Decoder
described earlier figure 16.9. The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit figure

Question No: 20 (Marks: 3)

Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL.

Device declaration, pin declarations and set declarations.

Question No: 21 (Marks: 5)

Explain with example how noise affects Operation of a CMOS AND Gate circuit.

Two CMOS 5 volt series AND gates are connected together. Figure 7.3 The first AND gate has both its inputs connected to logic high, therefore the output of the gate is guaranteed to be logic high. The logic high voltage output of the first AND gate is assumed to be 4.6 volts well within the valid VOH range of 5-4.4 volts. Assume the same noise signal (as described earlier) is added to the output signal of the first AND gate.

Question No: 22 (Marks: 10)

explain the SOP based implementation of the Adjacent 1s Detector Circuit

The Adjacent 1s Detector accepts 4-bit inputs. If two adjacent 1s are detected in the
input, the output is set to high. The operation of the Adjacent 1s Detector is represented by the
function table. Table 13.6. In the function table, for the input combinations 0011, 0110, 0111,
1011, 1100, 1101, 1110 and 1111 the output function is a 1.
Implementing the circuit directly from the function table based on the SOP form
requires 8 AND gates for the 8 product terms (minterms) with an 8-input OR gate. Figure 13.3.
The total gate count is
_ One 8 input OR gate
_ Eight 4 input AND gates
_ Ten NOT gates
The expression can be simplified using a Karnaugh map, figure 13.4, and then the
simplified expression can be implemented to reduce the gate count. The simplified expression
isAB + CD +BC . The circuit implemented using the expression AB + CD +BC has reduced
to 3 input OR gate and 2 input AND gates.
The simplified Adjacent 1s Detector circuit uses only four gates reducing the cost, the
size of the circuit and the power requirement. The propagation delay of the circuit is of the order of two gates

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