Cs 302 Mid Term Objective Type

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Please choose one
A SOP expression is equal to 1 _____

► All the variables in domain of expression are present
► At least one variable in domain of expression is present.
► When one or more product terms in the expression are equal to 0.
► **When one or more product terms in the expression are equal to 1**

- Please choose one
The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► **A=01, B=10**

) - Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► **True**
► False

- Please choose one
High level Noise Margins (VNH) of CMOS 5 volt series circuits is _____

► 0.3 V
► 0.5 V
► **0.9 V (**
► 3.3 V

Please choose one
If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them in
floating point representation and then multiplying them, the value of mantissa of result will be _____

► **24.582 (But not sure)**
► 2.4582
► 24582
► 0.24582

Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol“+“ here
represents OR Gate.

► Undefined
► **One**
► Zero

► 10 (binary)

Please choose one
If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► SET (
► RESET
► Clear
► Invalid

Please choose one
3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation
► Fast switching speeds, high power dissipation
► Fast switching speeds, very low power dissipation
► Low switching speeds, very low power dissipation

Please choose one
The binary value “1010110” is equivalent to decimal _____

► 86 (According to Formula)
► 87
► 88
► 89

Please choose one
The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder

► BCD-to-Decimal
► **Decimal-to-BCD Priority**

Please choose one
"Sum-of-Weights" method is used _____

► **to convert from one number system to other (**
► to encode data
► to decode data
► to convert from serial to parralel data

- Please choose one
The maximum number that can be represented using unsigned octal system is _____

► 1
► **7**
► 9
► 16

- Please choose one
If we add “723” and “134” by representing them in floating point notation i.e. by first, converting them in
floating point representation and then adding them, the value of exponent of result will be _____

► 0
► 1
► **2**
► 3

Please choose one
The diagram given below represents _____

► Demorgans law
► Associative law
► **Product of sum form (According to rule of theorem)**
► Sum of product form

Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2**
► 1
► 3
► 4

- Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic**
► Generic Array Logic
► Generic Analysis Logic

- Please choose one
The Quad Multiplexer has _____ outputs

► **4**
► 8
► 12
► 16

Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan‟s Law
► Distributive Law
► Commutative Law

► **Associative Law (**

Please choose one
2's complement of any binary number can be calculated by

► adding 1's complement twice
► **adding 1 to 1's complement (**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Please choose one
The binary value “1010110” is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

Please choose one
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► **XOR (**

The binary value “11011” is equivalent to _____

►**1B (According to rule)**
►1C
►1D
►1E

. An important application of AND Gate is its use in counter circuit

►**True (**
►False

The OR Gate performs a Boolean _____ function

►**Addition**
►Subtraction
►Multiplication
►Division

TTL based devices work with a dc supply of ____ Volts

►+10
►**+5**
►+3
►3.3

A standard POS form has _____ terms that have all the variables in the domain of the expression.

►**Sum**
►Product
►Min
►Composite

. A SOP expression having a domain of 3 variables will have a truth table having ____ combinations of inputs and corresponding output values.

►2
►4
►**8 (According to rule)**

►16

A BCD to 7-Segment decoder has

►3 inputs and 7 outputs
►4 inputs and 7 outputs)
►7 inputs and 3 outputs
► inputs and 4 outputs

. In the Karnaugh map shown above, which of the loops shown represents a legal grouping?

►A
► ►
C
►D

The binary value of 1010 is converted to the product term

►True
►False

10. The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

►A > B = 1, A < B = 0, A < B = 1
►A > B = 0, A < B = 1, A = B = 0
►A > B = 1, A < B = 0, A = B = 0
►A > B = 0, A < B = 1, A = B = 1

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

►**SET ()**
►RESET
►Clear
►Invalid

. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS
5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal
(VoH) will be in the range of _____ volts.

►4 to 4.5
►**4.5 to 5**
►0 to 4.5
►0 to 3.5

. A.(B.C) = (A.B).C is an expression of _____

►Demorgan‟s Law
►Distributive Law
►Commutative Law
►**Associative Law**

The 4-bit 2's complement representation of "+5" is _____

►1010
►1110
►**1011**
►0101

Which of the number is not a representative of hexadecimal system

►1234
►ABCD

►1001

Please choose one

► 1
► **7**
► 9
► 16

- Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8**
► 12
► 16

Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output
levels?

► A > B = 1, A < B = 0, A < B = 1
► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0**
► A > B = 0, A < B = 1, A = B = 1

) - Please choose one
A particular Full Adder has

► **3 inputs and 2 output**
► 3 inputs and 3 output
► 2 inputs and 3 output

► 2 inputs and 2 output

- Please choose one
The function to be performed by the processor is selected by set of inputs known as ____

► **Function Select Inputs**
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?
► **2 (**
► 1
► 3
► 4

- Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic (**
► Generic Array Logic
► Generic Analysis Logic

Please choose one
The Quad Multiplexer has _____ outputs
► **4**
► 8
► 12
► **16**

) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan‟s Law
► Distributive Law
► Commutative Law
► **Associative Law (**

- Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

- Please choose one
The binary value “1010110” is equivalent to decimal _____

► **86 (According to formula)**
► 87
► 88
► 89

- Please choose one
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► **NOT**
► **XOR**

- Please choose one
GALcan be reprogrammed because instead of fuses _____logic is

used in it

► **E2CMOS**
► TTL
► CMOS+
► **None of the given options**

Please choose one
The device shown here is most likely a

► Comparator
► **Multiplexer click here for detail**
► Demultiplexer
► Parity generator

Please choose one
If“1110” is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

► 2nd
► 4th
► 14th
► **No output wire will be activated**

- Please choose one
Half-Adder Logic circuit contains 2 XOR Gates

► True
► **False**

- Please choose one
A particular Full Adder has

► **3 inputs and 2 output**
► 3 inputs and 3 output

► 2 inputs and 3 output
► **2 inputs and 2 output**

- Please choose one
Sum = A ⊕ B ⊕ C CarryOut = C(A ⊕ B) + AB
are the Sum and CarryOut expression of

► Half Adder
► **Full Adder**
► 3-bit parralel adder
► MSI adder cicuit

Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input
variables and the resulting output of each value.

► **True click here for detail**
► **False**

Please choose one
The output A < B is set to 1 when the input combinations is

► A=10, B=01
► A=11, B=01
► A=01, B=01
► **A=01, B=10**

Please choose one
The 4-variable Karnaugh Map (K-Map) has _____cells for min or max terms

► 4
► 8
► 12

► **16**

- Please choose one
Generally, the Power dissipation of devices remains constant throughout their operation.

► **TTL**
► CMOS 3.5 series
► CMOS 5 Series
► **Power dissipation of all circuits increases with time.**

- Please choose one
The ecimal “8” is represented as using Gray-Code.

► 0011
► **1100**
► 1000
► 1010

Please choose one
(A+B).(A+C) =

► B+C
► **A+BC**
► AB+C
► AC+B

- Please choose one
A.(B+ C) = A.B + A.C is the expression of

► Demorgan‟s Law
► Commutative Law
► **Distributive Law**
► Associative Law

Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**
► **TRUE**

In ANSI/IEEE Standard 754 “Mantissa” is represented by 32-bits bits

► 8-bits
► 16-bits
► **32-bits**
► 64-bits

- Please choose one
Caveman number system is Base _5 number system

► 2
► **5**
► 10
► 16

- Please choose one
According to Demorgan‟s theorem:
_____

► A.B.C
►
► **(Page 74)**
►

- Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

\► 2-bit
► 7-bit
► **8-bit**
► 16-bit

) - Please choose one
The AND Gate performs a logical _____function

► Addition
► Subtraction
► **Multiplication**
► Division

Please choose one
NOR gate is formed by connecting _____

► **OR Gate and then NOT Gate**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Please choose one
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► **TTL**
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Please choose one
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► **True**
► False

Please choose one
When the control line in tri-state buffer is high the buffer operates like a _____ gate

► AND
► OR
► **NOT (**
► XOR

- Please choose one
The GAL22V10 has ____ inputs

► **22**
► 10
► 44
► 20

- Please choose one
The ABEL symbol for “OR” operation is

► !
► &
► **#**
► $

- Please choose one
The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► Similar
► Different
► **Similar with some enhancements**

► Depends on the type of PALs input size

Please choose one
All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► **" ; " (a semicolon)**
► " endl " (keyword "endl")

Please choose one
The Quad Multiplexer has _____ outputs

► **4 (**
► 8
► 12
► 16

- Please choose one
"Sum-of-Weights" method is used _____

► **to convert from one number system to other)**
► to encode data
► to decode data
► to convert from serial to parralel data

Please choose one
A latch has _____ stable states

► One
► **Two)**
► Three
► Four

- Please choose one
Sequential circuits have storage elements

► **True**
► False

Please choose one
The ABEL symbol for “XOR” operation is

► **$**
► #
► !
► &

- Please choose one
A Demultiplexer is not available commercially.

► **True**
► False

Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

► **A parallel to serial converter circuit**
► A counter circuit
► A BCD to Decimal decoder
► A 2-to-8 bit decoder

- Please choose one
The device shown here is most likely a
► Comparator
► **Multiplexer click here for detail**
► Demultiplexer

► Parity generator

Please choose one
The main use of the Multiplexer is to

► Select data from multiple sources and to route it to a single Destination (Page 167)
► Select data from Single source and to route it to a multiple Destinations
► Select data from Single source and to route to single destination
► Select data from multiple sources and to route to multiple destinations

- Please choose one
A logic circuit with an output consists of _____.

► two AND gates, two OR gates, two inverters
► three AND gates, two OR gates, one inverter
► two AND gates, one OR gate, two inverters
► two AND gates, one OR gate

Please choose one
The binary value of 1010 is converted to the product term

► True
► False

Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► 16

Please choose one
Following is standard POS expression

► **True (According to logic)**
► False

Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol"+" here
represents OR Gate.

► Undefined
► **One**
► Zero
► 10 (binary)

Please choose one
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► **8-bit**
► 16-bit

- Please choose one
The diagram given below represents _____

► Demorgans law
► Associative law
► **Product of sum form (According to rule)**
► Sum of product form

Please choose one
The diagram given below represents _____

► Demorgans law
► Associative law
► Product of sum form
► **Sum of product form**

Please choose one
The output of an AND gate is one when _____

► **All of the inputs are one**
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Please choose one
The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► **16)**

Please choose one
A BCD to 7-Segment decoder has

► 3 inputs and 7 outputs
► **4 inputs and 7 outputs**
► 7 inputs and 3 outputs
► 7 inputs and 4 outputs

Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement

a ____ multiplexer.

► 4-input, 8-bit
► 4-input, 16-bit
► 2-input, 8-bit
► **2-input, 4-bit**

- Please choose one
The PROM
consists of a fixed non-programmable _____ Gate array configured as a decoder.

► **AND**
► OR
► NOT
► XOR

Please choose one
In ABEL the variable „A“ is treated separately from variable „a“

► **True**
► False

Please choose one
The ABEL notation equivalent to Boolean expression A+B is:
► A & B
► A ! B
► **A # B**
► A $ B
L-21

Please choose one
If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be

_____.

► **SET**
► RESET
► Clear
► Invalid

Please choose one
Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► **Single input and multiple outputs.**
► Multiple inputs and single output.

- Please choose one
Which one is true:

► **Power consumption of TTL is higher than of CMOS**
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption
► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

Please choose one
The first Least Significant digit in decimal number system has

position 0 and weight equal to 1
position 1 and weight equal to 0
position 1 and weight equal to 10
position 0 and weight equal to 10

Please choose one
The decimal equivalent of the binary number “10011” is

19 (According to rule)
99
29
None of given options

Please choose one
In ANSI/IEEE Standard 754 “Mantissa” is represented by 32-bits bits

► 8-bits
► 16-bits
► **32-bits**
► 64-bits

Please choose one
The binary value “11011” is equivalent to

1B (According to rule)
1C
1D
1E

- Please choose one
NOR gate is formed by connecting

OR Gate and then NOT Gate
NOT Gate and then OR Gate
AND Gate and then OR Gate
OR Gate and then AND Gate

- Please choose one
“74ALS” stands for

Advanced Low-frequency Schottky TTL
Advanced Low-dissipation Schottky TTL
Advanced Low-Power Schottky TTL

Advanced Low-propagation Schottky TTL

- Please choose one
An adder circuit can be used to perform subtraction operation

True
False

Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

2)
3 4 1

Please choose one
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True
False

- Please choose one
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a multiplexer.

2-input, 4-bit
4-input, 8-bit
4-input, 16-bit
2-input, 8-bit

Please choose one
The four outputs of two 4-input multiplexers, connected to form a 16-input multiplexer, are connected
together through a 4-input gate

AND
OR
NAND
XOR

- Please choose one
The Programmable Array Logic (PAL) has AND array and a OR array

Fixed, programmable
Programmable, fixed
Fixed, fixed
Programmable, programmable

Please choose one
Sequential circuits have storage elements

True
False

Please choose one
Demultiplexer has

Single input and single outputs.
Multiple inputs and multiple outputs.
Single input and multiple outputs.
Multiple inputs and single output.

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