Total 26 Question
20 MCQ's
* All were from past paper ….. Especially from the Moaaz file.
Question No: 1 (Marks: 1) - Please choose one
A SOP expression is equal to 1 _____
► All the variables in domain of expression are present
► At least one variable in domain of expression is present.
► When one or more product terms in the expression are equal to 0.
► When one or more product terms in the expression are equal to 1. (Page 86)
Subjective Part:
"Write the uses of multiplexer". 2 marks
Answer: (Page 167) Multiplexer is a digital switch that has several inputs and a single output. Multiplexers are also known as Data Selectors. The main use of the Multiplexer is to select data from multiple sources and to route it to a single Destination.
"How many inputs and outputs have half Adder" 2 marks
Answer: 2 inputs and 2 outputs
"Write The parts of GAL16V8". 3marks
Answer: (Page 207) Lecture 21
"Draw the Function table of 2digit BCD Adder " 3marks
Answer: (Page 143)
"Write Function table and circuit of Logic Function Generator " 5marks
Answer: (Page 176)
"A Table was Given ... From table Sop Expression find karny thy by using K-map " 5marks

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Dear fellows,

This is the current paper of cs302 of 26/11/2011

Q1) See the attached file to solve the mcqs.
Q2) Draw the Tri_state buffer. 2
Q3) Draw the half adder graph. 2
Q4) Draw NOR gate based S_R (set rest) Latch. 3
Q5) Write drawback of 16_bit ALU with out Look_carry ahead. 5
Q6) Graph dia howa tha us k combinational logics likhne the or
simplified SOP expression likha tha. 5

---

20 mcqs thay
what is encoder
use of multiplexer
function of 3 to -8 deccoder
function table of 2 to -4 encoder
ak tabl sa diya hoa tha
for which input 2 complement is 0
yahi yad hain

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:1 Draw function table of an half adder circut? (2)
Q:2 What is diffrence b/w BCD to decimal decoder and binary 4-to-16 bit decoder? (2)
Q;3 Explain major use of decoder circuts? (3)
Q:4 PALS comes in different configurations and are identified by a unique number,identify parts of this number? (5)
Q:5 One of the ABEL entry method uses logic equation.explain atleast two example? (5)

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what is encoder
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function table of 2 to -4 encoder
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yahi yad hain

Aslamualaikum to all

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My today's CS302 paper **27-11-2011**
Q. Draw the function table of 2-to-4 decoder 2 marks
Q. Write Difference b/w "BCD to Decimal" decoder and "Binary 4 to 6" decoder 3marks
Q. Explain BCD to Decimal Decoder 3marks
Q.Explain how can we implement the addition of two BCD number with the help of two full adder. Also draw the block

diagram 5marks
Q. Explain 8-input Multiplexer with the help of circuit Diagram and Function Table. 5marks

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Total 26 questions.
20 MCQS.
6 Subjective.
12 MCQS are from past papers.

Subjective questions:
Q: 21: How a circuit with multiple outputs is shown in truth table? MARKS: 3:

Q: 22: Define Sequential Circuit. MARKS: 2:
Answer:
Digital circuits that generate a new output on the basis of some previously stored information and the new input are known as Sequential circuits.

Q: 23: Apply each of the following sets of binary numbers to Comparator inputs in figure and determine the output by following logic levels of the Circuit. MARKS: 5

(a) A= 10, B= 10.
(b) A= 11, B= 10.

Q: 24: Write uses of demultiplexer. MARKS: 5:

Q: 25: How decorder is used as demultiplexer.
MARKS: 3:

Q: 26: Two-bit iterative comparator circuit for comparison A=B. Explain functionality of the Circuit.
MARKS: 3:

Dear mera aj DLD ka paper tha.tough tha zra because past papers mein say kuch ni aya.mcqs bi.Ap k liay advice ha k just pprs pe satisfy na hn.Do more and more.paper is here

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1. Draw the function table of 3 to 8 decoder".5 marks
2. Draw the circuit diagram of NOR based S-R Latch ? 2 mrks
3. Demorgin's law 5 marks
4. table of half-adder 3marks

---

1. half adder 2

2. multiplexer 3
3. difference between bcd encoder and hexadecimal 2
4. BCD adder
5. ABEL language.
6. Full adder

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Answer: (Page 176)

"A Table was Given ... From table Sop Expression find karny thy by using K-map " 5marks

salam
1Q from ABEL ma vector bana tha
1Q from 2-bit comparator us SOP expression b bani thi cricuit b
1q about Kmap
1q demultipler and 2-to-4 binry decoder difference
baki mcqs pastpapers ma sa thya kuch .
2 qs yaad ni rhya
duwa kerna pass ho jaon umeed ni ha.
ALLAH kerya ma pass ho jaon .ameen

---

1. how many numbers of 1s does a minterm 1 contain?

2. Once the Logic circuit design has been entered its operation is verified by using 'test vectors'. Write two major roles of test vectors.
3. For a two bit comparator circuit, specify all the inputs for which the output A < B is set to 1.
4. Draw the function table of 2-input 4-bit multiplexer.

HINTS:
1) Input 1: 1A, 2A, 3A, 4A
2) Input 2: 1B, 2B, 3B, 4B
3) Active-high outputs: 1Y, 2Y, 3Y 4Y.
4) The "G" active-low pin enables or disables the Multiplexer
5) The single select input "S" allows input to be connected to output.
5. Draw the function table of Full adder circuit.
6. Decimal-to-BCD encoder circuit is shown below. Assume that the input 9 and 3 are both HIGH. Determine the output? Is it a valid BCD code

---

1-test vectors major two roles: (2marks)
2-difine three ways of connecting tri-state buffers. (3marks)
3- finding SOP expression from K-map. (3marks)
4- Draw given POS expressions to K-map. (5marks)
5- draw the function table of 8to3bit multiplexer. (5marks)
M.C.Qs were very easy.

CS302
Date 10-12-2012
Mid term

MCQs

1) Sum of C6 and B5 is ====== Answer: 17B
2) A.B.C Boolean expression generate 1 when _____ (under line is complement)

Answer: A=0, B=0, C=1

3) A+A.B = _____
a) A
b) B
c) A+B
d) (A+B)(A-B)
4) The output of AND gate is 1 when _____

Answer: all inputs are 1

5)

General implementation of _____ form

a) Boolean
b) Arbitrary
c) POS
d) SOP

6) The look_Ahead circuit is based on _____
7) Quad multiplexer has _____ inputs. Answer: 4
8) _____ Dual, 4 input multiplexer can be connected to form a 16 input multiplexer.

a) 2
b) 3
c) 4
d) 5

9) S-R latch can be implemented by _____Answer: NAND, NOR
10) What will be output of 3-input NOR gate for input value of A=1, B=0, C=1

a) Zero
b) One

11) 1100.111 first bit at right decimal point has the weight

a) ½
b) ¼
c) 0
d) 1

12) Which method of simplification is used when expression having more than 4 variables.
13) A k-map n grouping was given. Have to find legal grouping.
14) Main use of multiplexer is____ answer: collect data from different source and route it to a single destination
15) The device shown is like_____ Answer: Multiplexer tha
16) In signed binary number the_____ is used to represent the sign of number.

a) MSB
b) LSB
c) 0

17) Commutative law of multiplication. Answer: AB=BA
18) When 4 1's are taken as a group on k-map the number of variable eliminated from the output expression is/are_____

a) 1
b) 2
c) 3
d) 4

19) Simplifying POS expression requires the grouping of_____

a) 1's
b) 0's
c) Don't care
d) Both 0's and 1's

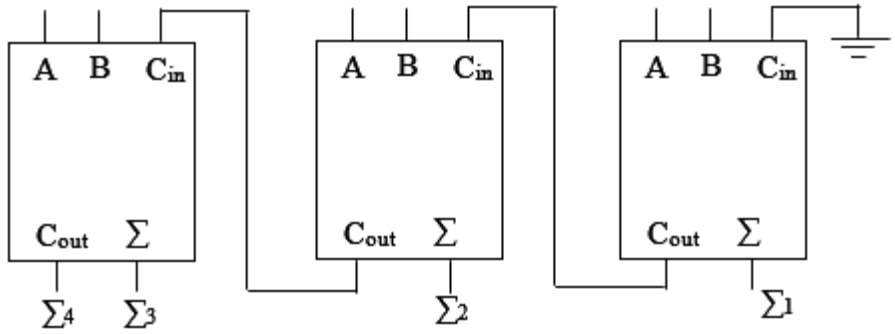
20) How many 4 bit parallel adders are required to add two BCD digits? 2marks
21) While comparing the operation of NAND and NOR in S-R latches. Diff b/w their operations. 2marks
22) 2 bit comparator circuit, specify all the input for which the output A<B is set to 1. 3marks

5/25/2013

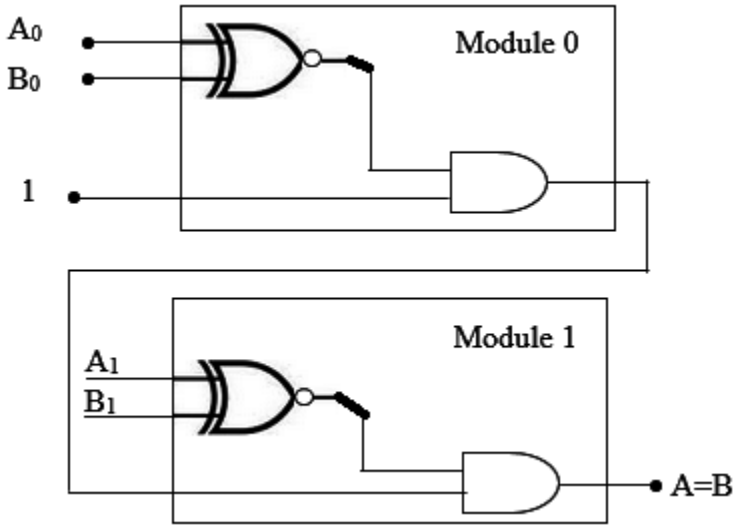
2 (A+C).(C+D).(B+C+D) State whether the above expression is SOP or POS?

2 How can we use 3-to-8 decoder to implement SOP expression?

3 The 3-bit parallel adder is shown below. The two numbers 101 and 011 are provided to this adder write down the values of $\sum_1$, $\sum_2$, $\sum_3$, $\sum_4$,C_{out1}, C_{out2}. $\sum_1$is the least significant.

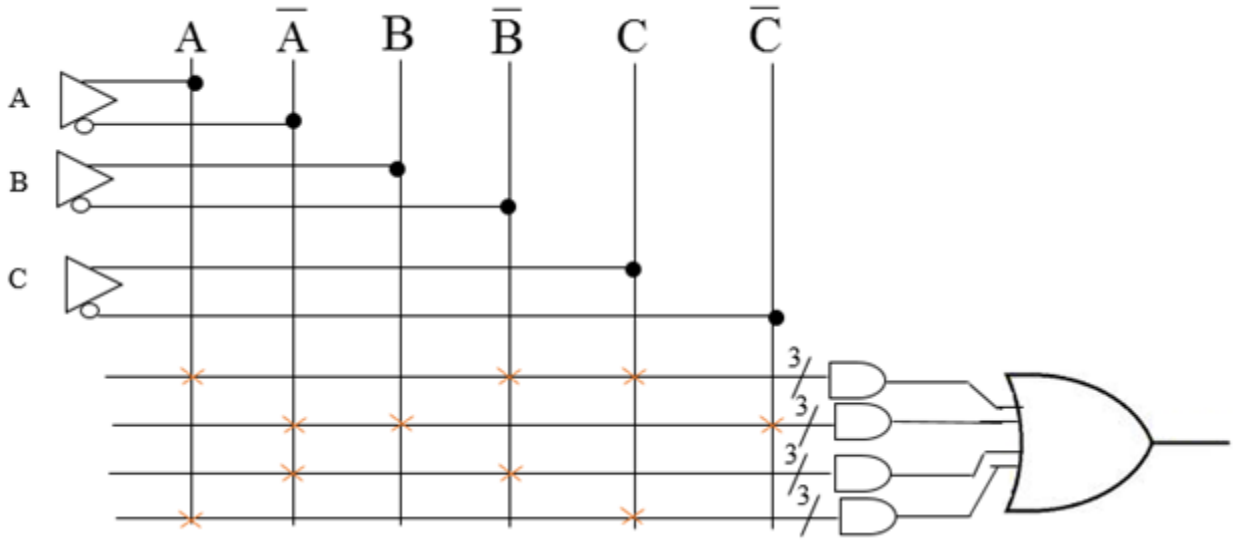


3 Given below is the diagram of 2-bit iterative comparator circuit for comparison A=B. Suppose A and B are the inputs; explain the functionality of circuit how this circuit works.



5 Draw the function table of the full adder.

5 A programmed array is shown in the figure below. The intact fusible link are indicated by small red Xs. Absence of an X means that the fuse is open. Analyze the figure below and write the output expression.



Current Cs302 paper (subjective)
1.what is the diffrence between BCD 7 segment decoder and binary decoder?(2)
2.Which gate is used for basic tri- state buffers?(2)
3.draw a circuit diagram for 2 -input ,4 bit multiplexer ?(3)
4.what an 8 bit adder/subtracter unit do/(3)
5. is m 1 truth table tha ODD parity generator wala ..and q ye tha k
define SOP expression mapping it on k-map and simplify them?(5)
6.elaborate tri -state buffer and draw tristate opening with NOT gate and High impedence state

---

25 may 2013 paper Cs302 Today Midterm Paper
Question (3 marks)
Converts binary values into Hexadecimal
1) 10001001
2) yad ni
3) 100100010001
Question (2 marks)
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Question (5 marks)
One karnauph map given SOP term nikalne thi
Question (2 marks)
What is comparator?
Question (5 Marks)
Explain Tri-State Buffers with the help of block diagram?
Question (5 Marks)
Draw the function table of 3 to 8 decoder

MCQS
1. In a karnaugh map the 6 term in pos or sop what is the value choose...
Option like
* 1100
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2.The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?
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* 10 pins
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* one
5. The _____ Encoder is used as a keypad encoder.
* Decimal-to-BCD Priority (Page 166)
6. the diagram above shows the general implementation of _____ form
* POS
7. The expression _____ is an example of Commutative Law for Multiplication.
* AB=BA (Page 72)
8. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS 5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (VoH) will be in the range of _____ volts.

* 4.5 to 5
9. The output A < B is set to 1 when the input combinations is
* A=01, B=10 (Page 109)
10. The 3-variable Karnaugh Map (K-Map) has _____cells for min or max terms
* 8
11. The output of an AND gate is one when _____
* All of the inputs are one
12. The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.
* AND (Page 182)
Baki mcqs yad ni hai...

All MCQs was from past papers.

1. How many inputs and outputs do half adder function contains?(2)
2. Write the simplified boolean expression of the given table. (2)

(A table was given)

3. How 3-to-8 encoder can be implemented?(3)
4. Give answers related to PAL GAL8V16 (3)
   1. How many inputs and outputs GAL8V16 contain?
   2. Name three modes of PAL.

5. Find the simplified Boolean expression of POS from the following table and how we implement by logic gates.(5)

(A table was given of 4 variables)

6. Write two bits comparator vector test.(5)

Todays Paper of CS302 DLD
Total 26 Q
20 MCqs
2 Q marks 2
2 Q marks 3
2 Q marks 5
MCQs were 50% from past papers
in subjective part that I can share are as follows
an express like AB+BC+AC was asked to write it in ABEL
like A&B # B&C # A&C
Max terms were given like (3,5,8,9,11)
and you have to map it to K-map.
One question was about Multiplexer
one question was about half adder.
wish you all best of luck.

Q1.HOW MANY 4BIT PARALLEL ADDRESS ARE TO ADD TWO BCD DIGITS?
Q2.DRAW THE CIRCUIT DIAGRAM OF TRI -STATE BUFFER
Q3.DRAW THE CIRCUIT OF NOR BASED S-R LATCH?
Q4. USING K MAP MINIMIZE THE POS EXPRESSION
Q5. A CIRCUIT WAS GIVEN AND WE EXPLAIN IT ABOUT 4 TO 5 LINES MEANS HOW TO WORK
Q6. A QUESTION ABOUT SOME DIGITS WAS GIVEN AND WE WRITE IT BY USING K MAP?

Aj ka paper

26 Questions
20 MCQ
2x2 = 4
3x2 = 6
5x2=10
Qestions about
Multiplexer
Demultiplexer
Hexadecimal
Decimal to BCD coded
ABEL language.
Write The parts of GAL16V8”

---

1. Draw the function table of 3 to 8 decoder".5 marks
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3. Demorgin's law 5 marks
4. table of half-adder 3marks

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multiplexer 3
difference between bcd encoder and hexadecimal 2

CS302 Paper

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Question (5 Marks)
Explain Tri-State Buffers with the help of block diagram?
Question (5 Marks)
Draw the function table of 3 to 8 decoder
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*** All of the inputs are one**
12. The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.
*** AND (Page 182)**

CS302 Today 26-05-2013 paper DLD (subjective)
1.why 2-bit comperator is called parallel comperator?(2)
2.Write the three modes in which PALs are programmed?(2)
3.Breifly explain the floating point number?(3)
4.draw a diagram for 16-bit multiplexer?(3)
5.AND gate and its uses?(5)

6..Implement odd parity generator circuit and mapping it on k-map and simplify expression?(5)

---

today my paper pray by God 4 me Allah hafiz
How many data select lines are required for selecting eight inputs? ► 1 ► 2
► 3 click here for detail ► 4
Demultiplexer has ► Single input and single outputs. ► Multiple inputs and multiple outputs. ► Single input and multiple outputs. (Page 178) ► Multiple inputs and single output
"Sum-of-Weights" method is used _____ ► to convert from one number system to other (Page 14) ► to encode data ► to decode data ► to convert from serial to parralel data
The range of Excess-8 code is from _____ to _____ ► +7 to -8 (Page 34) ► +8 to -7 ► +9 to -8 ► -9 to +8
A particular Full Adder has ► 3 inputs and 2 output (Page 135) ► 3 inputs and 3 output ► 2 inputs and 3 output ► 2 inputs and 2 output
is boolean expression for++11.)(1231SSSCout
►Half Adder ►Full Adder ►The Invalid BCD Detector Circuit (page 142) ►Parity Checker
The ecimal “8” is represented as using Gray-Code. ► 0011 ► 1100 (page 36) ► 1000 ► 1010
Write down the ABEL symbols that are used for NOT, AND, OR and XOR operations.
Answer:- (Page 201)•
NOT=! AND= & OR = # XOR =$.
"Draw the diagram of odd parity generator circuit". 2 marks
Draw the function table of two-bit comparator circuit, map it to K-Map and derive the expression

---

Current Cs302 paper (subjective)
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2.Which gate is used for basic tri- state buffers?(2)
3.draw a circuit diagram for 2 -input ,4 bit multiplexer ?(3)
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Today CS302 paper. Date: 25-5-2013
Today CS302 paper...

Date : 25-5-2013

Question (3 marks)

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3) 100100010001

Question (2 marks)

What is the opposite of the decoder?

Question (5 marks)

One karnauph map given SOP term nikalne thi

Question (2 marks)

What is comparator?

Question (5 Marks)

Explain Tri-State Buffers with the help of block diagram?

Question (5 Marks)

Draw the function table of 3 to 8 decoder

MCQS

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* A>B=1 A<B = 0 A=B= 0

3. What will be the output pins of decimal to bcd.

* 10 pins

4. 3 input or gate is given what will be the output when A=0, B=1, C=1

* one

5. The _____ Encoder is used as a keypad encoder.

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* AND (Page 182)

Baki mcqs yad ni hai...

My today's Paper of CS302 07/06/2014
Q1.Adder Circuit for Subtraction..[2]
Q2.NAND Base S-R Latch...[2]
Q3.Answer .....[3]
a)write input/ouput of following PAL GAL16v8
b)Three modes to program PAL.
Q4.Write Binary number for door lock and un-lock expression(Diagram was given)...[3]
Q5.using k Map minimize the following expression.(POS equation was given)...[5]
Q6.MUX used as logic function genrator,explain....[5]

My today's Paper of CS302 07/06/2014
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Q6.MUX used as logic function genrator,explain....[5]

MY today's paper of cs302 (MC120401302 WAQAS EJAZ)
All MCQs were from Moaaz file
Subjective
1.What are uses of multiplexer? 2marks

2. Provide at least four inputs for which the adjacent 1s detector circuit have active high output?

3Explain this unique number GAL16V8? 3 marks

4. Diagram was given and valuse were 101 and 011 given.
Write values of ? 3marks

5. Map following POS expression to Karnaugh Map 5marks

6. Diagram was given little bit same as in Fig 19.10 on page 184.
There were 3 input buffers A,B,C and 4 AND gates and fuse were in different place.
Us ko explain karna tha are output expression likhna tha. 5 marks

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CS302 Paper
Question (3 marks)
Converts binary values into Hexadecimal
1) 10001001
2) yad ni
3) 100100010001
Question (2 marks)
What is the opposite of the decoder?
Question (5 marks)
One karnauph map given SOP term nikalne thi
Question (2 marks)
What is comparator?
Question (5 Marks)
Explain Tri-State Buffers with the help of block diagram?
Question (5 Marks)
Draw the function table of 3 to 8 decoder
MCQS
1. In a karnaugh map the 6 term in pos or sop what is the value choose...
Option like
*** 1100**
*** 0011**
*** 1001**
2.The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?
*** A>B=1 A<B = 0 A=B= 0**
3. What will be the output pins of decimal to bcd.
*** 10 pins**
4. 3 input or gate is given what will be the output when A=0, B=1, C=1
one
5. The _____ Encoder is used as a keypad encoder.
*** Decimal-to-BCD Priority (Page 166)**
6. the diagram above shows the general implementation of _____ form
*** POS**
7. The expression _____ is an example of Commutative Law for Multiplication.
*** AB=BA (Page 72)**
8. Consider a circuit consisting of two consecutive NOT gates, the entire circuit belongs to a CMOS 5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (VoH) will be in the range of _____ volts.
*** 4.5 to 5**
9. The output A < B is set to 1 when the input combinations is
*** A=01, B=10 (Page 109)**
10. The 3-variable Karnaugh Map (K-Map) has _____cells for min or max terms
*** 8**
11. The output of an AND gate is one when _____
*** All of the inputs are one**

12. The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.
*** AND (Page 182)**

CS302 Today 26-05-2013 paper DLD (subjective)
1.why 2-bit comperator is called parallel comperator?(2)
2.Write the three modes in which PALs are programmed?(2)
3.Breifly explain the floating point number?(3)
4.draw a diagram for 16-bit multiplexer?(3)
5.AND gate and its uses?(5)
6..Implement odd parity generator circuit and mapping it on k-map and simplify expression?(5)

CS302 paper BY Anam Arooj

mcq mostly from old papers of Moaaz mcq file
Total 26 question 20 MCQS and 6 subjective
1-Draw the Truth-Table of NAND-based S-R Latch? (Marks: 2)
2-GAL are identified by a pre fix GAL no.there is GAL16v8 ?define Name of different parts in GAL16v8 and what function they perfome ? (Marks: 3)
3-Half adder explanation its function table Boolean expression and circuit diagram?draw half adder circuit? (Marks: 3)
4-non-standard SOP is converted into a standard SOP by accourding the rule??statement was given (marks:5)

On MCQ of voltage,options were:
1:one high voltage and two low voltage
2:two high voltage and one low voltage
3:all high voltage
4:all low
One MCQ was like "which metod is useful when the maximum numbers go above 4 variables"?Options were
1:karnugah map
2:quine-McCluskey
3:boolean expression & theorem
4:demorgan' s theorems

"which method is useful when the maximum numbers go above 4 variables"?Options were
1:karnugah map
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3:boolean expression & theorem
4:demorgan' s theorems
Ans:Quine McCluskey method

MY CS302 PAPER
Mcqs were mostly from Moaz's file

1. Make a test vector for 2 bit comparator circuit.
2. a= . Draw 'a' in logic gates
3. How to display Carry propagation?
4. Write 17 in BCD code.

5. Explain two major uses of Decoders.
6. How we can implement standard SOP using 3-t-8 decoder?

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in today my paper
80% mcq moaaz wali file mein sy thy mein ny file upload kar di hai is ko aap 100% prepare karey and mcq yeh tha..
which method is useful when the maximum numbers go above 4 variables"?Options were
1:karnugah map
2:quine-McCluskey
3:boolean expression & theorem
4:demorgan' s theorems
answer :2
The four outputs of two 4-input multiplexers, connected to form a 16-input multiplexer, are connected together through a 4-input gate
AND
OR
NAND
XOR
answer :OR
Two bit comparator? Explain by at least one example (2 marks)
Answer: (Page 109) Lec12 A 2-bit Comparator circuit compares two 2-bit numbers A and B. The comparator circuit has three outputs. It sets the A>B output to 1 if A>B. It sets the A=B output to 1 if A=B and sets A<B output to 1 if A < B.
jo mujey yaad tha wo mein ny aap ko bata diya 2 files mein ny aap ko di hain agar aap ny yeh prepare kar liya i assure ky aap achey marks ly kar pass hn gy

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draw the pos expression for the follwing k map marks 3
Draw the diagram of Nor based S R latch 3 Marks
write the Boolean expression for the 2 bit competitor circuit including A<B is High. 2 mraks
Truth Table of Nor S R latch 2 marks
Hire is my Today Paper Pleas share all papers Thank You

Asslam-O-Alaikum Friends...
80% MCQ'S From past paper (Moaaz Siddiq file)
How many input and output do half adder contain (2 marks)
Decoder (2 marks) lec #16
Implement for segment a = A+C+BD+ (3 Marks) [BCD to 7- sement Decoder] p#162
Write in hexadecimal…. (3 marks)
a)0100100
b)10011100
c)101010111
Tri state buffer (Draw tri state buffer in high-impedence) (5 marks) lec#20
Give is the circuit diagram of 4-bit comparator circuit formed by cascading 2 bit comparator (same as HASSAAN KHAN Question. Explain the working of circuit (5 marks)

MY TODAY paper
Mcqs from past papers
Q: why we use BCD (2)

Q: Modes of PALs (2)
Q: from K-map build any equation (K-map is given) (3)
Q: In tri state buffer describes different ways to connect control line ? (3)
Q: Full Adder Table (5)
Q:NOR gate based S_R Latch table (5)

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today at 10.30 am
50% mcqs were from past papers
1) how can we use adder circuit for subtraction?
2) diff b/w BCD to 7-segment and binary decoder?
3) boolean expression with 2bit comparator
4) Draw NOR gate based S_R Latch?
forgot the rest :p
enjoy ppl :)

My today paper
MCQS ye waly new thy baqi moaz ki file sy thy
1:110/10= _____
11,10,101,111
2:The simplest ande most commonly used Decoder are _____
n to 2n, (n-1)to(2n-1),n to 2n-1
3: The capability that allows the PLDs to be progrmmed after they have been circuit based is called REPM , ISP , ICP , EEPM
4: A Quad 1 to 4 Mux has _____
3 , 4 , 2 , 1
5: Addition of octal no 36 and 71 is _____
213 , 123 , 127 , 345
6: The basic building block for a logic circuit is
Logic Gate , Flip Flop , An Adder , A comparator
Subjective
Nor 5- latch wala tha ai circuit draw karna tha
Name And explain two major use of decoder circuit?
(A+C).(C+D).(B+C+D) State whether SOP or POS?

>>>> MY tODAY CS302 PAPER <21-12-2013 2PM
1.HOW CAN WE USE ADDER CIRCUIT FOR PERFORMING SUBTRACTION? 2
2. NAME ANY TWO MODELS IN WHICH PALS ARE PROGRAMMED. 2
3. FOR A TWO BIT COMPARATOR PROGRAMED.SPECIFY ALL THE INPUTS FOR WHICH THE OUTPUT IS A=B IS SET TO ZERO. 3.
4. DRAW THE CIRCUIT DIAGRAM OF NAND BASED SR LATCH. 3
5. SIMPLIFY BOOLEAN EXPRESSION (A+B) (A+B)' (A+B)' (A'+B')' 5
6. DRAW BLOCK DIAGRAM OF PAL .5

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please solve these mcqs
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7 mcqs from moaz file, rest were logical
subjective were
1. modes of pal
2. NOR gate based S_R Latch table
3. full adder fucntion table
4, which gate is comparator?

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my today papr :
20 mcqs mostly past paper and mostly mcqs in moaz past paprs
6 question
s-r latch NOR truth table
sop k map and simplicaion boolean expresion finding in truth table format
tri buffer diffrent three control line.
oor forget :(
