

CS302-Digital Logic and Design

Solved MCQS for Midterms papers

Solved by JUNAID MALIK and Team



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LMS Handling

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- 1) SRS
(Software Requirement's
Specification)
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- 3) Test phase + viva
- 4) Viva preparation
- 5) Final Deliverable

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1. Which of the following is a volatile memory?

1. PROM
2. DRAM
3. EPROM
4. EEPROM

2. _____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

1. Combinational Input/output
2. Combinational Output
3. Combinational Input
4. Programmable polarity

3. The AND Gate performs a logical _____ function.

1. Addition
2. Subtraction
3. Multiplication
4. Division

4. The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacent 1s are detected in the input, the output is set to high.

1. 2
2. 4
3. 1
4. 0

5. In the keyboard encoder, how many times per second does the ring counter scan the key board?

1. 600 scans/second
2. 625 scans/second

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3. 650 scans/second

4. 700 scans/second

6. The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

1. Slow

2. Faster

3. Medium

4. Modern

7. GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

1. column, row

2. row, column

3. column, column

4. row, row

8. Which of the following Output Equations determines the output of the State Machine?

1. $MIN = Q0Q1$

2. $MAX = Q0Q1EN$

3. $MIN = Q0Q1EN$

4. $MAX = Q1EN$

9. The maximum value, represented by a single hexadecimal digit is _____.

1. "E"

2. "F"

3. "G"

4. "H"

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10. If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

1. 0

2. 1

11. The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

1. Low

2. High

3. Medium

4. Hot

12. DE Morgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

1. Negative-OR, Negative-AND

2. Negative-AND, Positive-OR

3. Positive-OR, Negative-AND

4. Positive-OR, Positive-AND

13. Two signals _____ and _____ provide the timing inputs to the State Machine.

1. NSSR and EWSR

2. LTIME and STIME

3. PTIME and QTIME

4. NSGrn and NSYel

14. The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

1. 2

2. 4

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3. 6

4. 8

15. PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

1. PLAs

2. PALs

3. PLDs AL-JUNAID INSTITUTE OF GROUP

4. EPROM

16. The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

1. CONSTATE

2. FLOOR

3. MOTION

4. OPEN

17. Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.

1. Shift Registers

2. Circular Buffers

3. Ring Buffers

4. Reduce Registers

18. The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

1. Sequential

2. Asynchronous

3. Synchronous AL-JUNAID INSTITUTE OF GROUP

4. Combinational

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19. For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.

1. 111
2. 110
3. 010
4. None of the given

20. The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

1. AND, NOR
2. AND, NOT
3. AND, OR
4. XOR, NAND

21. The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.

1. One
2. Two
3. Three
4. Four

22. In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

1. NOR, NAND
2. NAND, NOR
3. NOR, NOR
4. NAND, NAND

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23. Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.

1. 8 OR
2. 8 AND
3. 8 XOR
4. 8 NOR

24. 8-bit parallel data can be converted into serial data by using _____ multiplexer.

1. 4-to-2
2. 8-to-1
3. 4-to-4
4. 8-to-4

25. The _____ input overrides the _____ input.

1. Asynchronous, synchronous
2. Synchronous, asynchronous
3. Preset input (PRE), Clear input (CLR)
4. Clear input (CLR), Preset input (PRE)

26. A SOP expression can be implemented by an _____ combination of gates.

1. OR-XOR
2. AND-NAND
3. AND-OR
4. XOR-NOR

27. The 64-cell array organized as 8 x 8 cell array is considered

1. as an 64 byte memory
2. as a 16 byte memory

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3. as an 8 byte memory
4. as an 4 byte memory
- 28. The terminal count of a 4-bit binary counter in the UP mode is _____.**
1. 1100
2. 0011
3. 1111
4. 0000
- 29. A 3-variable karnaugh map has**
1. eight cells
2. three cells
3. sixteen cells
4. four cells
- 30. An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.**
1. Q output of all flip-flops to clock input of next flip-flops
2. Q' output of all flip-flops to clock input of next flip-flops
3. Q output of all flip-flops to J input of next flip-flops
4. Q' output of all flip-flops to K input of next flip-flops
- 31. Memory is arranged in _____.**
1. linear fashion
2. two-dimensional manner
3. three-dimensional manner
4. random fashion
- 32. If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.**
1. 1001
2. 0110

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3. 1111

4. 1100

33. Subtractors also have output to check if 1 has been

_____.

1. Primed

2. Shifted

3. Complemented

4. Borrowed

34. The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.

1. One

2. Two

3. Three

4. Four

35. A multiplexer with a register circuit converts

1. Serial data to parallel

2. Parallel data to serial

3. Serial data to serial

4. Parallel data to parallel

36. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

1. True

2. False

37. The n flip-flops store _____ states.

1. 1

2. 2^n

3. 0

4. $2^{(n+1)}$

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38. The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

1. two
2. four
3. eight
4. sixteen

39. Why demultiplexer is called a data distributor?

1. The input will be distributed to one of the outputs
2. The input will be selected for the output
3. The output will be distributed to one of the inputs
4. Single input to Single Output

40. When the transmission line is idle in an asynchronous transmission

1. It is set to logic low
2. It is set to logic high
3. It remains in previous state
4. State of transmission line is not used to start transmission

41. UVERPROM is stands for

1. Ultra-Variant
2. Ultra-Vibrant
3. Ultra-Voilet
4. Ultra-Visible

42. In memory write cycle, the time for which the WE signal remains active is known as the _____.

1. Write address setup
 2. Write pulse width
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3. Write delay width
4. Write data time
- 43. The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.**
 1. NOT
 - 2. AND**
 3. OR
 4. XOR
- 44. PALs tend to execute _____ logic.**
 1. SPD
 - 2. SOP**
 3. SAC
 4. SAP
- 45. The ROM used by a computer is relatively _____ as it stores few byres of code used to Boot the Computer system on power up.**
 - 1. Small**
 2. Large
 3. Heavy
 4. High
- 46. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?**
 1. CS
 - 2. WE**
 3. W
 4. OE
- 47. You have to choose suitable option when your timer will reset by considering this given code:**

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TRSTATE.CLK = clk;

TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);

1. NSY2 or EWY2
2. NSSR or TMRST
3. EWSR or NSRED
4. EWRed or EWYel

48. A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

1. XOR, NAND
2. NOR, XOR
3. NOR, NAND
4. OR, XOR

49. Implementation of Latch is required almost _____ transistor.

1. Two
2. Four
3. Six
4. Eight

50. In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

1. 4.8 microsec
2. 5.9 microsec
3. 7.8 microsec
4. 5.5 microsec

51. The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

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1. AND
2. NAND
3. OR
4. NOT

52. For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1. 0
2. 1
3. x (don't care condition)
4. Any of given option depending on SOP term

53. Select the mode of programming in which GAL16V8 can be programmed:

1. Simple Mode
2. Complex Mode
3. Registered Mode
4. All of the given

54. Divide-by-32 counter can be achieved by using

1. Flip-Flop and DIV 10
2. Flip-Flop and DIV 16
3. Flip-Flop and DIV 32
4. DIV 16 and DIV 32

55. The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.

1. REQ0
2. OPEN
3. REQ1
4. FLOOR1

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56. Consider $A=1$, $B=0$, $C=1$. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

1. Zero
2. One
3. Undefined
4. No output as input is invalid

57. A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1. 0001
2. 1000
3. 1110
4. 1111

58. Adding two octal numbers "36" and "71" result in _____.

1. 213
2. 123
3. 127
4. 345

59. The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

1. Truth Table
2. State Diagram
3. Karnaugh Map
4. Logic Circuit

60. The domain of the expression $AB'CD + AB' + C'D + B$ is

1. A and D
2. B only

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3. A, B, C and D

4. None of the given

61. If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

1. Different

2. Same

3. Equal

4. Opposite

62. In DRAM read cycle R /W- signal is activated to read data which is made available on the _____ data line.

1. D(IN)

2. D(OUT)

3. D(AB)

4. D(INT)

63. In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

1. True

2. False

64. Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.

1. RAM AL-JUNAID INSTITUTE OF GROUP

2. ROM

3. PPRM

4. Flash Memory

65. As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.

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1. Bottom
2. Top
3. Down
4. Vertex

66. Which one flip-flop has an invalid output state?

1. T
2. JK
3. SR
4. D

67. The output of a NAND gate is _____ when all the inputs are one.

1. Zero
2. One
3. Available
4. Not available

68. The Transition table is very similar to the _____ table.

1. Truth
2. State
3. Transition
4. None of the given

69. Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

1. 64
2. 128
3. 256
4. 512

70. Canonical form is a unique way of representing _____.

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1. SOP

2. Minterm

3. Boolean Expression

4. POS

71. _____ Counters as the name indicates are not triggered simultaneously.

1. Asynchronous

2. Synchronous

3. Positive-Edge triggered

4. Negative-Edge triggered

72. C_{in} is part of _____ Adder.

1. Half

2. Full

3. Single

4. Double

73. Flash memory Operation are classified into _____ different operation.

1. Two

2. Three

3. Four

4. Five

1. A Product term is 0 when _____

a. Any one literal is 0

b. Any of the literals is 1

c. At least two literals are 1

d. All the literals are 1

2. In 8-input multiplexer, the two outputs are connected through a/an _____ gate.

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a. AND

5. OR AL-JUNAID INSTITUTE OF GROUP

b. NOT

c. NOR

3. ____ Device dissipate varying amount of power depending upon the frequency of operation.

a. TTL

b. CMOS

c. Storage

d. Peripheral

4. Boolean Addition operation is performed by a(an)____ gate.

a. AND

b. OR

c. XOR

d. NAND

5. A SOP expression can be implemented by an____ combination of gates.

a. OR-XOR

b. AND-AND

c. AND-OR

d. XOR-NOR

6. The maximum decimal number that can be represented using the 64-bit unsigned representation is _____.

a. 2^{63}

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- b. $(2^{64})-1$**
- c. $(2^{64}+$
- d. 2^{64}
7. In 16-bit ALU, The G output is activated if the 4-bit unit generate a Carry ____ irrespective of Carry ____.
- a. In,In
- b. In,Out
- c. Out,In**
- d. Out,Out
8. A standard POS form has ____ terms that have all the variables in the domain of the expression.
- a. Sum**
- b. Product
- c. Min
- d. Composite
9. In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles ____.
- a. Lower priority outputs
- b. Higher priority outputs
- c. Lower priority inputs**
- d. Higher priority inputs
10. Which of the following is the example of comparator?
- a. OR
- b. AND
- c. XOR

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d. XNOR

11. IN CMOS 5 Volt series, Input voltage of Logic high signal (V_{IH}) with a ranges from ____ to ____ volts.

- a. 4,5,5
- b. 0,5
- c. 0,3,5

d. 3,5,5

12. The Adjacent 1 S Detector accepts 4-bits input. If ____ adjacent 1S are detected in the input, the output is set to high.

- a. 2
- b. 4**
- c. 1
- d. 0

13. DE Morgan's two theorems prove the equivalency of the NAND and ____ gates and the NOR and ____ gates respectively.

a. Negative-OR, Negative-AND

b. Negative-AND, Negative-OR

c. positive-OR, Negative-AND

d. positive-AND, Negative-OR

14. Adding two octal numbers "36 and 71" result in ____.

- a. 213
- b. 123
- c. 127**
- d. 345

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15. Any of the ____ forms of the Karnaugh Map can be used to simplify Boolean expressions

- a. Three
- b. Four
- c. Two**
- d. Five

16. Quine-McCuskey and K-Map methods are used for ____ of Boolean expression.

- a. Multiplication
- b. Addition

6. Simplification AL-JUNAID INSTITUTE OF GROUP

- c. Subtraction

17. The number "1259" may belong to ____ number system.

- a. Binary number system
- b. Octal or Decimal system
- c. Decimal or Hexadecimal system**
- d. Binary or Hexadecimal system

18. The series of TTL chips are characterized by their ____.

- a. Switching Speed only**
- b. Power Dissipation only
- c. Both
- d. None of these

19. All ABEL statements must end with ____.

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- a. :
- b. ,
- c. ;**
- d. “
20. In sequential circuit memory elements are connected with ____.
- a. Logical circuit
- b. Clock**
- c. Feedback path
- d. External Event
21. In the 32-bit Single Precision Floating Point format, the exponent value ____ is reserved to represent infinity exponents.
- a. 98
- b. 99
- c. 255**
- d. 256
22. The ____ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.
- a. Combinational
- b. Combinational input/
- c. PLA**
- d. None
23. The limitation in implementation of parallel binary address is known as ____.
- a. Delay
- b. Carry propagation
- c. Carry input**

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d. Carry output

24. The Gray code is different from the unsigned binary code

because_____.

a. Successive value of Gray code by only one bit

b. Gray code is positional code

c. Gray code not support negative values

d. Gray code ranges from "0" to "9"

25. Removing the NOT gate at the output of the NOR gate result in an_____.

7. OR gate AL-JUNAID INSTITUTE OF GROUP

a. NAND gate

b. AND gate

c. NOT gate

26. Portable devices that run on batteries use_____ circuit that have low power dissipation.

a. Series

b. Integrated

c. Parallel

d. Electric

27. The domain of the expression $AB'CD+B$ is

a. A and D

b. A,B,C and D

c. C and D only

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d. B only

28. _____ is a single input gate

a. AND

b. OR

c. NOT

d. XOR

29. To represent in digital value, the number of digit (0s and 1s) that represent a quantity is _____ to the range of values that are to be represented.

a. Equal

b. Greater

c. Lesser

d. Not equal

30. BCD code of 16 is _____.

a. 10001

b. 00010001

c. 00010111

d. 01110001

31. To determine the seven expressions for each of the seven outputs in 7-segment display, seven _____ variable Karnaugh Maps are used.

8. 3

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a. 4

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b. 5

c. 2

32. In Odd parity generator circuit which gate is used to detect parity errors?

a. OR

b. NOR

c. XOR

d. AND

33. A 3-variable Karnaugh map has

a. Eight cells

b. Three cells

c. Sixteen cells

d. Four cells

34. The measurable values generally change over a

a. Specified period

b. Discrete range

c. Time

d. Continuous range

35. ____ uses E2CMOS technology which is Electrically Erasable CMOS

instead of Bipolar technology and fusible links.

a. PAL

b. GAL

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- c. PLA
 - d. PROM
36. When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?
- a. 1000
 - b. 1001**
 - c. 1010
 - d. 1100
37. How many of enable inputs is(are) active-low in 74xx138 3 to 8 Decoder?
- a. One
 - b. Two
 - c. Three**
 - d. Four
38. The simplified expression using either of the two K-maps are_____.
- a. Similar
 - b. Different
 - c. Identical**
 - d. None-identical
39. Which of the following expression in the product of sums form?
- a. $(A + B)(C+D)$
 - b. $(AB)(CD)$

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c. $AB(CD)$

d. $AB+CD$

40. CMOS technology is characterized by low power dissipation with _____ switching speeds.

a. **Slow**

b. Fast

c. Average

d. Medium

41. GAL Two 2-bit comparator circuits can be connected to form single 4-bit comparator

a. **True**

b. False

42. High level Noise Margins (VNH) of CMOS 5 volt series circuits is _____

a. 0.2 V

b. 0.5 V

c. **0.9 V**

d. 3.3 V

43. The output of the expression $F=A+B+C$ will be Logic _____

when $A=0$, $B=1$, $C=1$. the symbol "+" here represents OR Gate

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- a. Undefined
- b. One**
- c. Zero
- d. 10(binary)
44. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.
- a. SET**
- b. RESET
- c. Clear
- d. Invalid
45. 3.3 v CMOS series is characterized by _____ and _____ as compared to the 5 v CMOS series.
- a. Low switching speeds, high power dissipation
- b. Fast switching speeds, high power dissipation
- c. Fast switching speeds, very low power dissipation (page61)**
- d. Low switching speeds, very low power dissipation
46. The binary value "1010110" is equivalent to decimal _____.
- a. 86**
- b. 87
- c. 88
- d. 89
47. The _____ Encoder is used as a keypad encoder.

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- a. 2-to-8 encoder
- b. 4-to-16 encoder
- c. BCD-to-Decimal

d. Decimal-to-BCD Priority

48. How many data select lines are required for selecting eight inputs?

- a. 1
- b. 2
- c. 3**
- d. 4

49. The Quad Multiplexer has _____ outputs

- a. 4**
- b. 8
- c. 12
- d. 16

50. Demultiplexer has

- a. Single input and single outputs.
- b. Multiple inputs and multiple outputs.

c. Single input and multiple outputs.

- d. Multiple inputs and single output.

51. The expression _____ is an example of Commutative Law for Multiplication.

- a. $AB+C = A+BC$
- b. $A(B+C) = B(A+C)$

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c. $AB=BA$

d. $A+B=B+A$

52. The look-ahead carry circuits_____

a. Add a 1 to complemented inputs

b. Reduce propagation delay

c. Increase ripple delay

d. Determine sign and magnitude

53. What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?

a. $B+C'D'+CD$

b. $B'+C'D'+CD$

c. $B+C'D'+C'D$

d. $B'+C'D'+CD'$

54. 2-input, 8-bit Multiplexer, by setting the S input to logic_____

the_____ inputs of both the multiplexers are selected.

a. Low

b. High, B

c. Low, C

d. Low, C

55. The maximum decimal number that can be represented using the

64-bit unsigned representation_____

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- a. 2^{63}
- b. $(2^{64})-1$
- c. $(2^{64})+1$
- d. 2^{64}
56. When two or more products terms are assumed by Boolean addition, the result is a _____
- a. POS
- b. SOP
- c. Boolean
- d. Simplified
57. Tri-State Buffer is a _____ gate with a control line that disconnects the
- a. OR
- b. AND
- c. NAND
- d. NOT
58. The 4-bits 2's complement representation of "7" is _____
- a. 0111
- b. 1111
- c. 1001
- d. 0110
59. _____ and _____ are the steps of the Quine-McCluskey.

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- a. Draw a table and make groups
 - b. Write binary codes and write SOP
 - c. Find prime implicants and select minimal set of the prime implicants.
 - d. None of the given
60. The binary number 1011,101 has an Integer part represented by _____ and a fraction part ____ separated by a decimal point.
- a. 1011,101
 - b. 101,1011
 - c. 101,1101
 - d. 10111,11
61. Subtractors also have output to check if 1 has been _____
- a. Primed
 - b. Shifted
 - c. Complemented
 - d. Borrowed
62. CMOS technology is characterized by low power dissipation with _____ switching speeds.
- a. Slow
 - b. Fast
 - c. Average
 - d. Medium
63. The _____ description is used to simulate the logic circuit and verify its operation.

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- a. Test file
 - b. Declaration
 - c. Logic
 - d. Test vector
64. How many outputs can an integrated circuit comparator have?
- a. One
 - b. Two
 - c. Three
 - d. Four
65. Which of the following is not the correct method of grouping?
- a. Along adjacent columns
 - b. On comers
 - c. Diagonally
 - d. Along adjacent rows
66. The output of the expression $F=A.B.C$ will be logic _____
when $A=1, B=0, C=1$.
- a. Undefined
 - b. One
 - c. Zero
 - d. No output as input is valid

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67. The _____ gate and _____ gate implementation connected at the B

input of the 4-bit Adder is used to allow complemented or Un-Complemented B input to be connected to the Adder input.

- a. AND,NOR
- b. AND,NOT
- c. AND,OR
- d. XOR,NAND

68. In the 32-bit Single Precision Floating point format, the exponent value _____ is reserved infinity exponent.

- a. 98
- b. 99
- c. 255
- d. 256

69. The Boolean expression $(AB'CS')$ is used

- a. A sum term
- b. A product term
- c. A literal term
- d. A max term

70. The product of an XOR gate is zero(0), when _____

- I. All the inputs are zero
- II. Any of the inputs is zero

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III. An of the inputs is one IV.

All the inputs are one

- a. I only
- b. IV only
- c. I and IV only
- d. II and III

71. _____ methods are used to Convert Decimal fractions to Binary.

- a. 1
- b. 2
- c. 3
- d. 4

72. To display the number___ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

- a. 19
- b. 29
- c. 39
- d. 49

73. The look-ahead carry circuits_____

- a. Add a 1 to complemented inputs
- b. Reduce propagation delay
- c. Increase ripple delay

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- d. Determine sign and magnitude.
74. If two numbers in BCD representation generate an invalid BCD number then the binary ___ is added to the result
- a. 1001
 - b. 0110**
 - c. 1111
 - d. 1100
75. Both the multiplexers are selected simultaneously when _____ is set to logic _____ in 2-inputs, 8-bit Multiplexer.
- a. G, Low
 - b. G, High
 - c. S, Slow
 - d. S, High
76. Function labels required to represent the input/output combinations for each segment in 7-segment display
- a. 5
 - b. 7**
 - c. 8
 - d. 10
77. Multiplexers are also known as _____
- a. Data distributors
 - b. Data selectors**
 - c. Data manipulators

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d. Data setters

78. The PLA can be programmed to give an output of constant

_____ or _____

a. 0,1

b. 1,2

c. 2,3

d. 0,0

79. C_{in} is part of _____ Adder.

a. Half

b. Full

c. Single

d. Double

80. The look-ahead carry circuits _____

a. Add 1 to complemented inputs

b. Reduce propagation delay

c. Increase ripple delay

d. Determine sign and magnitude

81. Which of the following gates has the output 1 if and only if at least one input is 1?

a. AND

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- b. NOR
- c. NAND
- d. OR

82. A sop expression can be implemented by on _____ combination of gates.

- a. OR-XOR
- b. AND-NAND
- c. AND-OR
- d. XOR-NOR

83. The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through _____ ALU units in 16-bit ALU.

- a. Two
- b. Four
- d. 9

91. Digital circuits operates with _____ voltage value(s)

- a. 1
- b. 2
- c. 3
- d. 4

92. Which of the following is the octal equivalent of 28 decimal numbers?

- a. 31
- b. 32

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c. 33

d. 34

93. In cascading Priority Encoders, the EO output is connected to the EI of the encoder which handles _____

a. Lower priority outputs

b. Higher priority outputs

c. Lower priority inputs

d. Higher priority inputs

94. To determine the seven expressions for each of the seven outputs in 7-segment display, seven _____ variable Karnaugh maps are used.

a. 3

b. 4

c. 5

d. 2

95. The output of a NAND Gate is _____ when all the inputs are one.

a. Zero

b. One

c. Available

d. Not available

96. The _____ is the slowest and consumes more power.

a. Standard TTL

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- b. Schottky TTL
 - c. Advanced Schokottky TTL
 - d. Low-Power Schottky TTL
97. The between expression $X-AB+CD$ represents
- a. Two Ors ANDed together
 - b. A 4-input AND gate
 - c. Two ANDs ORed together
 - d. An eclusive-OR
98. The expression $F-A+B+C$ describes the operation of three bits ___ Gate.
- a. OR
 - b. AND
 - c. NOT
 - d. NAND
99. Which one of the following is NOT a valid rule of Boolean Algebra?
- a. $A+1=1$
 - b. $A=A'$
 - c. $AA=A$
 - d. $A+0=A$
100. A 5-Variable Karnaugh map has
- a. Sixteen cells
 - b. Thirty two cells
 - c. Sixty four cells
 - d. None of these

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101. _____ is invalid number of cells in a single group formed by the adjacent cells K-map
- a. 2
 - b. 8
 - c. 12**
 - d. 16
102. In 32-bit Single –Precision floating point format representation the range of exponent value is from _____ to _____
- a. +127 to -126**
 - b. +127 to -254
 - c. +128 to -254
 - d. +256 to -255
103. _____ has the fastest switching speed and low power requirements
- a. Advanced low power schottky
 - b. Fast TTL
 - c. Standard TTL
 - d. Schottky TTL**
104. A standard sum term is equal to zero for only one combination of _____ values.
- a. Literal
 - b. Maximum
 - c. Variable**
 - d. None
105. NOR gate is form by connecting _____
- a. OR Gate and then NOT Gate**
 - b. NOT Gate and then OR Gate
 - c. AND Gate and then OR Gate
 - d. OR Gate and then AND Gate

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106. The output of an AND gate with three inputs, A, B, and C, is HIGH when _____.
- a. A=1, B=1, C=0
 - b. A=1, B=1, C=1**
 - c. A=1, B=0, C=1
 - d. A=0, B=1, C=1
107. The output of an exclusive-OR gate is HIGH if _____.
- a. All Input or Unequal**
 - b. All inputs are DON'T care
 - c. All inputs are HIGH
 - d. All inputs are low
108. On a Karnaugh map, grouping the 0s produces _____.
- a. A POS expression**
 - b. A SOP expression
 - c. AND-OR Logic
 - d. NAND-NOR Logic
109. The simplified expression is presented in a _____ format.
- a. Function Table**
 - b. Logic Table
 - c. Truth Table
 - d. Data Table
110. The boolean expression $X = AB + CD$ represents.
- a. two ors anded together
 - b. a 4-input and gate
 - c. two ands ored together**
 - d. an exclusive- or
111. Which of the following is the example of comparator?
- a. SPD
 - b. SOP**
 - c. SAC
 - d. SAP
112. The 4-variable K-Map has _____ rows and _____ columns of cells.
- a. 4,4**
 - b. 2,2
 - c. 3,3
 - d. 6,6
113. The switching speed of CMOS is now _____.
- a. competitive with TTL**

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- b. three times that of TTL
c. slower than TTL
d. twice that of TTL
114. Gray code of 8 is:
a. **1100**
b. 1000
c. 0100
d. 0000
115. The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms.
a. 12
b. **16**
c. 8
d. 4
116. Which circuit is used in 7-segments display?
a. **BCD Code**
b. Excess Code
c. Binary code
d. Gray code
117. The 4-bit 2's complement representation of "-7" is ____
a. 0111
b. 1111
c. **1001**
d. 0110
118. _____ integrated circuit technology can easily be damaged due to accumulated static charge.
119. Don't care conditions are marked as _____ in the output column of the function table
a. A
b. 1
c. **X**
d. 0
120. The digital circuits operate with which combination of values given below?
a. 0 volts, 0 volts
b. **+5 volts, 0 volts**
c. -5 volts, 0 volts

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- d. -5 volts, 0 volts
121. In 15 digit decimal floating point format, the biased exponent value _____ can be used to represent the number zero whatever the value of the mantissa.
- a. 00
 - b. 000
 - c. 0
 - d. 0000
122. The ANSI/IEEE Standard 754 defines a _____ Single-Precision Floating Point format for binary numbers.
- a. 16-bit
 - b. 32-bit
 - c. 64-bit
 - d. 8-bit
123. A function represented by an expression in _____ form can be readily programmed.
- a. Boolean
 - b. Standard POS
 - c. Standard SOP
 - d. Non-standard SOP
124. _____ is an essential part of sequential circuit.
- a. Clock
 - b. Memory element
 - c. JK flip flop
 - d. Multiplexer
125. The OR Gate performs a Boolean _____ function
- a. Multiplication
 - b. Addition
 - c. Subtraction
 - d. Division
126. The values that exceed the specified range can not be correctly represented and are considered as _____
- a. Carry
 - b. Parity
 - c. Overflow
 - d. Sign Value
127. which of the following is the hexadecimal equivalent of 28?
- a. 1A
 - b. 1C

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- c. 1B
d. 1D
128. To implement the decoder circuit, having _____ inputs and _____ outputs, function tables have to be drawn which represent the output status of each output line for all combinations of inputs.
- a. 3 and 8
 - b. 4 and 7**
 - c. 1 and 9
 - d. 5 and 6
129. The _____ Gate is used in applications where the output signal is a 1 when any one input is a 1.
- a. OR**
 - b. XOR
 - c. NOT
 - d. AND
130. "1101" in signed representation is equivalent to _____
- a. 13
 - b. -5**
 - c. 10
 - d. -10
131. The three fundamental gates are _____
- a. NOT, OR, AND**
 - b. AND, NANAD, XOR
 - c. NOT, NOR, XOR
 - d. OR, AND, NAND
132. In a 4-variable K-map, a 2-variable product term is produced by
- a. A 4-cell group of 0s
 - b. A 8-cell group of 1s
 - c. A 4-cell group of 1s**
 - d. a 2-cell group of 1s
133. _____ function tables are required to represent the input/output combinations for each segment in 7-segment display.
- a. 5
 - b. 7**
 - c. 10
 - d. 8
134. Suppose we want to transmit the data "10001101", and an "Even-Parity" bit scheme is used to detect errors, the parity bit added to this data will be _____

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- a. "0"
b. "1"
c. Both "0" and "1"
d. Parity bit is not needed in this case
135. A variable can have a _____ value.
a. 0
b. 0 or 1
c. 0 and 1
d. 1
136. Which one is true?
a. Power consumption of both CMOS and TTL depends on no. of gates in circuit.
b. Power consumption of CMOS is higher than TTL
c. Power consumption of TTL is higher than CMOS
d. Both TTL and CMOS have same power consumption
137. XOR is an abbreviation of _____.
a. Inclusive-OR
b. Extended-OR
c. Extendable-NOR
d. Exclusive-OR

138.

Inputs		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

This function table represents _____ Gate.

- a. NAND
b. AND
c. OR
d. XOR
139. Which of the following is the example of comparator?
a. AND
b. XOR
c. OR
d. XNOR

140. The output of an AND gate is one when _____.

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- a. Both inputs are 1
141. The decimal value “20” is equivalent to binary value _____.
- 10011
 - 11001
 - 00101
 - 10100
142. Boolean algebra is the _____ of Digital Systems.
- Science
 - Equation
 - Expression
 - Mathematics
143. In 15 digit decimal floating point format, the biased exponent value _____ can be used to represent the number infinity whatever the value of mantissa.
- 99
 - 98
 - 256
 - 255
144. The digital circuits operate with which combination of values given below?
- A=0, B=0, C=1, D=1
 - A=1, B=0, C=0, D=1
 - A=0, B=1, C=1, D=0
 - A=1, B=1, C=,0, D=0
145. A ___ is converted into a standard POS by using the rule AA=0.
- No-standard SOP
 - Non-standard POS
 - Simplified POS
 - Simplified SOP
146. $(A+B).(A+C)=$ _____
- A+BC
 - B+C
 - AC+B
 - AB+C
147. The PLDs are implemented having a general purpose structure based on ___ arrays
- AND+NANAD

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- b. AND-OR
c. XOR-NOR
d. OR-XOR
148. Each octal Number didgit can represent a ___ binary Number.
a. 2-bit
b. 3-bit
c. 4-bit
d. 7-bit
149. The output of any CMOS ___ series logic gate can be at logic high “1” or logic low “0”.
a. 3.3 and 5 volt
b. 5+ volt
c. 4.5 volt
d. 5 volt
150. A standard SOP from has ___ terms that have all the variables in the domain of the expression.
a. Sum
b. Max
c. Composite
d. Product
151. In caveman number system the value “2” is represented by Symbol _____.
a. “>”
b. “!”
c. “^”
d. “&”
152. The expression $F=A.B.C$ describes the Operating of three bits ___ Gate.
a. NAND
b. NOT
c. OR
d. AND
153. In CMOS 5 volts series, input voltage of logic high signal (V_H) with a range from ___ to ___ volts.
a. 0, 3.5
b. 4.5,5
c. 0,5
d. 3.5,5

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154. TTL based devices work with a DC supply of ___ volts.
- a. +5
 - b. 3.3
 - c. +10
 - d. +3
155. A function represented by an expression in ___ form can be readily programmed.
- a. Non-standard SOP
 - b. Standard SOP
 - c. Boolean
 - d. Standard POS
156. Sum term (Max term) is implemented using ___ gates.
- a. NOT
 - b. AND
 - c. NOR
 - d. OR