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How many possible outputs does a decoder of 3 inputs contain?

Answer ([Please click here to Add Answer](#))



How can we use 3-to-8 decoder to implement SOP expressions?

Answer ([Please click here to Add Answer](#))

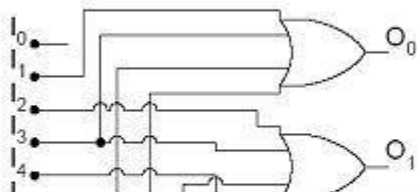


For a two bit comparator circuit, specify all the inputs for which $A > B$ is set to 1.

Answer ([Please click here to Add Answer](#))

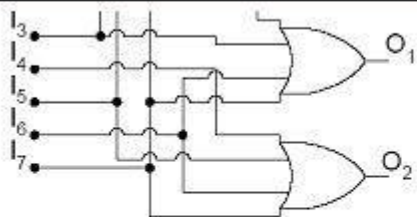


Identify the following circuit that is which combinational circuit is being represented by this diagram?



Answer ([Please click here to Add Answer](#))





Answer ([Please click here to Add Answer](#))



Consider a logical circuit for 4-bit binary number. The circuit gives output 0 for adjacent 0s in a binary number. Draw the karnaugh map of such circuit and derive simplified POS expression.

Answer ([Please click here to Add Answer](#))



Multiplexers can be used as a "Logic Function Generator". Draw only circuit diagram and function table based on three variables.

Answer ([Please click here to Add Answer](#))



How many possible outputs does a decoder of 3 inputs contain?

Answer ([Please click here to Add Answer](#))



Decoder, the 3-to-8 Decoder has active-low outputs and three extra NOT gates connected at the three inputs to reduce the four unit load to a single unit load. The 3-to-8 Decoder has three enable inputs, one of the three enable inputs is active-high and the remaining two are active-low. All three enable inputs have to be activated for the Decoder to work

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Once the Logic circuit design has been entered its operation is verified by using 'test vectors'. Write two major roles of test vectors.

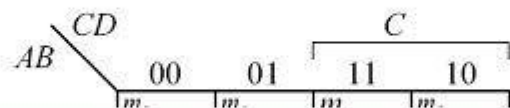
Answer ([Please click here to Add Answer](#))



The testing verifies the design of the logic circuit before committing it to the PLD. If any flaws are detected during the testing process the design must be debugged and submitted for recompilation. Once the design has been finalized a documentation file is produced along with a fuse map file which is downloaded to the programmer which programs the PLD device inserted in the programmer socket.

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Derive simplified Boolean equation from the following Karnuagh Map.



Answer ([Please click here to Add Answer](#))

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		C			
		00	01	11 10	
AB	00	m_0	m_1	m_3 1	m_2
	01	m_4	m_5	m_7 1	m_6

Answer ([Please click here to Add Answer](#))



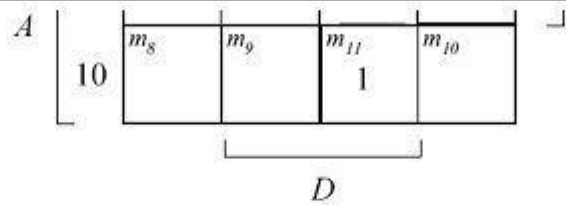
Normal Arial 12 B I U

$$A \begin{bmatrix} 11 \\ 10 \end{bmatrix} \begin{bmatrix} m_{12} & m_{13} & m_{13} & m_{14} \\ m_8 & m_9 & m_{11} & m_{10} \end{bmatrix} B$$

Answer ([Please click here to Add Answer](#))



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Answer ([Please click here to Add Answer](#))

Normal Arial 12 B I U

Tri-state buffer control input can be connected in four different ways. Name any three of them.

Answer ([Please click here to Add Answer](#))



Using Karnaugh map minimize the following POS expression:

$$(B + C + D)(A + B + \bar{C} + D)(\bar{A} + B + C + \bar{D})(A + \bar{B} + C + D)(\bar{A} + \bar{B} + C + D)$$

Answer ([Please click here to Add Answer](#))



A rich text editor toolbar with various icons for file operations (save, print, copy, paste), editing (undo, redo, bold, italic, underline), and formatting (bullet points, numbered lists, indent). It also includes a font dropdown menu showing 'Normal', 'Arial', and '12', and a zoom level dropdown set to '100%'.

Draw the function table of 8-to-3 Encoder.

Answer ([Please click here to Add Answer](#))



How many possible outputs does a decoder of 3 inputs contain?

Answer ([Please click here to Add Answer](#))



Write down four uses of multiplexers.

Answer ([Please click here to Add Answer](#))

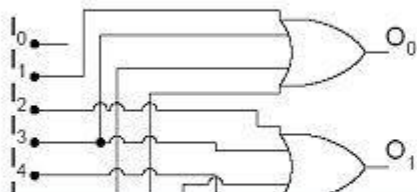


For a two bit comparator circuit, specify all the inputs for which the output $A = B$ is set to 1.

Answer ([Please click here to Add Answer](#))



Identify the following circuit that is which combinational circuit is being represented by this diagram?



Answer ([Please click here to Add Answer](#))



Map the following POS expression on a karnaugh map:

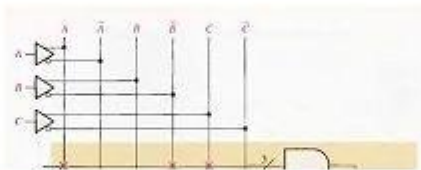
$$(\bar{A} + \bar{B} + C + D)(\bar{A} + B + \bar{C} + \bar{D})(A + B + \bar{C} + D)(\bar{A} + \bar{B} + \bar{C} + \bar{D})(A + B + \bar{C} + \bar{D})$$

Answer ([Please click here to Add Answer](#))



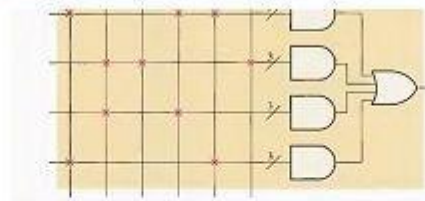
A rich text editor toolbar with various icons for file operations (save, print, copy, paste), editing (undo, redo, bold, italic, underline), and formatting (bullet list, numbered list, indent, outdent). It also includes a font face dropdown set to 'Arial', a font size dropdown set to '12', and a zoom level dropdown set to '100%'.

A programmed array is shown in Figure below. The intact fusible link, are indicated by small red Xs. Absence of an X means that the fuse is open. Analyze the figure below and write the output expression.



Answer ([Please click here to Add Answer](#))

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Answer ([Please click here to Add Answer](#))

Rich text editor toolbar with icons for file operations, editing, and formatting. The font is set to Arial, size 12. The zoom level is 100%.

How many input and output bits do a Half-Adder contain?

Answer ([Please click here to Add Answer](#))



Draw the Truth-Table of NAND based S-R Latch.

Answer ([Please click here to Add Answer](#))



Draw the block diagram of 4-bit BCD Adder.

Answer ([Please click here to Add Answer](#))



Tri-state buffer control input can be connected in four different ways. Name any three of them.

Answer ([Please click here to Add Answer](#))



Simplify the following Boolean expressions, using Boolean Algebraic rules

- $(A+B)(A+B')$
- $(A+B)'(A'+B)'$

Answer ([Please click here to Add Answer](#))



Multiplexers can be used as a "Logic Function Generator". Draw only circuit diagram and function table based on three variables.

Answer ([Please click here to Add Answer](#))

