



CS-302 Digital & Logical Design
Update MCQS For Quiz-1 File
Solve By Vu Topper RM



80 To 100% Marks



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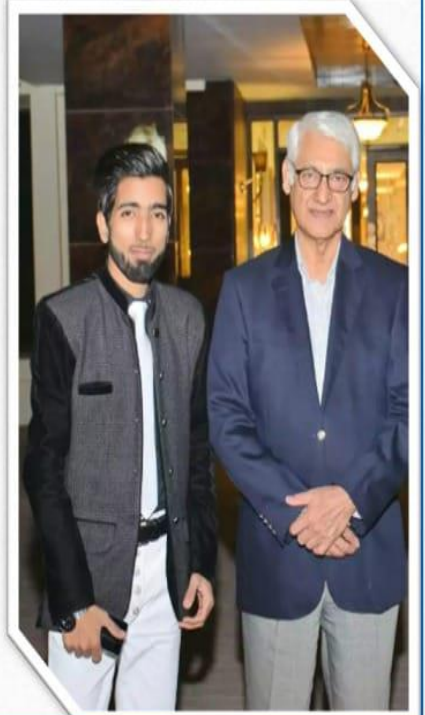
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Question No:1

(Marks:1)

Vu-Topper RM

Function tables are required to represent the input/output combinations for each segment in 7-segment display.

- A. One
- B. Two
- C. Five

D. Seven **Page 104**

Question No:2

(Marks:1)

Vu-Topper RM

The decimal value "20" is equivalent to binary value _____.

- A. 10100** **Google**
- B. 00110
- C. 11001
- D. 00111

Question No:3

(Marks:1)

Vu-Topper RM

Decimal number system is Base_____number system

- A. Two** **Page 5**
- B. One
- C. Five
- D. Eight

Question No:4

(Marks:1)

Vu-Topper RM

NOT gate is also known as an _____.

- A. Inverter circuit** **Google**
- B. Switch circuit
- C. Both
- D. None

Question No:5

(Marks:1)

Vu-Topper RM

A variable can have a _____ value.

- A. 0 or 1 value** **Page 71**
- B. 0 or 0 value

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- C. 1 or 0 value
- D. 0 and 1 value

Question No:6 (Marks:1) **Vu-Topper RM**
_____ come in different configurations they are identified by unique number

- A. PALs** Page 186
- B. PLAS
- C. DALs
- D. ADLS

Question No:7 (Marks:1) **Vu-Topper RM**
Arithmetic and Logic Units can perform any of the arithmetic operations and logic operations on _____ input values.

- A. One
- B. Two** Page 147
- C. Four
- D. Three

Question No:8 (Marks:1) **Vu-Topper RM**
A _____ output can change from one state to the other by applying appropriate inputs.

- A. Latch** Page 211
- B. Logic
- C. Analog
- D. None of these

Question No:9 (Marks:1) **Vu-Topper RM**
When the error condition is not detected in BCD adder, the circuit output is 0 and the 2nd Adder input B is set to _____.

- A. 0000** Page 142
- B. 1111
- C. 0011

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D. 1100

Question No:10 (Marks:1) **Vu-Topper RM**

A _____ attached to the Select inputs of the Demultiplexer routes the incoming serial bits to successive outputs where each bit is stored.

- A. Data
- B. Buffer
- C. Memory

D. A counter Page 178

Question No:11 (Marks:1) **Vu-Topper RM**

The _____ allows both its AND Gate array and the OR gate array to be programmed independently.

- A. PLA** Page 188
- B. DLA
- C. LPS
- D. PAL

Question No:12 (Marks:1) **Vu-Topper RM**

In 16-bit ALU, the Carry outputs C1, C2 and C3 from the Look-Ahead Carry generator circuit are generated after a gate delay of _____.

- A. 2** Page 151
- B. 4
- C. 3
- D. 1

Question No:13 (Marks:1) **Vu-Topper RM**

The GAL16V8 has eight _____ each connected to eight product terms.

- A. OLMCs** Page 200
- B. LMDS
- C. PLDS
- D. MNLS

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Question No:14

(Marks:1)

Vu-Topper RM

In 1-to-4 demultiplexer, how many select lines are required

- A. 1 select lines
- B. 2 select lines**
- C. 3 select lines
- D. 4 select lines

Page 396

Question No:15

(Marks:1)

Vu-Topper RM

In the Iterative Circuit for $A > B$, the output of Module 0 is 1 when

- A. $A > B$ of Module 1 is 1**
- B. $B > A$ of Module 1 is 1
- C. $A = B$ of Module 1 is 1
- D. $A - B$ of Module 1 is 1

Page 155

Question No:16

(Marks:1)

Vu-Topper RM

A circuit that converts the n inputs to 2^n outputs is called_____.

- A. Decoder**
- B. Shifter
- C. Encoder
- D. Comparator

Google

Question No:17

(Marks:1)

Vu-Topper RM

The Decimal-to-BCD Encoder has _____ outputs

- A. Two
- B. Ten**
- C. Four
- D. Five

Page 166

Question No:18

(Marks:1)

Vu-Topper RM

In a Digital System, Binary data is used and represented in_____.

- A. Static
- B. Serial
- C. Variable

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D. Parallel Page 175

Question No:19 (Marks:1) Vu-Topper RM

The absence of a _____ element in sequential circuit restricts the use of digital combinational circuits to certain application areas.

A. Memory Page 210

- B. Logic
- C. Both
- D. None

Question No:20 (Marks:1) Vu-Topper RM

The BCD to 7-Segment Decoder unlike the Binary Decoders activates multiple but unique set of outputs for each _____ BCD input combination.

- A. 1-bit
- B. 2-bit
- C. 3-bit

D. 4-bit Page 1

Question No:21 (Marks:1) Vu-Topper RM

In look ahead circuits G stands for _____.

- A. Carry Input
- B. Carry Output
- C. Carry Propagate

D. Carry Generator Page 150 and 151

Question No:22 (Marks:1) Vu-Topper RM

When the fuse of the _____ gate input is blown to set the input to logic high, the output of the XOR gate is opposite of the OR gate output.

- A. OR
- B. XOR Page 186**
- C. AND
- D. NAND

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Question No:23

(Marks:1)

Vu-Topper RM

Combinational Logic is used for combinational circuits, where as Registered Logic is based on -----circuits.

A. 4 Wire Page 194

B. 3 Wire

C. 2 Wire

D. 1 Wire

Question No:24

(Marks:1)

Vu-Topper RM

The 4-bit ALU (74XX381) only has three function select inputs allowing only ____ different arithmetic and logic functions.

A. 8 Page 147

B. 6

C. 4

D. 2

Question No:25

(Marks:1)

Vu-Topper RM

Which of the following is the MSI version of the Look-Ahead Carry Generator, which provides identical inputs and outputs except for the C4 output?

A. 74XX182 Page 151

B. 47xx182

C. 182XX74

D. 74XX183

Question No:26

(Marks:1)

Vu-Topper RM

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

A. OR

B. AND Page 182

C. XOR

D. NAND

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Question No:27

(Marks:1)

Vu-Topper RM

Each Octal Number digit can represent a _____ Binary Number

A. 3 Bit Page 31

B. 4

C. 5

D. 6

Question No:28

(Marks:1)

Vu-Topper RM

The simplified expressions using either of the two K-maps are-----?

A. Logical

B. Physical

C. Identical Page 89

D. None of these

Question No:29

(Marks:1)

Vu-Topper RM

The _____ gate and _____ gate implementation connected at the B input of the 4bit Adder

A. AND and OR Page 146

B. XOR and And

C. NOT and OR

D. NAND and XOR

Question No:30

(Marks:1)

Vu-Topper RM

In 16-Input Multiplexer, the four outputs are connected together through a 4-input _____ gate.?

A. OR Page 171

B. AND

C. XOR

D. NAND

Question No:31

(Marks:1)

Vu-Topper RM

_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

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- A. 12** **Google**
B. 10
C. 14
D. 16

Question No:32 **(Marks:1)** **Vu-Topper RM**
XOR is an abbreviation of-

- A. Exclusively-OR** **Google**
B. Exclusively-AND
C. Exclusively-XOR
D. Exclusively-NAND

Question No:33 **(Marks:1)** **Vu-Topper RM**
When the control line in tri-state buffer is high, the buffer operates like a _____ gate

- A. OR
B. AND
C. NOT **Page 196**
D. XOR

Question No:34 **(Marks:1)** **Vu-Topper RM**
The expression $F=A.B.C$ describes the operation of three bits ____ Gate.

- A. OR** **Google**
B. AND
C. XOR
D. NAND

Question No:35 **(Marks:1)** **Vu-Topper RM**
How many sets of AND-OR based circuit are used to allow complemented and un-complemented B input to be applied at the B inputs of the two 4-bit Adders?

- A. One
B. Two **Page 146**

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- C. Five
- D. Four

Question No:36

(Marks:1)

Vu-Topper RM

The product terms in Standard SOP are called _____

A. Minterms

Page 85

- B. Minimum
- C. Maximum
- D. Manterms

Question No:37

(Marks:1)

Vu-Topper RM

In 8-input multiplexer, when ___ is set to 0, the first multiplexer is selected allowing its inputs 1C0, 1C1, 1C2 and 1C3 to be selected.

- A. B
- B. C**
- C. D
- D. A

Page 170

Question No:38

(Marks:1)

Vu-Topper RM

Basic function of a Comparator is to _____ two binary quantities.

- A. Different
- B. Compare**
- C. Both
- D. None of these

Page 153

Question No:39

(Marks:1)

Vu-Topper RM

How many of enable inputs is(are) active-low in 74XX138 3-to-8 Decoder?

- A. One
- B. Two
- C. Four
- D. Three**

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Question No:40

(Marks:1)

Vu-Topper RM

A Karnaugh Map is organized in the form of a(an)_____.

A. Array **Page 89**

- B. Method
- C. Function
- D. Data Type

Question No:41

(Marks:1)

Vu-Topper RM

The _____ Gate is used in circuits to generate the 1's Complement of a number by inverting all its bits.

- A. OR
- B. AND
- C. NOT**
- D. XOR

Page 44

Question No:42

(Marks:1)

Vu-Topper RM

The OR Gate performs a Boolean_____function

- A. Addition** **Page 22**
- B. Subtraction
- C. Both
- D. None of these

Question No:43

(Marks:1)

Vu-Topper RM

The expression $F=A+B+C$

- A. OR**
- B. AND
- C. NOT
- D. NAND

Question No:44

(Marks:1)

Vu-Topper RM

In Caveman number system, the value "2" is represented by symbol

A. > **Page 11**

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- B. <
- C. =
- D. @

Question No:45 (Marks:1) **Vu-Topper RM**
A standard SOP form has _____ terms that have all the variables in the domain of the expression.

A. Sum Page 85

- B. Both
- C. None
- D. Product

Question No:46 (Marks:1) **Vu-Topper RM**
The 4-bit 2's complement representation of "-7" is _____

A. 1001 Page 23

- B. 0011
- C. 0010
- D. 1111

Question No:47 (Marks:1) **Vu-Topper RM**
The AND Gate performs a logical _____ function.

A. Multiplication Page 40

- B. Different
- C. None
- D. Both

Question No:48 (Marks:1) **Vu-Topper RM**
The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacent 1s are detected in the input, the output is set to high.

- A. 1
- B. 2 Page 123**
- C. 3
- D. 4

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Question No:49

(Marks:1)

Vu-Topper RM

In 16-input multiplexer, the decoder inputs _____ and _____ enable one out of the four multiplexers.

A. C and D

Page 171

- B. A and B
- C. B and A
- D. A and D

Question No:50

(Marks:1)

Vu-Topper RM

8-bit parallel data can be converted into serial data by using _____ multiplexer

A. 8-to-1

Page 175

- B. 8-to-0
- C. 1-to-8
- D. 0-to-8

Question No:51

(Marks:1)

Vu-Topper RM

The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through _____ ALU units in 16-bit ALU.

A. Four

Page 150

- B. One
- C. Two
- D. Three

Question No:52

(Marks:1)

Vu-Topper RM

A SOP expression having a domain of 3 variables will have a truth table having _____ combinations of inputs and corresponding output values.

A. 4

Page 87

- B. 3
- C. 2
- D. 1

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Question No:53

(Marks:1)

Vu-Topper RM

The _____ is the slowest and consumes more power.

A. Standard TTL Page 61

B. Simple LTT

C. None

D. Different TTL

Question No:54

(Marks:1)

Vu-Topper RM

The output of a NAND gate is _____ when all the inputs are one.

A. 1 Page 47

B. 2

C. 3

D. 4

Question No:55

(Marks:1)

Vu-Topper RM

If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

A. Different Page 1

B. Between

C. Both

D. None of these

Question No:56

(Marks:1)

Vu-Topper RM

Canonical form is a unique way of representing _____.

A. SOP Page 117

B. POS

C. SUM

D. PRODUCT

Question No:57

(Marks:1)

Vu-Topper RM

In 16-bit ALU, the G output is activated if the 4-bit unit generates a _____ irrespective of _____.

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- A. Carry in, carry out
- B. Carry out, carry in**
- C. Input number, carry in
- D. Carry in, input number

Page 150

Question No:58

(Marks:1)

Vu-Topper RM

Any of the _____ forms of the Karnaugh Map can be used to simplify Boolean expressions

- A. 2**
- B. 3
- C. 4
- D. 5

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Question No:59

(Marks:1)

Vu-Topper RM

The _____ enable input of the decoder when set to 1 disables the decoder and the multiplexers.

- G**
- Page 171**
- B
- A
- S

Question No:60

(Marks:1)

Vu-Topper RM

A specific half-adder has _____ inputs and _____ output(s).

- A. 2.2**
- B. 3.3
- C. 4.2
- D. 3.5

Google

Question No:61

(Marks:1)

Vu-Topper RM

The _____ input selects/deselects both the decoders simultaneously.

- A. Enable**
- B. Disable
- C. Active high

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D. Active low

Question No:62

(Marks:1)

Vu-Topper RM

All ABEL statements must end with_____.

A. ; Page 203

B. @

C. :

D. #

Question No:63

(Marks:1)

Vu-Topper RM

Removing the NOT gate at the output of the NOR gate results in an

_____.

A. OR gate

Page 50

B. AND

C. XOR

D. NOT

Question No:64

(Marks:1)

Vu-Topper RM

In Odd parity generator circuit which gate is used to detect parity errors?

A. XOR

Page 132

B. AND

C. XOR

D. NAND

Question No:65

(Marks:1)

Vu-Topper RM

When the number 29 is represented on 7-segment display, which BCD input is represented on LSD display unit?

A. 1001

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B. 0011

C. 1100

D. 0101

Question No:66

(Marks:1)

Vu-Topper RM

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The expression _____ is an example of Commutative Law for Multiplication.

A. $AB=BA$

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B. $BA@AB$

C. $BA=AB$

D. $AB\#BA$

Question No:67

(Marks:1)

Vu-Topper RM

In a 4-variable K-map, a 2-variable product term is produced by

A. 4-cell group of 1s

B. a 8-cell group of 1s

C. a 2-cell group of 1s

D. a 4-cell group of 0s

Question No:68

(Marks:1)

Vu-Topper RM

The output of any CMOS series logic gate can be at logic high '1' or logic low '0'

A. 3.3 and 5volt

B. 2.2 and 5volt

C. 1.1 and 5volt

D. 3.2 and 5volt

Question No:69

(Marks:1)

Vu-Topper RM

$1011 - 101 =$

A. 0110

B. 0011

C. 1100

D. 0101

Question No:70

(Marks:1)

Vu-Topper RM

$(A+B).(A+C)=$

A. $AC+B$

B. $AB=C$

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- C. $BC=D$
- D. $AB+B$

Question No:71 (Marks:1) **Vu-Topper RM**

_____ and _____ are the steps of the Quine-McCluskey.

- A. Draw a table and make groups.
- B. Write binary codes and write SOP.
- C. Write binary codes and write POS.

D. Find prime implicants and select minimal set of the prime implicants.

Question No:72 (Marks:1) **Vu-Topper RM**

K-Map is difficult to manage for _____ or more variables.

- A. 3
- B. 5
- C. 7** **Google**
- D. 9

Question No:73 (Marks:1) **Vu-Topper RM**

In 32-bit Single –Precision floating point format representation the range of exponent value is from _____ to _____

- A. +127 to -126**
- B. -126 to 127
- C. +125 to 126
- D. -127 to +128

Question No:74 (Marks:1) **Vu-Topper RM**

The output of the expression $F=A.B.C$ will be logic _____ when

$A=1, B=0, C=1$.

- A. One
- B. Two
- C. Six
- D. Zero**

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Question No:75

(Marks:1)

Vu-Topper RM

The NOR logic gate is the same as operation of the.....gate with an inverter connected to the output

- A. OR
- B. AND
- C. NOT**
- D. NAND

Question No:76

(Marks:1)

Vu-Topper RM

The GAL22V10 device is available as low-voltage 3.0V

- 3.3V** **Page 194**
- 2.0V
- 1.5V

Question No:77

(Marks:1)

Vu-Topper RM

The active high and active low inputs of 3-to-8 Decoder are as follows

- A. All active low
- B. All active high
- C. One active high and two are remaining active low**
- D. Two active-high and the remaining one is active-low

Question No:78

(Marks:1)

Vu-Topper RM

The 16 input multiplexer the decoder input....and.....enable one out of four multiplexer

- A. C, D**
- B. A, C
- C. B, D
- D. A, B

Question No:79

(Marks:1)

Vu-Topper RM

The Programmable Array Logic (PAL) has _____ AND array

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and a _____ OR array.

A. Fixed, fixed

B. Programmable, fixed

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C. Fixed, programmable

D. Programmable, programmable

Question No:80

(Marks:1)

Vu-Topper RM

If odd-Parity is being used therefore the 4-bit data and the parity bit should add up to give _____ of 1s.

A. Prime

B. Add

Page 131

C. Both

D. Even

Question No:81

(Marks:1)

Vu-Topper RM

How many 74HC85s are cascaded together forms a 12-bit Comparator circuit?

A. 1

B. 4

C. 3

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D. 2

Question No:82

(Marks:1)

Vu-Topper RM

In 2-bit comparator the input combinations 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11 are for _____?cs302

A. $A > B$

B. $A = B$

C. $A < B$

Page 109

D. $A == B$

Question No:83

(Marks:1)

Vu-Topper RM

The based devolves with WC supply....vexes

A. +1

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- B. -2
- C. +3
- D. +5**

Question No:84

(Marks:1)

Vu-Topper RM

In 16-bit ALU, the Carry Out 16 is generated only when ALU3 has received Carry In ____.

- A. 6
- B. 8
- C. 10
- D. 12**

Page 150

Question No:85

(Marks:1)

Vu-Topper RM

Subtraction also have output check 1 has been

- A. Simple
- B. Difficult
- C. None
- D. Borrowed**

Question No:86

(Marks:1)

Vu-Topper RM

The data digit circuit operates with which contribution of value given blow

- A. +5volts and 0 volts**
- B. +1 volts and 5 volts
- C. -5volts and 0 volts
- D. *5volts and 0 volts

Question No:87

(Marks:1)

Vu-Topper RM

_____ single digit BCD Adders can be cascaded together to form a 2-digit BCD Adder.

- A. One
- B. Two**
- C. Four
- D. Three

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Question No:88

(Marks:1)

Vu-Topper RM

If $S=1$ and $R=0$ then for positive edge triggered flip flop

- A. 1**
- B. 2
- C. 3
- D. 4

Question No:89

(Marks:1)

Vu-Topper RM

The terminal count of 4 bit binary counter in the UP mode is.....

- A. 1001** **Page 288**
- B. 0011
- C. 1100
- D. 1010

Question No:90

(Marks:1)

Vu-Topper RM

For a gated D latch If $EN = 1$ and $D = 1$ then $Q(t+1) = \dots\dots$

- A. 1**
- B. 2
- C. 3
- D. 4

Question No:91

(Marks:1)

Vu-Topper RM

Which of the following expression is in the product-of-sums form?

- A. $AB(CD)$
- B. $AB+CD$** **Google**
- C. $(AB)(CD)$
- D. $(A + B)(C+D)$

Question No:92

(Marks:1)

Vu-Topper RM

Binary Decoders have _____ inputs and _____ outputs

- A. $2n$
- B. $2^n, n$** **Page 158**

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- C. $2n.n$
- D. n^2

Question No:93 (Marks:1) **Vu-Topper RM**

Addition of two decimal digits in BCD can be done through

- A. Full Adder
- B. BCD adder** **Page 141**
- C. Ripple Carry Adder
- D. Carry Look Ahead Genertor

Question No:94 (Marks:1) **Vu-Topper RM**

_____ have Buffers at the inputs which produce the

- A. PLA
- B. PAL** **Page 184**
- C. GAL
- D. EPROM

Question No:95 (Marks:1) **Vu-Topper RM**

Both the multiplexer are selected simultaneously when...is not to logic..... In 2 input 8 bit multiplexer

- A. S LOW**
- B. S HIGH
- C. C LOW
- D. C HIGH

Question No:96 (Marks:1) **Vu-Topper RM**

The primary use of multiplexers is _____.

- A. Data Router
- B. Operation sequencing
- C. Logic function generator
- D. Parallel to Serial Converter** **Page 172**

Question No:97 (Marks:1) **Vu-Topper RM**

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A standard interface for programming the In-System PLD consists of

A. 4 wires **Page 194**

- B. 2 wires
- C. 1 wires
- D. 3 wires

Question No:98

(Marks:1)

Vu-Topper RM

In 8 multiplexer the two output are connected though a gate

- A. OR
- B. AND**
- C. XOR
- D. NAND

Question No:99

(Marks:1)

Vu-Topper RM

The.....select input (S) of the 4 input multiplexer are common dual 4 input multiplexer

- A. One
- B. Two**
- C. Five
- D. Nine

Question No:100

(Marks:1)

Vu-Topper RM

Maxterm is the sum of.....of the corresponding monetary with its literal complemented

- A. Terms**
- B. SOP
- C. POS
- D. NONE

Question No:101

(Marks:1)

Vu-Topper RM

_____ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.

- A. PAL

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B. GAL Page 183

C. PLA

D. PROM

Question No:102

(Marks:1)

Vu-Topper RM

Any of the.....forms of the karnaugh map can be used to simplify Boolean expression

A. One

B. Two

C. Five

D. Four

Question No:103

(Marks:1)

Vu-Topper RM

What is the value of output adding of following binary number

1011+1110

A. 11001

B. 11001

C. 00110

D. 11101

Question No:104

(Marks:1)

Vu-Topper RM

The GAL22v10 is popular GAL having.....input and 10 input/output

A. 6

B. 8

C. 10

D. 12

Question No:105

(Marks:1)

Vu-Topper RM

To determine the seven expressions for each of the seven outputs in 7-segment display, seven ___-variable Karnaugh maps are used.

A. 3

B. 0

C. 2

D. 4

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Question No:106

(Marks:1)

Vu-Topper RM

A 3-variable Karnaugh map has

A. Eight cells

B. One cells

C. Two cells

D. Five cells

Question No:107

(Marks:1)

Vu-Topper RM

In gate SR latch what is the value of the output of $EN=1, S=0$ and $R=0$?

A. 1

B. 2

C. 3

D. 4

Question No:108

(Marks:1)

Vu-Topper RM

The limitation in implementation of parallel binary adders is known as .

A. Delay

B. Carry input

C. Carry output

D. Carry propagation

Question No:109

(Marks:1)

Vu-Topper RM

In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles _____.

A. Lower priority outputs

B. Higher priority outputs

C. Higher priority inputs

D. Lower priority inputs

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Question No:110

(Marks:1)

Vu-Topper RM

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We have a digital circuit Different parts of circuit operate at different clock frequencies (4MHZ,2MHZ and 1MHZ), but we have a single clock sources of circuit we can get help by using

A. J-k flip-flop

B. J-d flip-flop

C. k-j flip-flop

D. None of these

Question No:111

(Marks:1)

Vu-Topper RM

A Divide- by 20 counter can be achieved by using

A. Flip-Flop and DIV 10

B. Flip-Flop and DIV 12

C. Flip-Flop and DIV 14

D. Flip-Flop and DIV 16

Question No:112

(Marks:1)

Vu-Topper RM

In a 4-bit binary counter, the next state after the terminal count in the DOWN mode is _____

0000

Page 288

1111

0001

10000

Question No:113

(Marks:1)

Vu-Topper RM

For a gated D-latch if EN=1 and D=1 then $Q(t+1)=$

A. 1

B. 2

C. 3

D. 4

Question No:114

(Marks:1)

Vu-Topper RM

The ABEL symbol for “OR” operation is

A. #

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- B. @
- C. !
- D. *

Question No:115

(Marks:1)

Vu-Topper RM

The domain of the expression $AB'CD+AB'+CD+B$ is

- A. A, B
- B. B, C
- C. A, B, C
- D. A,B,C and D**

Question No:116

(Marks:1)

Vu-Topper RM

Boolean Addition operation is performed by a(n) _____ gate.

- A. OR**
- B. AND
- C. XOR
- D. NAND

Question No:117

(Marks:1)

Vu-Topper RM

The maximum decimal number that can be represented using the 64-bit unsigned represented is..

- A. $(2^{64})-1$**
- B. $(2^{65})-2$
- C. $(2^{64})-3$
- D. $(2^{65})-0$

Question No:118

(Marks:1)

Vu-Topper RM

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.

- A. 8 AND** **Page 123**
- B. 8XOR

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- C. 8 OR
- D. 8XOR

Question No:119

(Marks:1)

Vu-Topper RM

Is used when the output is connected back to the input of the PAL or if the output pin is used as a

- A. Input
- B. Output
- C. None of these

D. Combinational input/ output

Question No:120

(Marks:1)

Vu-Topper RM

The GAL22V10 is a popular device having inputs and ten inputs/outputs

- A. 10
- B. 12
- C. 14
- D. 16

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Question No:121

(Marks:1)

Vu-Topper RM

Power dissipation of device's remaining constant throughout their operation

- A. TTL
- B. LLL
- C. LTT
- D. TLT

Question No:122

(Marks:1)

Vu-Topper RM

In 8-input multiplexer, the two outputs are connected through a/an _____ gate.

- A. OR
- B. NOT
- C. AND
- D. XOR

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Question No:123

(Marks:1)

Vu-Topper RM

Digital circuits operate with voltage value (s).

A. 2

B. 3

C. 4

D. 5

Question No:124

(Marks:1)

Vu-Topper RM

How many data select lines are required for selecting eight inputs?

A. 1

B. 2

C. 3

Google

D. 4

Question No:125

(Marks:1)

Vu-Topper RM

High level Noise margins (VNH) of CMOS 5volt series circuit is

A. 3.3v

B. 2.3v

C. 3.3a

D. 3.1v

Question No:126

(Marks:1)

Vu-Topper RM

Both the multiplexers are selected simultaneously when _____ is set to logic _____ in 2-inputs, 8-bit Multiplexer.

A. S, Low

Page 171

B. S,High

C. G,Slow

D. G,High

Question No:127

(Marks:1)

Vu-Topper RM

The _____ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.

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A. Two **Page 168**

- B. One
- C. Five
- D. Three

Question No:128 **(Marks:1)** **Vu-Topper RM**

The PLA can be programmed to give an output of constant ____ or ____.

A. 2.3

B. 0.1 **Page 190**

- C. 0.0
- D. 1.2

Question No:129 **(Marks:1)** **Vu-Topper RM**

Tri-State Buffer is a _____ gate with a control line that disconnects the output from the input.

- A. OR
- B. AND

C. NOT **Page 196**

D. NAND

Question No:130 **(Marks:1)** **Vu-Topper RM**

Divide-by-32 counter can be achieved by using

A. Flip-Flop and DIV 10

B. Flip-Flop and DIV 16

C. Flip-Flop and DIV 32

D. DIV 16 and DIV 32

Question No:131 **(Marks:1)** **Vu-Topper RM**

The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)

A. (n raise to power 2)

B. (n raise to power 2 and then minus 1)

C. (2 raise to power n)

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D. (2 raise to power n and then minus 1)

Question No:132

(Marks:1)

Vu-Topper RM

A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

A. 1001

B. 1011

C. 0011

D. 1100

Question No:133

(Marks:1)

Vu-Topper RM

A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is _____

A. 0001

B. 1111

C. 1000

D. 1110

Question No:134

(Marks:1)

Vu-Topper RM

Divide-by-160 counter is achieved by using

Flip-Flop and DIV 10

Flip-Flop and DIV 16

DIV 16 and DIV 32

DIV 16 and DIV 10

Question No:135

(Marks:1)

Vu-Topper RM

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

A. 3

B. 7

C. 8

D. 15

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Question No:136

(Marks:1)

Vu-Topper RM

RCO stands for _____

- A. Reconfiguration Counter Output
- B. Ripple Counter Output
- C. Reconfiguration Clock Output
- D. Ripple Clock Output**

Question No:137

(Marks:1)

Vu-Topper RM

For a down counter that counts from (111 to 000), if current state is "101" the next state will be

- A. 111
- B. 110
- C. 010
- D. None of given options**

Question No:138

(Marks:1)

Vu-Topper RM

The 74HC163 is a 4-bit Synchronous Counter. it has.....data output pins

- A. 2
- B. 4** **Page 278**
- C. 6
- D. 8

Question No:139

(Marks:1)

Vu-Topper RM

_____ Counters as the name indicates are not triggered simultaneously

- A. Asynchronous**
- B. Synchronous
- C. Positive-Edge triggered
- D. Negative-Edge triggered

Question No:140

(Marks:1)

Vu-Topper RM

A synchronous decade counter will have _____ flip-flops

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- A. 2
- B. 3
- C. 4**
- D. 10

Question No:141

(Marks:1)

Vu-Topper RM

Karnaugh map is used in designing

- A. a clock a counter
- B. an UP/DOWN counter
- C. All of the above**

Question No:142

(Marks:1)

Vu-Topper RM

_____ is said to occur when multiple internal variables change due to change in one input variable

- A. Hold and Wait
- B. Clock Skew
- C. Race condition**
- D. Hold delay

Question No:143

(Marks:1)

Vu-Topper RM

An Astablemultivibrator is known as a(n) _____

- A. Oscillator**
- B. Booster
- C. One-shot
- D. Dual-shot

Question No:144

(Marks:1)

Vu-Topper RM

_____ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

- A. Race condition
- B. Clock Skew**
- C. Ripple Effect

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D. None of given options

Question No:145

(Marks:1)

Vu-Topper RM

The glitches due to "Race Condition" can be avoided by using a __

- A. Gated flip-flops
- B. Pulse triggered flip-flops
- C. Positive-Edge triggered flip-flops
- D. Negative-Edge triggered flip-flops**

Question No:146

(Marks:1)

Vu-Topper RM

An Asynchronous Down-counter is implemented (Using J-K flipflop) by connecting_____

- A. Q output of all flip-flops to clock input of next flip-flops
- B. Q' output of all flip-flops to clock input of next flip-flops**
- C. Q output of all flip-flops to J input of next flip-flops
- D. Q' output of all flip-flops to K input of next flip-flops

Question No:147

(Marks:1)

Vu-Topper RM

A decade counter is _____

- A. Mod-3 counter
- B. Mod-5 counter
- C. Mod-8 counter
- D. Mod-10 counter**

Question No:148

(Marks:1)

Vu-Topper RM

Don't care conditions are marked as _____ in the output column of the function table

X

Question No:149

(Marks:1)

Vu-Topper RM

An example of SOP expression is

both (a) and (b)

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Question No:150 (Marks:1) **Vu-Topper RM**
“1101” in signed representation is equivalent to _____
13

Question No:151 (Marks:1) **Vu-Topper RM**
In decimal value “275” the weight of the digit “7” is
100

Question No:152 (Marks:1) **Vu-Topper RM**
The decimal “10” will have an octal equivalent
12

Question No:153 (Marks:1) **Vu-Topper RM**
Caveman number system is Base _____ number system
A. 2
B. 5 **Page 11**
C. 10
D. 15

Question No:154 (Marks:1) **Vu-Topper RM**
When an Asynchronous sequential circuit changes two or more binary states variables a Condition occurs called _____
Race condition

Question No:155 (Marks:1) **Vu-Topper RM**
Time delay device is memory element of _____
Asynchronous circuits

Question No:156 (Marks:1) **Vu-Topper RM**
Boolean function must be brought into _____ To perform product of max terms
OR terms

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Question No:157

(Marks:1)

Vu-Topper RM

The binary number 10101 is equivalent to the decimal number_____.

21

Question No:158

(Marks:1)

Vu-Topper RM

The Boolean expression $A BC D$ is—

Sum term

Question No:159

(Marks:1)

Vu-Topper RM

The universal gate is_____.

NAND gate

Question No:160

(Marks:1)

Vu-Topper RM

According to Boolean algebra absorption law, which of the following is correct?

$xy+y=x$

Question No:161

(Marks:1)

Vu-Topper RM

A Boolean function may be transformed into

logical diagram

Question No:162

(Marks:1)

Vu-Topper RM

The inverter is _____

NOT gate

Question No:163

(Marks:1)

Vu-Topper RM

The resulting circuit of a NAND gate are connected together is_____

NOT gate

Question No:164

(Marks:1)

Vu-Topper RM

OR gate and _____ will form The NOR gate?

NOT gate

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Question No:165 (Marks:1) **Vu-Topper RM**
The NAND gate is AND gate followed by
NOT gate

Question No:166 (Marks:1) **Vu-Topper RM**
Max terms are also called _____.
Standard sum

Question No:167 (Marks:1) **Vu-Topper RM**
By the repeated use of _____ Digital circuit can be made
NAND gates

Question No:168 (Marks:1) **Vu-Topper RM**
The only function of NOT gate is _____ of the following.
Invert input signal

Question No:169 (Marks:1) **Vu-Topper RM**
Boolean algebra is defined as a set of _____.
two values

Question No:170 (Marks:1) **Vu-Topper RM**
If $S=1$ and $R=1$, for negative edge triggered flip-flop then $Q(t+1) =$
Invalid

Question No:171 (Marks:1) **Vu-Topper RM**
Adjacent 1s detector circuit will have active low output for the input
A. 1010
B. 1011
C. 0110

D. 1101 **Page 123**

Question No:172 (Marks:1) **Vu-Topper RM**

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The 3-to-8 Decoder has active-low outputs and three extra ____ gates connected at the three inputs to reduce the four unit load to a single unit load.

Not

Question No:173 (Marks:1) **Vu-Topper RM**
Adjacent 1s detector circuit will have active high output for the input.
0011 Page 123

Question No:174 (Marks:1) **Vu-Topper RM**
Modern information techniques are relying more on ____ transmission.
Digital

Question No:175 (Marks:1) **Vu-Topper RM**
Maxterm is the sum of _____ of the corresponding Minterm with its literal complemented.

A. Word

B. Terms

C. Nibble

D. Numbers

Question No:176 (Marks:1) **Vu-Topper RM**
Select the mode of programming in which GAL 16V8 can be programmed.

All of the given option

Question No:177 (Marks:1) **Vu-Topper RM**
_____ has the fastest switching speed and low power requirements.

A. Fast TTL

B. Standard TTL

C. Schottky TTL

D. Advanced low power Schottky

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Question No:178

(Marks:1)

Vu-Topper RM

$(A+B).(A+C)=$

AC+B

Question No:179

(Marks:1)

Vu-Topper RM

The minimum time for which the input signal has to be maintained at the input of flip-flop is called ____ of the flip-flop.

Hold time

Question No:180

(Marks:1)

Vu-Topper RM

Each stage of Master-slave flip-flop works at ____ of the clock signal.

One half

Question No:181

(Marks:1)

Vu-Topper RM

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using ____

NOT

Question No:182

(Marks:1)

Vu-Topper RM

The n flip-flops store ____ states.

2^n

Question No:183

(Marks:1)

Vu-Topper RM

When the ____ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of ____

1,2

Question No:184

(Marks:1)

Vu-Topper RM

A positive edge-triggered flip-flop changes its state when ____

Low-to-high transition of clock

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Question No:185

(Marks:1)

Vu-Topper RM

Which of the following is the octal equivalent of 28 decimal number?

A. 32

B. 34

C. 30

D. 28

Question No:186

(Marks:1)

Vu-Topper RM

The _____ input select/deselects both the decoders simultaneously.

Enable

Question No:187

(Marks:1)

Vu-Topper RM

NAND and _____ gates are known as Universal Gates.

NOR

Question No:188

(Marks:1)

Vu-Topper RM

The declaration section of ABEL generally includes the device declaration, _____ declarations and set declarations.

Pin

Question No:189

(Marks:1)

Vu-Topper RM

An SOP expression having a domain of 2 variables will have a truth table having _____ combinations of inputs and corresponding output values.

A. 2

B. 4

C. 6

D. 8

Question No:190

(Marks:1)

Vu-Topper RM

In the 32-bit Single Precision Floating formation, the exponent value _____ is reserved to represent 0 exponents.

0

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Question No:191

(Marks:1)

Vu-Topper RM

CMOS technology is characterized by low power dissipation with _____ switching speeds.

A. Slow

B. Fast

C. Medium

D. Average

Question No:192

(Marks:1)

Vu-Topper RM

The complement of a variable is always

A. 1

B. 0

C. equal to the variable

D. The inverse of the variable

Question No:193

(Marks:1)

Vu-Topper RM

$A(B + C) = A.B + A.C$ is the expression of _____.

Distributive Law

Question No:194

(Marks:1)

Vu-Topper RM

If the number 2025 is represented in floating point, then exponent is _____.

A. 1

B. 3

C. 5

D. 7

Question No:195

(Marks:1)

Vu-Topper RM

Excess-8 code of -6 is _____.

0010

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Question No:196
RM

(Marks:1)

Vu-Topper

A 3-variable Karnaugh map has
Eight cells

Question No:197

(Marks:1)

Vu-Topper RM

To represent in digital value, the number of digit (0s and 1s) that represents a quantity is _____ to the range of values that are to be represented.

Proportional

Question No:198

(Marks:1)

Vu-Topper RM

The expression $F=A+B+C$ describes the operation of three bits ___ Gate.
OR

Question No:199

(Marks:1)

Vu-Topper RM

GAL Two 2-bit comparator circuits can be connected to form single 4bit comparator

True

Question No:200

(Marks:1)

Vu-Topper RM

The output of the expression $F=A+B+C$ will be Logic _____ when $A=0, B=1, C=1$. the symbol "+" here represents OR Gate

One

Question No:201

(Marks:1)

Vu-Topper RM

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

SET

Question No:202

(Marks:1)

Vu-Topper RM

3.3 v CMOS series is characterized by _____ and _____ as compared to the 5 v CMOS series.

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Question No:203

(Marks:1)

Vu-Topper RM

The binary value "1010110" is equivalent to decimal _____

86

Question No:204

(Marks:1)

Vu-Topper RM

The _____ Encoder is used as a keypad encoder.

Decimal -to-BCD Priority

Question No:205

(Marks:1)

Vu-Topper RM

The Quad Multiplexer has _____ outputs

4

Question No:206

(Marks:1)

Vu-Topper RM

Demultiplexer has

Single input and multiple outputs.

Question No:207

(Marks:1)

Vu-Topper RM

The 4-bits 2's complement representation of "7" is _____

1001

Question No:208

(Marks:1)

Vu-Topper RM

The binary number 1011,101 has an Integer part represented by _____ and a fraction part ____ separated by a decimal point.

1011,101

Question No:209

(Marks:1)

Vu-Topper RM

The _____ description is used to simulate the logic circuit and verify its operation.

Test vector

Question No:210

(Marks:1)

Vu-Topper RM

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The implement the decoder circuit having inputs and outputs. Function tables have to be drawn which represent the output status of each Output line for or combinations of inputs

1 and 9

Question No:211

(Marks:1)

Vu-Topper RM

This function table represents _____ Gate.

Or gate

Question No:212

(Marks:1)

Vu-Topper RM

Suppose we want to transmit the data” 10001101”, and an “Even-parity” bit scheme is used to detect errors the parity bit added to this data will be

0

Question No:213

(Marks:1)

Vu-Topper RM

Which one of the following is not a valid rule of Boolean algebra?

A. $A = \bar{A}$

B. $AA = A$

C. $A + 1 = 1$

D. $A + 0 = A$

Question No:214

(Marks:1)

Vu-Topper RM

How many outputs can an integrated circuit comparator have?

Three

Question No:215

(Marks:1)

Vu-Topper RM

Which of the following is not the correct method of grouping?

Diagonally

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Question No:216 (Marks:1) **Vu-Topper RM**
The product of an XOR gate is zero(0), when _____ All the inputs are zero

I and IV only

Question No:217 (Marks:1) **Vu-Topper RM**
-----methods are used to Convert Decimal fractions to Binary.

2

Question No:218 (Marks:1) **Vu-Topper RM**
To display the number___ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-segment display circuit connected to the MSD &-Segment Display digit

29 Page 172

Question No:219 (Marks:1) **Vu-Topper RM**
A SOP expression is equal to I _____

When one or more product terms in the expression are equal to 1

Question No:220 (Marks:1) **Vu-Topper RM**
The output A B is set to I when the input combinations is

A=01, B=10

Question No:221 (Marks:1) **Vu-Topper RM**
If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them into floating point representation and then multiplying them, the value of mantissa of result will be _____

24.582

Question No:222 (Marks:1) **Vu-Topper RM**
Parts of logic gate identifies the switching

XX

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Question No:223

(Marks:1)

Vu-Topper RM

Sum term (max term) is implemented usinggates

OR

Question No:224

(Marks:1)

Vu-Topper RM

The output of the expression $FA+B+C$ will be Logic _____represents
OR Gate.

10(binary)

Question No:225

(Marks:1)

Vu-Topper RM

The binary value "1010110" is equivalent to decimal _____

86 (According to Formula)

Question No:226

(Marks:1)

Vu-Topper RM

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together

True

False

Question No:227

(Marks:1)

Vu-Topper RM

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

False

Question No:228

(Marks:1)

Vu-Topper RM

The terminal count of a modulus-13 binary counter is
0000

1101

Question No:229

(Marks:1)

Vu-Topper RM

The Synchronous counters are also known as Ripple Counters:

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True
False

Question No:230 (Marks:1) **Vu-Topper RM**
Design of state diagram is one of many steps used to design
a clock a truncated counter an UP/DOWN counter
Any counter

Question No:231 (Marks:1) **Vu-Topper RM**
Multiplexers are also known as _____.
Data Selectors **Page 167**

Question No:232 (Marks:1) **Vu-Topper RM**
TTL based devices work with a dc supply of _____ Volts
A. +3
B. +5
C. 3.3
D. +10

Question No:233 (Marks:1) **Vu-Topper RM**
How many bits must each word have in one-to-four line de-multiplexer
to be implemented using a memory?
1Bits

Question No:234 (Marks:1) **Vu-Topper RM**
The total amount of memory is depends upon _____
The size of the address bus of the microprocessor

Question No:235 (Marks:1) **Vu-Topper RM**
_____ can be determined the Instability condition.
logic diagram

Question No:236 (Marks:1) **Vu-Topper RM**

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If we add an inverter at the output of AND gate, what function is produced?

NAND

Question No:237

(Marks:1)

Vu-Topper RM

Which is also known as coincidence detector?

AND gate

Question No:238

(Marks:1)

Vu-Topper RM

Transition table include _____

Squares

Question No:239

(Marks:1)

Vu-Topper RM

For every possible combination of logical states in the inputs, which table shows the logical state of a digital circuit output?

Truth table

Question No:240

(Marks:1)

Vu-Topper RM

Stack is an acronym for _____

LIFO memory

Question No:241

(Marks:1)

Vu-Topper RM

Positive OR gate is also a negative

AND gate

Question No:242

(Marks:1)

Vu-Topper RM

First operator precedence for evaluating Boolean expressions is

Parenthesis

Question No:243

(Marks:1)

Vu-Topper RM

The output is _____ When an input signal 1 is applied to a NOT gate

0

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Question No:244 (Marks:1) **Vu-Topper RM**
The value of n is _____ when the resolution of an n bit DAC with a maximum input of 5 V is 5 mV.

10

Question No:245 (Marks:1) **Vu-Topper RM**
2's complement of binary number 0101 is _____

1011

Question No:246 (Marks:1) **Vu-Topper RM**
An OR gate has 4 inputs. The output is When One input is high and the other three are low.

High

Question No:247 (Marks:1) **Vu-Topper RM**
convert BCD to seven segments _____ device is used.

Decoder

Question No:248 (Marks:1) **Vu-Topper RM**
Decimal number 10 is equal to binary number _____.

1010

Question No:249 (Marks:1) **Vu-Topper RM**
In 2's complement representation the number 11100101 represents the decimal number _____.

-27

+28

Question No:250 (Marks:1) **Vu-Topper RM**
BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are_____.

All

Question No:251 (Marks:1) **Vu-Topper RM**

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In asynchronous digital systems all the circuits change their state with respect to a common clock

False

True

Question No:252

(Marks:1)

Vu-Topper RM

Which of the number is not a representative of hexadecimal system?

“1001”

Question No:253

(Marks:1)

Vu-Topper RM

To get the answer “1” in Boolean addition of three variables, _____

One of the variables must be 1

Question No:254

(Marks:1)

Vu-Topper RM

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

8

Question No:255

(Marks:1)

Vu-Topper RM

Consider $A=1, B=0, C=1$. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

Zero

Question No:256

(Marks:1)

Vu-Topper RM

The Binary number 1011.101 has an Integer part represented by _____ and a fraction part _____ separated by a decimal point.

1011, 101

Question No:257

(Marks:1)

Vu-Topper RM

Adding two octal numbers “36” and “71” result in _____

A. 127

B. 213

C. 123

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D. 345

Question No:258

(Marks:1)

Vu-Topper RM

The first Least Most digit in decimal number system has

Has position 0 and weight equal to 1

Question No:259

(Marks:1)

Vu-Topper RM

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

True

False

Question No:260

(Marks:1)

Vu-Topper RM

The three fundamental gates are _____

A. NOT, OR, AND

B. OR, AND, NAND

C. NOT, NOR, XOR

D. AND, NAND, XOR

Question No:261

(Marks:1)

Vu-Topper RM

For a Standard SOP expression, a ____ is placed in the cell corresponding to the product term present in the expression.

1

Question No:262

(Marks:1)

Vu-Topper RM

The carry propagation delay problem in parallel binary adder can be solved by _____.

A. Using two full adders

B. Using look-ahead carry circuits

C. Using bridge circuit between two adders

D. Carry propagation problem can not be solved

Question No:263

(Marks:1)

Vu-Topper RM

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Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a _____ multiplexer.

2-input, 8-bit

Question No:264

(Marks:1)

Vu-Topper RM

The octal equivalent of the following binary number is _____

117

Question No:265

(Marks:1)

Vu-Topper RM

A' is written in ABEL as _____.

!A

Question No:266

(Marks:1)

Vu-Topper RM

Which of the following is the hexadecimal equivalent of 28?

1C

Question No:267

(Marks:1)

Vu-Topper RM

Function labels required to represent the input/output combinations for each segment in 7-segment display

7

Question No:268

(Marks:1)

Vu-Topper RM

Which of the following gates has the output 1 if and only if at least one input is 1?

A. OR

B. NOR

C. AND

D. NAND

Question No:269

(Marks:1)

Vu-Topper RM

Digital circuits operate with _____ voltage value(s)

2

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Question No:270

(Marks:1)

Vu-Topper RM

A sop expression can be implemented by on ___ combination of gates.

AND-OR

Question No:271

(Marks:1)

Vu-Topper RM

The between expression $X-AB+CD$ represents

Two ANDs O Red together

Question No:272

(Marks:1)

Vu-Topper RM

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

Question No:273

(Marks:1)

Vu-Topper RM

The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

Question No:274

(Marks:1)

Vu-Topper RM

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

row, column

Question No:275

(Marks:1)

Vu-Topper RM

Which of the following Output Equations determines the output of the State Machine?

MAX = Q0Q1EN

Question No:276

(Marks:1)

Vu-Topper RM

The maximum value, represented by a single hexadecimal digit is ____.

A. "F"

B. "H"

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- C. "E"
D. "G"

Question No:277 (Marks:1) **Vu-Topper RM**
If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

1

Question No:278 (Marks:1) **Vu-Topper RM**
The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

High

Question No:279 (Marks:1) **Vu-Topper RM**
Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

Negative-OR, Negative-AND

Question No:280 (Marks:1) **Vu-Topper RM**
Two signals _____ and _____ provide the timing inputs to the State Machine.

PTIME and QTIME

Question No:281 (Marks:1) **Vu-Topper RM**
PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

PLDs **Page 194**

Question No:282 (Marks:1) **Vu-Topper RM**
The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

CONSTATE

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Question No:283

(Marks:1)

Vu-Topper RM

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.

Shift Registers

Question No:284

(Marks:1)

Vu-Topper RM

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

Synchronous

Question No:285

(Marks:1)

Vu-Topper RM

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.

Four

Question No:286

(Marks:1)

Vu-Topper RM

In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

NAND, NAND

Question No:287

(Marks:1)

Vu-Topper RM

The _____ input overrides the _____ input.

Asynchronous, synchronous

Question No:288

(Marks:1)

Vu-Topper RM

The 64-cell array organized as 8 x 8 cell array is considered

8-byte memory

Question No:289

(Marks:1)

Vu-Topper RM

Memory is arranged in _____.

Two-dimensional manner

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Question No:290

(Marks:1)

Vu-Topper RM

Subtractors also have output to check if 1 has been _____.

Primed

Question No:291

(Marks:1)

Vu-Topper RM

The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.

Three

Question No:292

(Marks:1)

Vu-Topper RM

A multiplexer with a register circuit converts

Parallel data to serial

Question No:293

(Marks:1)

Vu-Topper RM

The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

Four

Question No:294

(Marks:1)

Vu-Topper RM

Why demultiplexer is called a data distributor?

Single input to Single Output

Question No:295

(Marks:1)

Vu-Topper RM

When the transmission line is idle in an asynchronous transmission

It is set to logic high

Question No:296

(Marks:1)

Vu-Topper RM

UVERPROM is stands for

Ultra-Violet

Question No:297

(Marks:1)

Vu-Topper RM

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In memory write cycle, the time for which the WE signal remains active is known as the _____.

Write pulse width

Question No:298

(Marks:1)

Vu-Topper RM

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.

AND

Question No:299

(Marks:1)

Vu-Topper RM

PALs tend to execute _____ logic.

A. SPD

B. SAC

C. SOP

D. SAP

Question No:300

(Marks:1)

Vu-Topper RM

The ROM used by a computer is relatively _____ as it stores few buyers of code used to Boot the Computer system on power up.

Small

Question No:301

(Marks:1)

Vu-Topper RM

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration towed?

WE

Question No:302

(Marks:1)

Vu-Topper RM

You have to choose suitable option when your timer will reset by considering this given code:

TRSTATE.CLK = clk;

TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);

NSY2 or EWY2

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Question No:303

(Marks:1)

Vu-Topper RM

A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

NOR, NAND

Question No:304

(Marks:1)

Vu-Topper RM

Implementation of Latch is required almost _____ transistor.

Six

Question No:305

(Marks:1)

Vu-Topper RM

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

7.8 microsec

Question No:306

(Marks:1)

Vu-Topper RM

The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

NAND

Question No:307

(Marks:1)

Vu-Topper RM

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.

REQ1

Question No:308

(Marks:1)

Vu-Topper RM

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

One

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Question No:309

(Marks:1)

Vu-Topper RM

The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

Truth Table

Question No:310

(Marks:1)

Vu-Topper RM

In DRAM read cycle R /W⁻ signal is activated to read data which is made available on the _____ data line.

D(OUT)

Question No:311

(Marks:1)

Vu-Topper RM

Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.

RAM

Question No:312

(Marks:1)

Vu-Topper RM

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack ____.

Top

Question No:313

(Marks:1)

Vu-Topper RM

Which one flip-flop has an invalid output state?

SR

Question No:314

(Marks:1)

Vu-Topper RM

The Transition table is very similar to the _____ table.

State

Question No:315

(Marks:1)

Vu-Topper RM

Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

256

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Question No:316

(Marks:1)

Vu-Topper RM

Cin is part of _____ Adder.

Full

Question No:317

(Marks:1)

Vu-Topper RM

Flash memories Operation are classified into _____ different operation.

Two

Question No:318

(Marks:1)

Vu-Topper RM

A Product term is 0 when _____

Any one literal is 0

Question No:319

(Marks:1)

Vu-Topper RM

Device dissipate varying amount of power depending upon the frequency of operation.

CMOS

Question No:320

(Marks:1)

Vu-Topper RM

A standard POS form has _____ ters that have all the variables in the domain of the expression.

Sum

Question No:321

(Marks:1)

Vu-Topper RM

Which of the following is the example of comparator?

XNOR

Question No:322

(Marks:1)

Vu-Topper RM

In CMOS 5 Volt series, Input voltage of Logic high signal (V_{IH}) with a ranges from _____ to _____ volts.

A. 0,5

B. 3.5,5 Google

C. 0,3.5

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D. 4.5,5

Question No:323

(Marks:1)

Vu-Topper RM

The Adjacent 1 S Detector accepts 4-bits input. If ____ adjacent 1S are detected in the input, the output is set to high.

4

Question No:324

(Marks:1)

Vu-Topper RM

DE Morgan's two theorems prove the equivalency of the NAND and ____ gates and the NOR and ____ gates respectively.

Negative-AND, Negative-OR

Question No:325

(Marks:1)

Vu-Topper RM

Consider A=1, B=0,C=1 B and C represent the input of three bit NAND gate, the output of the NAND gate will be.

No output as input is invalid

Question No:326

(Marks:1)

Vu-Topper RM

Sequential circuit memory elements are connected with ____.

Clock

Question No:327

(Marks:1)

Vu-Topper RM

In the 32-bit Single Precision Floating Point format, the exponent value ____ is reserved to represent infinity exponents.

255

Question No:328

(Marks:1)

Vu-Topper RM

The Gray code is different from the unsigned binary code because

A. Gray Code is positional code

B. Gray Code ranges from "0" to "9"

C. Gray Code does not support negative values

D. Successive value of Gray code by only one bit

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Question No:329

(Marks:1)

Vu-Topper RM

Portable devices that run on batteries use____ circuit that have low power dissipation.

Integrated

Question No:330

(Marks:1)

Vu-Topper RM

The domain of the expression $AB'CD+B$ is

B only

Question No:331

(Marks:1)

Vu-Topper RM

_____ is a single input gate

OR

Question No:332

(Marks:1)

Vu-Topper RM

BCD code of 16 is_____.

00010001

Question No:333

(Marks:1)

Vu-Topper RM

The measurable values generally change over a

Continuous range

Question No:334

(Marks:1)

Vu-Topper RM

What is the output expression of segment 'b' implementation in BCD to 7segment decoder?

$B'+C'D'+CD$

Question No:335

(Marks:1)

Vu-Topper RM

It is more suitable to use _____ method in order to simplify the Boolean expression having more than 4 variables.

A. Karnaugh map

B. Quin McClusky

Google

C. De Morgan's theorem

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D. Boolean algebra and Laws

Question No:336 (Marks:1) **Vu-Topper RM**
System having memory elements are called _____ circuits.
Sequential circuits **Google**

Question No:337 (Marks:1) **Vu-Topper RM**
Demultiplexer is also called _____
Data Distributor **Page 178**

Question No:338 (Marks:1) **Vu-Topper RM**
For a 3-to-8 decoder how many 2-to-4 decoders will be required?
Decoders **Google**

Question No:339 (Marks:1) **Vu-Topper RM**
“The complement of a product of variables is equal to the sum of the complements of the variables.” is known as:
A. Boolean Expression
B. Boolean Algebra Rule
C. Demorgan's First Theorem **Page 74**
D. Demorgan's Second Theorem

Question No:340 (Marks:1) **Vu-Topper RM**
The _____ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.
Programmed Polarity **Page 18**

Question No:341 (Marks:1) **Vu-Topper RM**
Quine-McCluskey and K-Map methods are used for _____ of Boolean expression.
Simplification **Page 111**

Question No:342 (Marks:1) **Vu-Topper RM**

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The series of TTL chips are characterized by their_____.

Switching Speed only **Page 61**

Question No:343 (Marks:1) **Vu-Topper RM**

When two or more sum terms are multiplied by Boolean multiplication, the result is a _____ expression.

Product-of-sums **POS**

Question No:344 (Marks:1) **Vu-Topper RM**

The logical sum of two or more logical product terms is called

SOP

Question No:345 (Marks:1) **Vu-Topper RM**

-----has fastest switching speed and low power requirements

Advanced low power socket

Question No:346 (Marks:1) **Vu-Topper RM**

The multiplexer circuit hasinput (s) and.....output (s)

Multiple, signal

Question No:347 (Marks:1) **Vu-Topper RM**

Which of the following 4 bit has five function select inputs?

74XX181

Question No:348 (Marks:1) **Vu-Topper RM**

NAND gate is form by connecting _____

A. AND Gate and then OR Gate

B. OR Gate and then AND Gate

C. NOT Gate and then AND Gate

D. AND Gate and then NOT Gate

Question No:349 (Marks:1) **Vu-Topper RM**

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.....occur when the same clock signal arrive at different at different clock input due to propagation delay

Clock skew

Question No:350

(Marks:1)

Vu-Topper RM

A non shot mono stable device contain.....

NOR gate resister,capacitor and NOT gate

Question No:351

(Marks:1)

Vu-Topper RM

“74ALS” stands for _____

A. Advanced low power Schottky TTL

B. Advanced Low-frequency Schottky TTL

C. Advanced Low-dissipation Schottky TTL

D. Advanced Low-propagation Schottky TTL

Question No:352

(Marks:1)

Vu-Topper RM

Which one is true

A. Powe consumption of TTL is higher from CMOS

B. Power consumption of CMOS is higher than TTL

C. Both TTL and CMOS have same power consumption

D. Power consumption of both CMOS and TTL depends on no. of gates in circuit.

Question No:353

(Marks:1)

Vu-Topper RM

The complement of product of variable is equal to the sum of complement of variable is known as

DeMorgan's second theorem

Question No:354

(Marks:1)

Vu-Topper RM

The below are Integrated Circuit Technologies except _____.

A. TTL

B. ECL

C. PMOS

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D. ETMOS

Question No:355

(Marks:1)

Vu-Topper RM

Which of the following is not correct method of grouping

On corners

Question No:356

(Marks:1)

Vu-Topper RM

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the

Set- up time

Question No:357

(Marks:1)

Vu-Topper RM

A one- shot mono-stable device contains=

NOR gate, Resistor, capacitor and NOT Gate

Question No:358

(Marks:1)

Vu-Topper RM

Two 2-input ,4-bit multiplexers 74x157 can be connected to implement a...multiplexer.

2- input,8bit

Question No:359

(Marks:1)

Vu-Topper RM

Canonical form is a unique way of representing

Boolean Expression

Question No:360

(Marks:1)

Vu-Topper RM

The 4-variable Karnaugh Map (K-Map) has _____rows and _____columns

4,4

Modern information transmission techniques are relying more on _____ transmission.

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A. Digital **Page 5**

- B. Analogue
- C. None of given
- D. Both Digital and Analogue

Which number is added for correction purpose to an incorrect result obtained in BCD addition?

A. 0001

B. 0110 **Page 35**

- C. 1001
- D. 0011

The switching speed of CMOS is now _____.

- A. Slower than TTL
- B. Twice that of TTL
- C. Three times that of TTL
- D. Competitive with TTL**

Gray code of 8 is:

A. 1100 **Google**

- B. 1000
- C. 0000
- D. 0100

The number "1259" may belong to _____ number system.

- A. Binary number system
- B. Octal or Decimal system.
- C. Binary or Hexadecimal system
- D. Decimal or Hexadecimal system**

The _____ Gate is used in applications where the output signal is a 1 when any one input is a 1.

A. OR **Page 43**

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- B. XOR
- C. AND
- D. NOT

_____ and _____ Gates are used to detect dissimilar and similar inputs respectively.

OR, XOR

OR, Inverter

NOT, XNOR

XOR, XNOR Page 53

The boolean expression $X = AB + CD$ represents an exclusive-Or

a 4-input AND gate

two ORs ANDed together

two ANDs ORed together

The range of Excess-8 code is from _____ to _____

+8 to -7

+9 to -8

+7 to -8

-9 to +8

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.

A. 1001

B. 1000

C. 1111

D. 0011

A function represented by an expression in _____ form can be readily programmed.

Boolean

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Non-standard SOP

The output of an exclusive-OR gate is HIGH if _____.

All inputs are LOW

All inputs are HIGH

All inputs are unequal

All inputs are DON'T care

Which of the following is the hexadecimal equivalent of 39?

27 Google

28

29

30

In 15 digit decimal floating point format, the biased exponent value _____ can be used to represent the number zero whatever the value of the mantissa.

0

00 Google

000

0000

To implement the decoder circuit, having _____ inputs and _____ outputs, function tables have to be drawn which represent the output status of each output line for all combinations of inputs.

1 and 9

4 and 7

3 and 8

5 and 6

The output of an AND gate with three inputs, A, B, and C, is HIGH when _____.

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A=1, B=0, C=1

A=1, B=1, C=1

A=1, B=1, C=0

A=0, B=0, C=0

To represent the signal digitally the signal is sampled at _____
and _____ intervals.

Fixed, Equal **Google**

Unfixed, Equal

Fixed, Un-equal

Unfixed, Un-equal

In 32-bit Single-Precision Floating Point format representation the range
of exponent value is from _____ to _____

+127 to -126

+255 to - 254

+256 to -255

+128 to -254

In 15 digit decimal floating point format, the biased exponent value
_____ can be used to represent the number infinity whatever
the value of mantissa.

99

98

256

255

The values that exceed the specified range can not be correctly
represented and are considered as _____

Carry

Parity

Overflow

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Sign value

$A + B = B + A$ is _____

Distributive Law

Associative Law

Demorgan's Law

Commutative Law Google

NOR gate is form by connecting _____

OR Gate and then AND Gate

AND Gate and then OR Gate

NOT Gate and then OR Gate

OR Gate and then NOT Gate

The digital circuits operate with which combination of values given below?

0 volts, 0 volts

-5 volts, 0 volts

+5 volts, 0 volts

-5 volts, +5 volts

Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

Positive-OR, Positive-AND

Negative-AND, Positive-OR

Positive-OR, Negative-AND

Negative-OR, Negative-AND

Page 74

Karnaugh Map Array is considered to be wrapped around where all sides are _____ to each other.

Serial

Parallel

Opposite

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Vu Topper RM

برى صءبء سے ءءهائى بهءر هء اور ءءهائى سے نىك صءبء بهءر هء

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