File Version Update: (Dated: 17-May-2011)

This version of file contains:

- Content of the Course (Done)
- FAQ updated version.(These must be read once because some very basic definition and question are being answered)
- Glossary updated version.(These must be read once because some very basic terms are being explained which you even might not found in the book) (Done)
- Solved Past Assignment Selected for MID Term. (Done)
- Solved Question From Mid-Term Papers (Done))
- MCQs GIGA File (with references) (Done)
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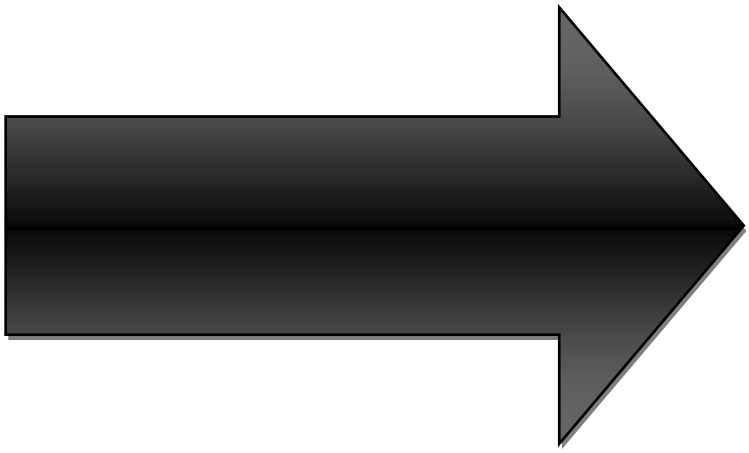
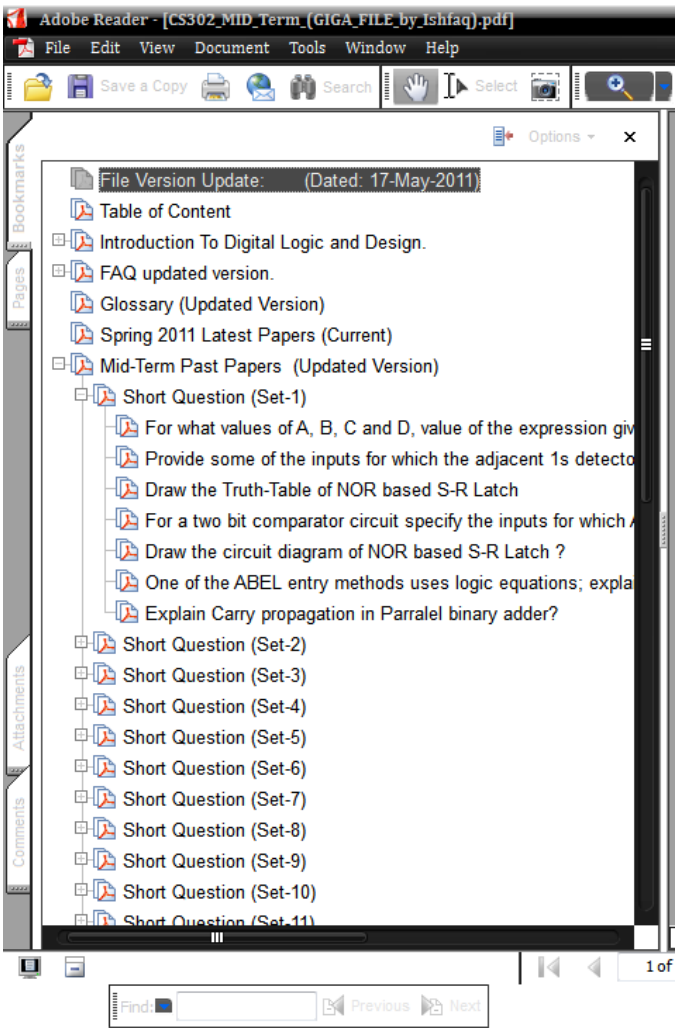
Note: Use Table Of Content to view the Topics, In PDF(*Portable Document Format*) format , you can check Bookmarks menu.





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Introduction To Digital Logic and Design.

Course Content:

An overview & number systems, Number systems & codes, Logic gates, Digital circuits and operational characteristics, Boolean algebra and logic simplification, Karnaugh map & Boolean expression simplification, Comparator, Odd-Prime Number detector, Implementation of an odd-parity generator circuit, BCD adder, 16-bit ALU, the 74xx138 3-to-8 decoder, 2-input 4-bit multiplexer, Demultiplexer, Implementing constant 0s and 1s, the gal16v8, Abel input file of a quad 1-of-4 MUX, Application of S-R Latch, Flip-Flops, the 555 Timer, Up-Down counter, Digital Clock, Shift Registers, Memory, Analog to Digital Converters

FAQ updated version.

Question: How can a D flip-flop can be made to toggle?

Answer: A D flip-flop can be made to toggle by connecting Q' to D.

Question: What is the difference between a counter and shift register ?

Answer: A counter has a specified sequence of states, but a shift register does not.

Question: How many outputs and inputs GAL22V10 have?

Answer: The GAL22V10 has 22 inputs and 10 outputs. V=variable

Question: What is an equivalent representation for the Boolean expression A' + 1 ?

Answer: From the Boolean property A + 1 = 1, let A = A'=> A' + 1=1

Question: What is K-map and why we used it?

Answer: A Karnaugh map provides a pictorial method of grouping together expressions with common factors and therefore eliminating unwanted variables. The Karnaugh map can also be described as a special arrangement of a truth table.

Question: Each stage in a shift register represents how much storage capacity?

Answer: one bit

Question: what are PLD's? How are they classified.

Answer: The programmable logic devices (PLD's) are used in a lot of applications. These replaced SSI (Small Scale Integration) and MSI (Medium Scale Integration) circuits, due the space saving and reduce the number of devices in a certain design. A PLD is made of a matrix of AND and OR gates, that can be programmed to obtain certain logic functions. There are four types of devices that can be classified as PLD's:

a)The Programmable Read-Only Memory, PROM.
b)The Programmable Logic Array , PLA.
c)The Programmable Array Logic, PAL.
d)The Generic Array Logic, GAL.(same as PAL with OR gate fixed)

Question: What are Flip-flops?

Answer: The memory elements in a sequential circuit are called flip-flops. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the stored bit.

Question: If an S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, then what the latch will be?

Answer: The latch will be in reset condition. See the table.

Question: In a 4-bit Johnson counter sequence there are a total of how many states, or bit patterns?

Answer: 8

Question: Explain the truth table and timing diagram of Gated S-R latch and Gated D latch in detail.

Answer: The logic symbol for the S-R flip-flop is shown here and its operation outlined in Table below.
Now we examine the output waveforms from the S-R flip-flop given the inputs. Assume that Q is HIGH initially.
The logic symbol for the D flip-flop is also shown below and its operation outlined in the Table. Notice that this flip-flop only has one input in addition to the clock called the D-input. Note that whatever is on the D-input when the trigger occurs is output at Q.

Notice that a D flip flop can be made from a S-R flip flop by ensuring that the S and R outputs are the complement of each other at all times.

Question: What is the difference between asynchoronous and synchronous counters?

Answer: Synchronous refers to the situation when all the interrelated devices have some common and fixed time relationship. Whereas in Asynchronous refers to the situation when the situation is opposite.

In Synchronous counters all the flip-flops have same clock pulse and in Asynchronous counters flip-flops does not change state at the exactly same time because they don't have common clock pulse.

Question: What is meant by D in gated D latch and what is the fuction of this D input. What is the basic difference between latchs and flip-flops?

Answer: The 'D' in 'Gated D Latch' stands for 'Data'.Unlike 'S-R Latch' Gated D Latch has only one input ,which is D(data) Input. Whcih will give the output of the latch depending on the 'EN' (enable) state of the latch. To understand latches and flip-flops lets consider a basic fact about the whole DLD

In the same way that gates are the building blocks of combinatorial circuits, latches and flip-flops are the building blocks of sequential circuits. While gates had to be built directly from transistors, latches can be built from gates, and flip-flops can be built from latches.

Both latches and flip-flops are circuit elements whose output depends not only on the current inputs, but also on previous inputs and outputs. The difference between a latch and a flip-flop is that

a latch does not have a clock signal, whereas a flip-flop always does

Latches are asynchronous, which means that the output changes very soon after the input changes. A flip-flop is a synchronous version of the latch.

Question: I cannot understand the timing diagram for the master slave flip flop.

Answer: A master-slave flip-flop is constructed from two separate flip-flops. One circuit serves as a master and the other as a slave. The logic diagram of an SR flip-flop is shown here. The master flip-flop is enabled on the positive edge of the clock pulse CP and the slave flip-flop is disabled by the inverter. The information at the external R and S inputs is transmitted to the master flip-flop. When the pulse returns to 0, the master flip-flop is disabled and the slave flip-flop is enabled. The slave flip-flop then goes to the same state as the master flip-flop.

Logic diagram of a master-slave flip-flop

The timing relationship is also shown here and is assumed that the flip-flop is in the clear state prior to the occurrence of the clock pulse. The output state of the master-slave flip-flop occurs on the negative transition of the clock pulse. Some master-slave flip-flops change output state on the positive transition of the clock pulse by having an additional inverter between the CP terminal and the input of the master.

Timing relationship in a master slave flip-flop.

Question: I am not able to understand the truth table and timing diagram of " S-R Edge-trigged flip-flop, D edge-trigged flip-flop and J-K edge-trigged flip-flop kindly explain it in detail.

Answer: An edge-triggered flip-flop changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input.

The S-R, J-K and D inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. On the other hand, the direct set (SET) and clear (CLR) inputs are called asynchronous inputs, as they are inputs that affect the state of the flip-flop independent of the clock. For the synchronous operations to work properly, these asynchronous inputs must both be kept LOW.

The basic operation of Edge-triggered S-R flip-flop is illustrated below, along with the truth table for this type of flip-flop. The operation and truth table for a negative edge-

triggered flip-flop are the same as those for a positive except that the falling edge of the clock pulse is the triggering edge.

Note that the S and R inputs can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output. This is illustrated in the timing diagram below:

While an Edge-triggered J-K flip-flop works very similar to S-R flip-flop. The only difference is that this flip-flop has NO invalid state. The outputs toggle (change to the opposite state) when both J and K inputs are HIGH. The truth table is shown below.

The operations of an Edge-triggered D flip-flop is much more simpler. It has only one input addition to the clock. It is very useful when a single data bit (0 or 1) is to be stored. If there is a HIGH on the D input when a clock pulse is applied, the flip-flop SETs and stores a 1. If there is a LOW on the D input when a clock pulse is applied, the flip-flop RESETs and stores a 0. The truth table below summarize the operations of the positive edge-triggered D flip-flop. As before, the negative edge-triggered flip-flop works the same except that the falling edge of the clock pulse is the triggering edge.

Question: What is Multiplexer and what are its applications and expression simplification using Multiplexer?

Answer: Multiplexer is a digital circuit with multiple signal inputs, one of which is selected by separate address inputs to be sent to the single output. The multiplexer circuit is typically used to combine two or more digital signals onto a single line, by placing them there at different times. Technically, this is known as time-division multiplexing.

Input A is the addressing input, which controls which of the two data inputs, X0 or X1, will be transmitted to the output. If the A input switches back and forth at a frequency more than double the frequency of either digital signal, both signals will be accurately reproduced, and can be separated again by a demultiplexer circuit synchronized to the multiplexer.

This is not as difficult as it may seem at first glance; **the telephone network** combines multiple audio signals onto a single pair of wires using exactly this technique, and is readily able to separate many telephone conversations so that everyone's voice goes only to the intended recipient. With the growth of the Internet and the World Wide Web, most people have heard about T1 telephone lines. A T1 line can transmit up to 24 individual telephone conversations by multiplexing them in this manner.

A very common application for this type of circuit is found in computers, where dynamic memory uses the same address lines for both row and column addressing. A set of multiplexers is used to first select the row address to the memory, then switch to the column address. This scheme allows large amounts of memory to be incorporated into

the computer while limiting the number of copper traces required connecting that memory to the rest of the computer circuitry. In such an application, this circuit is commonly called a data selector. Multiplexers are not limited to two data inputs. If we use two addressing inputs, we can multiplex up to four data signals. With three addressing inputs, we can multiplex eight signals.

Question: Explain S-R Latch? what do you mean by bi-stable devices?

Answer: A bi-stable multivibrator has two stable states, as indicated by the prefix bi in its name. Typically, one state is referred to as set and the other as reset. The simplest bi-stable device, therefore, is known as a set-reset, or S-R, latch.
The Q and not-Q outputs are supposed to be in opposite states. I say "supposed to" because making both the S and R inputs equal to 1 results in both Q and not-Q being 0. For this reason, having both S and R equal to 1 is called an invalid or illegal state for the S-R multivibrator. Otherwise, making S=1 and R=0 "sets" the multivibrator so that Q=1 and not-Q=0. Conversely, making R=1 and S=0 "resets" the multivibrator in the opposite state. When S and R are both equal to 0, the multivibrator's outputs "latch" in their prior states.
By definition, a condition of Q=1 and not-Q=0 is set. A condition of Q=0 and not-Q=1 is reset. These terms are universal in describing the output states of any multivibrator circuit. So A bistable multivibrator is one with two stable output states. In a bistable multivibrator, the condition of Q=1 and not-Q=0 is defined as set. A condition of Q=0 and not-Q=1 is conversely defined as reset. If Q and not-Q happen to be forced to the same state (both 0 or both 1), that state is referred to as invalid. In an S-R latch, activation of the S input sets the circuit, while activation of the R input resets the circuit. If both S and R inputs are activated simultaneously, the circuit will be in an invalid condition. A race condition is a state in a sequential system where two mutually-exclusive events are simultaneously initiated by a single cause.

Question: What is meant by triggering or triggering edge of clock pulse and synchronous? also what is trigging transition of clock?

Answer: Generally the term 'synchronous' means "Moving or changing at the same time". In our senario this term also holds the same meaning.
Here the two things which will change at the same time will be "Clock (CLK or C)" and the "output of the device". Means changes in the output occur with synchronization with clock.

Edge-Triggered devices changes staes either at the positive edge(rising edge) or the negative edge (falling edge) of the clock pulse and is sensative to its inputs only at the these two (negative or positive) edges,which in technical terms is called 'Transition of the clock'.
By examining the picture below you will understand it completly.

Question: How to up and down the clock in J K flops plz explain the example?

Answer: In J-K filp-flops the clock moves normaly as in other cases no difference.The clock pulse will change its state after the specified intervals(usually defined in 'nano seconds'(ns)) to either UP i.e '1' or DOWN i.e '0'.

Question: For BCD numbers that add up to an invalid BCD number or generate a carry, the number 6 (0110) is added to the invalid number, why ?

Answer: These binary numbers are not allowed in the BCD code: 1010, 1011, 1100, 1101, 1110, 1111
Then, if the addition produces a carry and/or creates an invalid BCD number, an adjustment is required to correct the sum. The correction method is to add 6 to the sum in any digit position that has caused an error.
For example,
15 + 9 = 24
0001 0101 = 15
+ 0000 1001 = 9

_____

0001 1110 = 1? (invalid 1110)

0001 1110 = 1? (invalid)
+ 0000 0110 = 6 (adjustment)

_____

0010 0100 = 24

Question: Why do we use +0V and +5V instead of +0V and +1V in DLD, when it is always '0' and '1' ?

Answer: In DLD, the circuits of logic gates (embedded in IC's) are operated with +5 Volts input. That is why we refer to +5 V for these logic inputs. It is considered as binary 1 when the +5V are applied to the logic gate, and binary 0 when 0 V are applied to the logic gate.

Question: What is BCD and how do we write them?

Answer: BCD (Binary-Coded Decimal) is a system for encoding Decimal Numbers in binary form to avoid rounding and conversion errors. In BCD coding, each digit of a decimal number is coded separately as a binary numeral. Each of the decimal digits 0 through 9 is coded in four bits and for ease of reading, each group of four bits is separated by a space. This format, also called 8-4-2-1 after the weights of the four bit positions, uses the following codes:
0000 = 0
0001 = 1
0010 = 2
0011 = 3
0100 = 4
0101 = 5
0110 = 6
0111 = 7
1000 = 8
1001 = 9
Thus, the decimal number 12 is 0001 0010 in binary-coded decimal notation.

Question: Where do we use Caveman Number System ?

Answer: Caveman Number System was introduced in old ages as symbolic representation of decimal number system. You do not need to study it in detail, as it is also mentioned that this system is not used anywhere now a days.

Question: What is Gray Code and how do we write them?

Answer: Gray Code is a binary sequence with the property that an ordering of 2n binary numbers such that only one bit changes from one entry to the next. Gray codes are useful in mechanical encoders since a slight change in location only affects one bit. Using a typical binary code, up to n bits could change, and slight misalignments between reading elements could cause wildly incorrect readings.
It is a number code where consecutive numbers are represented by binary patterns that differ in one bit position only.
Here you can see, for each number, there is a difference of 1 (addition or elimination of 1)
0000 =0
0001 =1
0011 =2 ,1 is added
0010 =3 , again change of 1, elimination of 1
0110 =4 ,addition of 1
0111 =5 ,again addition of 1
0101 =6 ,elimination of 1
0100 =7 ,elimination of 1
1100 =8 ,addition of 1
1101 =9 ,addition of 1
One way to construct a Gray code for n bits is to take a Gray code for n-1 bits with each code prefixed by 0 (for the first half of the code) and append the n-1 Gray code reversed with each code prefixed by 1 (for the second half). This is called a "binary-reflected Gray code". Here is an example of creating a 3-bit Gray code from a 2-bit Gray code. 00 01 11 10
A Gray code for 2 bits
000 001 011 010 the 2-bit code with "0" prefixes
10 11 01 00 the 2-bit code in reverse order
110 111 101 100 the reversed code with "1" prefixes
000 001 011 010 110 111 101 100 A Gray code for 3 bits

Glossary (Updated Version)

ABEL : Advanced Boolean Expression Language; a software compiler language for SPLD programming; a type of hardware description language (HDL)
Adder : A digital circuit which forms the sum and carry of two or more numbers.
address : The location of a given storage cell or group of cells in a memory; a unique memory location containing one byte.
address bus : Generally, a one-way group of conductors from the microprocessor to memory, containing the address information.
Analog : A signal which is continuously variable and, unlike a digital signal, does not have discrete levels. (A slide rule is analog in function.)
Analog Computer : Computer which represents numerical quantities as electrical and physical variables. Solutions to mathematical problems are accomplished by manipulating these variables.
AND Gate : A basic logic gate that outputs a 1 only if both inputs are a 1 , otherwise outputs a 0. See also, NAND, NOR and OR.
Binary : The binary number system has only two digits - 0 and 1.

Binary Code : A code in which each element may be either of two distinct values (eg the presence or absence of a pulse).
Binary Coded Decimal (BCD) : A coding system in which each decimal digit from 0 to 9 is represented by four bits.
Bit : A single digit of a binary number. A bit is either a one represented by a voltage or a zero represented by no voltage. The number 5 represented in 4 and 8 bit binary would be 0101 and 00000101 respectively.
Boolean Algebra : The algebra of logic named for George Boole. Similar in form to ordinary algebra, but with classes, propositions, yes/no criteria, etc for variables rather than numeric quantities. It includes the operators AND, OR, NOT, IF, EXCEPT, THEN.
Cascade : To connect 'end-to-end' as when several counters are connected from the terminal count output of one counter to the enable input of the next counter.
Clock : The device in a digital system which provides the continuous train of pulses used to synchronize the transfer of data. Sometimes referred to as "the heartbeat."
CMOS : (Complementary Metal Oxide Semiconductor) An advanced IC manufacturing process technology characterized by high integration, low cost, low power and high performance. CMOS is the preferred process for today's high density ICs.
Combinational Logic : Logic circuits whose outputs depend only on the present logic inputs. These do not have any storage element.
Comparator : A digital circuit that compares the magnitudes of two quantities and produces an output indicating the relationship of the quantities.
Counter: A digital circuit capable of counting electronic events, such as pulses, by progressing through a sequence of binary states.
Data selector : A circuit that selects data from several inputs one at a sequence and places them on the output: also called a **multiplexer.**
Decoder : A logic function that uses a binary value, or address, to select between a number of outputs and to assert the selected output by placing it in its active state.
Digital System : A system in which information is transmitted in a series of pulses. The source is periodically sampled, analyzed, and converted or coded into numerical values and transmitted. Digital transmissions typically use the binary coding used by computers so most data is in appropriate form, but verbal and visual communication must be converted. Many satellite transmissions use digital formats because noise will not interfere with the quality of the end product, producing clear and higher-resolution imagery.
Emitter: One of the three regions in a bipolar junction transistor.
Encoder: A digital circuit (device) that converts information to a coded form.
Even parity : The condition of having an even number of 1s in every group of bits.
Exponent: The part of floating point number that represents the number of places that the decimal point (or binary point) is to be moved.
Fan in : The number of logic inputs into a logic gate.
Fan out : The number of logic inputs that can be driven by the output of a logic gate.
flip-flop : A basic digital building block that, at its simplest, uses two gates cross-coupled so that the output of one gate serves as the input of the other. It is capable of changing from one state to another on application of a control signal, but can remain in that state after the signal is removed. It thus serves as a basic storage element. Most flip-flops contain additional features to make them more versatile. Many digital circuits, such as registers and counters, are a number of flip flops connected together.
GAL: Generic array logic; an SPLD with a reprogrammable AND array, a fixed OR array, and programmable Output Logic Macro Cells **(OLMC)**.

Gate: The control terminal of a MOSFET, or alternately a basic digital logic element, for example an AND Gate, See also, OR, NAND, NOR.
Gate Array : An integrated circuit made up of digital logic gates that are not yet connected. Typically gate arrays are fabricated up to the metal layers and then a custom metal mask is designed for a customer and used to connect the gates into a customer specific circuit.
Gray code: The mirror image of the binary counting code which changes one bit at a time when increasing or decreasing by one.
half-adder : A digital circuit that adds two bits and produces a sum and output carry. It cannot handle input carries.
High: A digital logic state corresponding to a binary "1."
High logic: In digital logic, the more positive of the two logic levels in a binary system. Normally, a high logic level is used to represent a binary 1 or true condition.
IC : (Integrated Circuit) A single piece of silicon on which thousands or millions of transistors are combined. ICs are the major building blocks of modern electronic systems.
Inverter: In logic, a digital circuit which inverts the input signal, as for example, changing a 1 to a 0. This is equivalent logically to the NOT function. An inverter may also serve as a buffer amplifier.
JK flip-flop: A type of flip-flop that can operate in the SET, RESET, no-change, and toggle modes.
Karnaugh map : An arrangement of cells representing the combinations of literals in a Boolean expression and used for a systematic simplification of the expression.
Latch: A bi-stable digital circuit used for storing a bit.
LED: Light-Emitting Diode (component) Abbreviated LED. A semiconductor diode, generally made from gallium arsenide, that can serve as an infrared or visible light source when voltage is applied continuously or in pulses.
Logic: One of the three major classes of ICs in most digital electronic systems: microprocessors, memory, and logic. Logic is used for data manipulation and control functions that require higher speed than a microprocessor can provide
Low: A logic state corresponding to a binary "0". Satellite imagery is displayed on a computer monitor by a combination of highs and lows.
Low logic : In digital logic, the more negative of the two logic levels in a binary system. In positive logic, a low-logic level is used to represent a logic 0, or a not-true, condition.
Mantissa: The magnitude of a floating-point number.
MSI: Medium-scale integration' a level of fixed-function IC complexity in which there are 12 to 99 equivalent gates per chip.
Multiplexer: An electronic device normally used to scan a number of input terminals and receive data from, or send data to, the same. Multiplexers are normally one of two types:
The **cyclic type** which continually and sequentially looks at each input for a request to send or receive data.
The **random type** which waits in a "rest" position until other circuitry notifies it of a request to receive or send data.
NAND gate : A logic circuit in which a LOW output occurs only if all the inputs are HIGH.
NOR gate : A logic circuit which performs the OR function and then inverts the result. A NOT-OR gate.
NOT : The logical operator having that property which if P is a statement, then the not of P (P) is true if P is false, and the not of P (P) is false if P is true.
octal : Describes a number system with a base of eight.

odd parity : The condition of having an odd number of 1s in every group of bits.
OR gate : A multiple-input gate circuit whose output is energized when any one or more of the inputs is in a prescribed state. Used in digital logic
overflow : The condition that occurs when the number of bits in a sum exceeds the number of bits in each of the numbers added.
PAL : Programmable array logic; an SPLD with a programmable AND array and a fixed OR array with programmable output logic.
parity : In relation to binary codes, the condition of evenness or oddness of the number of 1s in a code group.
parity bit : A bit attached to each group of information bits to make the total number of 1s in a code group.
PLA : Plogrammable logic array; an SPLD with programmable AND and OR arrays.
queue : A high-speed memory that stores instructions or data.
register : A digital circuit capable of storing and shifting binary information; typically used as a temporary storage device.
Shift : To move information serially right or left in a register(s). Information shifted out of a register may be lost, or it may be re-entered at the other end of the register.
Shift register : A shift register is an electronic device which can contain several bits of information. Shift registers are normally used to collect variable input data and send this data out in a predetermined pattern.
Sign bit : Computers generally indicate whether a number is positive or negative by a sign bit, which is usually located adjacent to the most significant numerical digit. Usually zero (0) is used for positive (+) and one (1) for negative (-).
Significant digit : A digit that contributes to the preciseness of a number. The number of significant digits is counted beginning with the digit contributing the most value, called the most significant digit, and ending with the one contributing the least value, called the least significant digit.
toggle : The action of flip-flop when it changes state on each clock pulse.
Truth Table : A table that defines a logic function by listing all combinations of input values, and indicating for each combination the true output values.
TTL : Transistor-transistor logic; a class of integrated logic circuits that uses bipolar junction transistors.
Universal gate : Either a NAND or a NOR gate; The term universal refers to the property of a gate that permits any logic function to be implemented by that gate or by a combination of gates of that kind.
up/down counter : A counter that can progress in either direction through a certain sequence.
VLSI : Very large-scale integration; a level of IC complexity in which there are 10,000 to 99,000 equivalent gates per chip.
volatile : A term that describes a memory that loses stored data when the power is removed.
Weight: The value of digit in a number based on its position in the number.

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Spring 2011 Latest Papers (Current)
Papers Number 01

Define decoder, Encoders , Multiplese , demultiplexer

Encoders: A digital circuit (device) that converts information to a coded form.

Decoders: Decoder : A logic function that uses a binary value, or address, to select between a number of outputs and to assert the selected output by placing it in its active state.

Multiplexer: An electronic device normally used to scan a number of input terminals and receive data from, or send data to, the same. Multiplexers are normally one of two types:

The cyclic type which continually and sequentially looks at each input for a request to send or receive data.

The random type which waits in a "rest" position until other circuitry notifies it of a request to receive or send data.

Demultiplexer : A Multiplexer has several inputs. It selects one of the inputs and routes the data at the selected input to the single output. Demultiplexer has an opposite function to that of the Multiplexer. It has a single input and several outputs. The Demultiplexer selects one of the several outputs and routes the data at the single input to the selected output. A demultiplexer is also known as a Data Distributor.

Some commonly used combinational functional devices are Comparators, Decoders, Encoders, Multiplexers and Demultiplexers.

Sequential Circuits:

Sequential logic and implementation Digital systems are used in vast variety of industrial applications and house hold electronic gadgets. Many of these digital circuits generate an output that is not only dependent on the current input but also some previously saved information which is used by the digital circuit.

Consider the example of a digital counter which is used by many digital applications where a count value or the time of the day has to be displayed. The digital counter which counts downwards from 10 to 0 is initialized to the value 10. When the counter receives an external signal in the form of a pulse the counter decrements the count value to 9. On receiving successive pulses the counter decrements the currently stored count value by one, until the counter has been decremented to 0. On reaching the count value zero, the counter could switch off a washing machine, a microwave oven or switch on an air-conditioning system.

Why S and R input of NAND based latch should not be at logic high at same time?

Thus, with S and R inputs both set to logic 1, the previous output state is maintained. If initially, the Q andQare at logic 1 and 0 respectively, setting S=1 and R=1 maintains the same outputs. Similarly, if initially Q and Q are at logic 0 and 1 respectively, setting S=1 and R=1 maintains the same outputs.

2 input 4 bit multiplexer function table 3 marks

2-INPUT 4-BIT MULTIPLEXER

The MSI, 74X157 is a 2-input, 4-bit Multiplexer. This multiplexer has two sets of 4-bit inputs. It also has 4-bit outputs. The single select input line allows the first set of four inputs or the second set of 4-inputs to be connected to the output. Thus four-bits of

data from two sources are routed to the output. The function table and the circuit of the multiplexer are shown. table 18.1, figure 18.1

The multiplexer has two sets of 4-bit active-high inputs 1A, 2A, 3A, 4A and 1B, 2B, 3B, 4B respectively. The multiplexer has 4-bit active-high outputs 1Y, 2Y, 3Y 4Y. The single select input allows either the 4-bit input A or the 4-bit input B to be connected to the 4-bit output Y.

The G active-low pin enables or disables the Multiplexer.

Inputs		Outputs			
G	S	1Y	2Y	3Y	4Y
1	X	0	0	0	0
0	0	1A	2A	3A	4A
0	1	1B	2B	3B	4B

Table 18.1 Function table of 2-Input 4-Bit Multiplexer

- BCD to decimal conversion of three BCDs codes 3marks
- Half adder explanation its function table Boolean expression and circuit diagram 5 marks
- Explain S-R latch in your own words

Mid-Term Past Papers (Updated Version)

Short Question (Set-1)

Question No: 18 (Marks: 2)

Provide some of the inputs for which the adjacent 1s detector circuit have active high output?

Ans:

The Adjacent 1s Detector accepts 4-bit inputs.

If two adjacent 1s are detected in the input, the output is set to high.

Some input combinations will be

1. 0011,
2. 0110,
3. 0111,
4. 1011,
5. 1100,
6. 1101,
7. 1110 and
8. 1111

The output function is a 1.

Question No: 19 (Marks: 2)

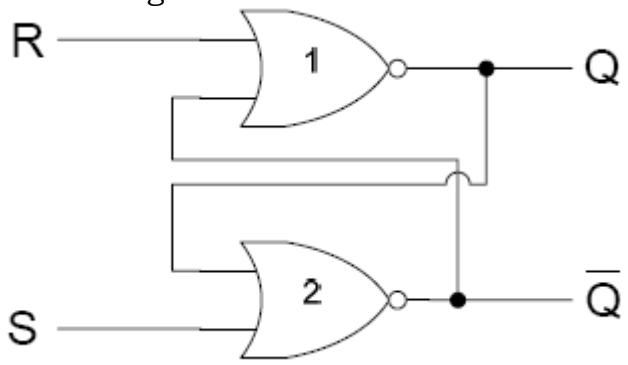
Draw the Truth-Table of NOR based S-R Latch

Answer:

Input		Output
S	R	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	invalid

Table 22.3 Truth-Table of NOR based S-R Latch

Circuit Diagram of NOR based S-R Latch.



NAND Based S-R Latch

Function Table:

Input		Output
S	R	Q_{t+1}
0	0	invalid
0	1	1
1	0	0
1	1	Q_t

Table 22.2 Truth-Table of NAND based S-R Latch

Circuit Diagram:

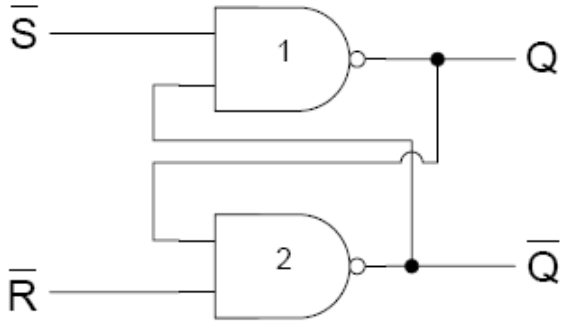


Figure 22.3 NAND based S-R Latch

Question No: 20 (Marks: 3)

For a two bit comparator circuit specify the inputs for which A > B

Ans:

1. 01 00,
2. 10 00,
3. 10 01,
4. 11 00,
5. 11 01
6. 11 10

Write a note on COMPARATOR

COMPARATOR

A comparator circuit compares two numbers and sets one of its three outputs to 1 indicating the result of the comparison operation. A Comparator circuit has multiple inputs and three outputs.

A 2-bit Comparator circuit compares two 2-bit numbers A and B. The comparator circuit has three outputs. It sets the A>B output to 1 if A>B. It sets the A=B output to 1 if A=B and sets A<B output to 1 if A < B.

• The output A>B is set to 1 when the input combinations are 01 00, 10 00, 10 01, 11 00, 11 01 and 11 10

• The output A=B is set to 1 when the input combinations are 00 00, 01 01, 10 10 and 11 11

• The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11

The circuit has 4-bit input, 2-bits represent A and 2-bits represent B and a 3-bit output representing A>B, A=B and A<B. To represent the function of a Comparator circuit, three function tables are required for each of the three outputs. A single function table is drawn with three outputs. Table 12.1.

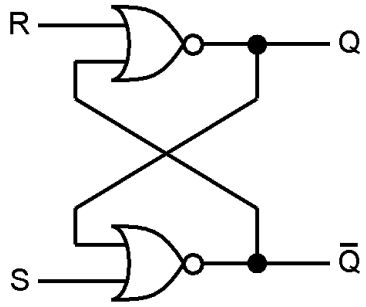
Input				Output		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Table 12.1 Function Table of a Comparator Circuit

Question No: 21 (Marks: 3)

Draw the circuit diagram of NOR based S-R Latch?

Ans:



Question No: 22 (Marks: 5)

One of the ABEL entry methods uses logic equations; explain it with at least a single example.

Ans:

In ABEL any letter or combination of letters and numbers can be used to identify variables.

ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'.

All ABEL equations must end with ';'

Boolean expression F = AB' + AC +(BD)' is written in ABEL as

F = A & !B # A & C # !B & !D;

Logic Operation	ABEL Symbol
NOT	!
AND	&
OR	#
XOR	$

Table 21.1 ABEL Symbols for logic operations

Question No: 23 (Marks: 5)

Explain Carry propagation in Parallel binary adder?

Ans:

Parralel binary adder:

A binary adder circuit is described using dynamic transistor logic in which for high speed carry propagation the adder stages are grouped in pairs or larger numbers and additional dynamic logic means is provided in each group to control a single transistor connected in series in the carry propagation path over the group.

The transistors used in the specific embodiments are MOS transistors, but some or all of these could be replaced by junction FET's or bipolar transistors

==========>

Short Question (Set-2)

Question No: 18 (Marks: 1)

Name any two modes in which PALs are programmed.

Ans:

PAL devices are programmed by blowing the fuses permanently using over voltage. PALs typically have 8 or more inputs to the AND array and 8 or less outputs from the fixed OR

array. Some PALs have combined inputs and outputs that can be programmed as either inputs or outputs

Question No: 19 (Marks: 2)

Explain Combinational Function Devices?

Ans;
XOR,XNOR,NAND,NOR are combinational function devices.

Question No: 20 (Marks: 3)

Differentiate between hexadecimal and octal number system

Octal - base 8
Hexadecimal - base 16
Octal and hex are used to represent numbers instead of decimal because there is a very easy and direct way to convert from the "real" way that computers store numbers (binary) to something easier for humans to handle (fewer symbols). To translate a binary number to octal, simply **group the binary digits three** at a time and convert each group. For hex, **group the binary digits four at a time**.

Question No: 21 (Marks: 5)

Explain "Sum-of-Weights Method" for Hexadecimal to Decimal Conversion with at least one example ?

Ans:
The hexadecimal (Hex) numbering system provides even shorter notation than octal. Hexadecimal uses a base of 16. It employs 16 digits: number 0 through 9, and letters A through F, with A through F substituted for numbers 10 to 15, respectively,
Hexadecimal numbers can be expressed as their decimal equivalents by using the sum of weights method, as shown in the following example:

Weight	2	1	0	
Hex. Number	1	B	7	
				$7 \times 16^0 = 7 \times 1 = 7$
				$11 \times 16^1 = 11 \times 16 = 176$
				$1 \times 16^2 = 1 \times 256 = 256$
				Sum of products 439_{10}

Like octal numbers, hexadecimal numbers can easily be converted to binary or vise versa. Conversion is accomplished by writing the 4-bit binary equivalent of the hex digit for each position, as illustrated in the following example:

Hex. Number 1 B 7

0001 1011 0111 ← Binary number

Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3

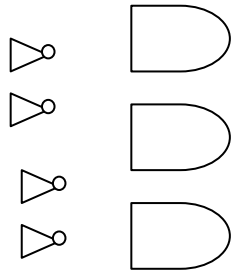
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

Question No: 22 (Marks: 10)

Draw the function table of two-bit comparator circuit, map it to K-Map and derive the expression for (A > B)

Ans:

X_1	X_0	Y_1	Y_0	X<Y	X=Y	X>Y
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0



The circuit has inputs X_1X_0 and Y_1Y_0 and outputs X > Y, the expression for > is

$X_1 \overline{Y_1} + X_0 \overline{Y_1} \overline{Y_0} + X_1 X_0 \overline{Y_0}$

==========>

Short Question (Set-3)

Question:

How SOP is converted into POS ? 3mark

Answer:

Converting Standard SOP into Standard POS

The binary values of the product terms in a given standard SOP expression are not present in the equivalent standard POS expression. Also, the binary values that are not represented in the SOP expression are present in the equivalent POS expression.

$\overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C + ABC$ has the binary values 000, 010,011,101 and 111

Canonical Sum = $\sum_{A,B,C}(0,2,3,5,7) = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C + ABC$

The missing binary values are 001, 100 and 110.

The POS expression is $(A + B + \overline{C})(\overline{A} + B + C)(\overline{A} + \overline{B} + C)$

Question:

S-R latch Diagram 5mark

Answer:

Two NAND base S-R Latch (Set-Reset)

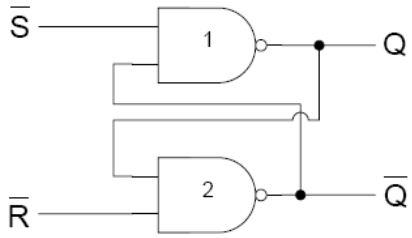
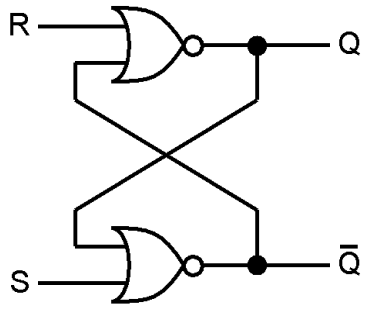


Figure 22.3 NAND based S-R Latch

Two NOR base S-R Latch (Set-Reset)



Question:

Write NOR gate table 3mark

Answer:

Logical NOR Operation		
Inputs		Output
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Write NAND gate table 3mark

Answer:

Logical NAND Operation		
Inputs		Output
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Write XOR gate table 3mark

Answer:

Logical XOR Operation		
Inputs		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Question:

8 to 3 bit encoder 5mark

Answer:

Encoder

An Encoder functional device performs an operation which is the opposite of the Decoder function. The Encoder accepts an active level at one of its inputs and at its output generates a BCD or Binary output representing the selected input. There are various types of Encoders that are used in Combinational Logic Circuits.

Binary Encoder

The simplest of the Encoders are the 2n-to-n Encoders. The functional table and the circuit diagram of an 8-to-3 Binary Encoder are shown in table 17.2 and figure 17.6 respectively.

Input								Output		
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	O_2	O_1	O_0
X	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	1
X	0	1	0	0	0	0	0	0	1	0
X	0	0	1	0	0	0	0	0	1	1

X	0	0	0	1	0	0	0	1	0	0
X	0	0	0	0	1	0	0	1	0	1
X	0	0	0	0	0	1	0	1	1	0
X	0	0	0	0	0	0	1	1	1	1

Table 17.2 Function Table of an 8-to-3 Encoder

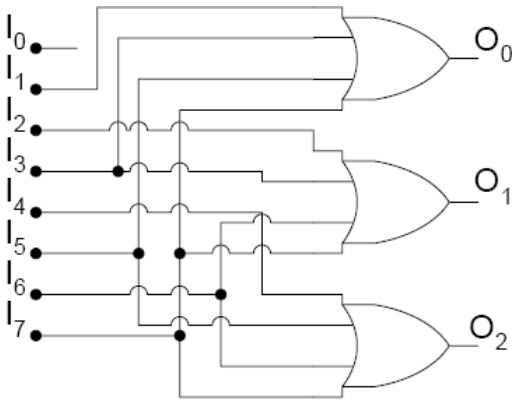


Figure 17.6 8-to-3 Encoder

Question:

Tri-stuff diagram 3mark

Answer:

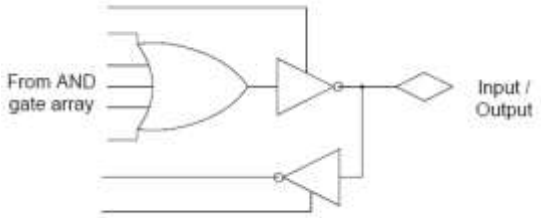


Figure 19.12b Combinational Input/Output with active-low output

The output of the OR gate from the OR gate Array is shown to be connected to a tri-state buffer input. The tri-state buffer can be activated or deactivated through the control line shown connected to its side. The Combinational Output for an SOP function is implemented by activating the tri-state buffer which allows the output of the OR gate to be inverted by the tri-state buffer and passed to the output of the PAL device. An active-high output can be obtained if the PAL device has active-high output tri-state buffers.

==========>

Short Question (Set-4)

Question No: 17 (Marks: 2)

For what values of A, B, C and D, value of the expression given below will be logic 1. Explain at least one combination.

$\overline{A.\overline{B} + \overline{A}.\overline{B}.C.D}$

Ans:

Write the uses of multiplexer. 2 marks question

The Multiplexers are used to route the contents of any two registers to the ALU inputs.
Many Audio signals in telephone network.
Computer use Dynamic Memory addressing using same address line for row and column addressing to access data.

Write any two advantages of Boolean expressions. 2 marks question

Boolean expressions which represent Boolean functions help in two ways. The function and operation of a Logic Circuit can be determined by Boolean expressions without implementing the Logic Circuit. Secondly, Logic circuits can be very large and complex. Such large circuits having many gates can be simplified and implemented using fewer gates. Determining a simpler Logic circuit having fewer gates which is identical to the original logic circuit in terms of the function it performs can be easily done by evaluating and simplifying Boolean expressions.

Draw the diagram of odd parity generator circuit. 2 marks question

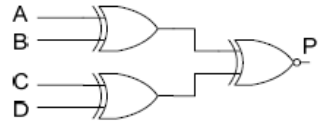


Figure 14.2 Odd-Parity Generator Circuit

2 XOR and 1 XNOR gate is used.

What does a 8-bit adder/subtracter circuit do"? 3 marks question

An 8-bit Adder/Subtracter Unit
Two 4-bit 74LS283 chips can be cascaded together to form an 8-bit Parallel Adder Unit. Each of the two 74LS283 ICs is connected to the 1's Complement circuitry that allows either the un-complemented form for addition or the complemented form for subtraction to be applied at the B inputs of the two 74LS283s. Figure 15.8 The 8-bit Adder/Subtracter Circuit is similar to the 4-bit Adder/Subtracter Circuit. Two sets of AND-OR based circuit that allows complemented and un-complemented B input to be applied at the B inputs of the two 4-bit Adders. The Add/Subtract function select input are tied together. The Carry In of the 1st 4-bit Adder circuit is connected to the Add/Subtract function select input. The Carry Out of the 1st 4-bit Adder circuit is connected to the Carry In of the 2nd 4-bit Adder circuit

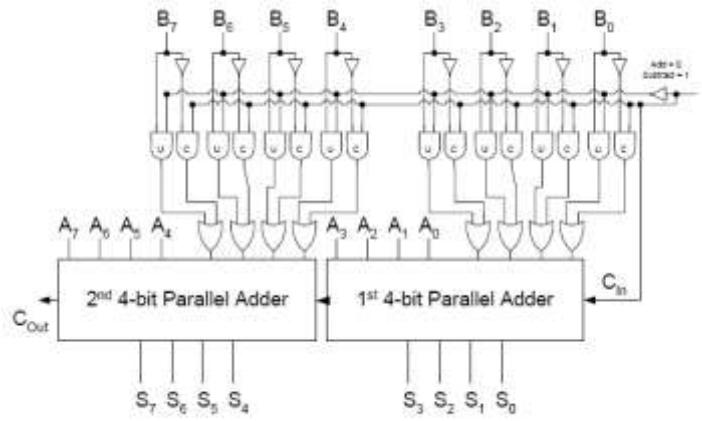


Figure 15.8 8-bit Adder/Subtracter Circuit

Draw the function table of 3 to 8 decoder. 3 marks question

THE 74XX138 3-TO-8 DECODER

The 3-to-8, 74XX138 Decoder is also commonly used in logical circuits. Similar, to the 2-to-4 Decoder, the 3-to-8 Decoder has active-low outputs and three extra NOT gates connected at the three inputs to reduce the four unit load to a single unit load. The 3-to-8 Decoder has three enable inputs, one of the three enable inputs is active-high and the remaining two are active-low. All three enable inputs have to be activated for the Decoder to work. The function table of the 3-to-8 decoder is presented. Table 17.1

Inputs						Outputs							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y7}$	$\overline{Y6}$	$\overline{Y5}$	$\overline{Y4}$	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

Table 17.1 Function Table of 74LS138, 3-to-8 Decoder

Describe 16 bit ALU". 5 Marks

Implementing 16-bit ALU

16-bit ALU can be implemented by cascading together four 4-bit ALUs. These 4-bit ALUs have built in Look-Ahead Carry Generator circuits that eliminate the delay caused by carry bit propagating through the Parallel Adder circuit within the 4-bit ALU circut. However, when a number of such units are cascaded together to implement large 16-bit and 32-bit ALU, the carry propagating between one unit to the next gets delayed due to the Carry rippling

through multiple 4-bit units. For large 32-bit ALUs, the Carry propagates through 8, 4-bit units delaying the Carry out from the last most significant unit by a factor of 8.The 74XX181 and 74XX381 circumvent the problem by having Group-Carry Look-Ahead.

Describe in your own words about latches". 5 Marks

See the answer above S-R latch using NAND and NOR

==========>

Short Question (Set-5)

Question No: 17 (Marks: 2)

Why a 2-bit comparator is called parallel comparator?

The 2-bit Comparator discussed earlier is considered to be a Parallel Comparator as all the bits are compared simultaneously. External Logic has to be used to Cascade together two such Comparators to form a 4-bit Comparator.

Question No: 18 (Marks: 2)

Explain at least two advantages of the circuit having low power consumption

Power Dissipation

Logic Gates and Logic circuits consume varying amount of power during their operation. Ideally, logic gates and logic circuit should consume minimal power. Advantages of low power consumption are circuits that can be run from batteries instead of mains power supplies. Thus portable devices that run on batteries use Integrated circuits that have low power dissipation. Secondly, low power consumption means less heat is dissipated by the logic devices; this means that logic gates can be tightly packed to reduce the circuit size without having to worry about dissipating the access heat generated by the logic devices.

Microprocessors for example generate considerable heat which has to be dissipated by mounting small fans. Generally, the Power dissipation of TTL devices remains constant throughout their operation. CMOS device on the other hand dissipate varying amount power depending upon the frequency of operation.

Question No: 19 (Marks: 2)

Name the four OLMC configurations

A typical GAL has eight or more inputs to the reprogrammable AND array and 8 or more input/outputs from its 'Output Logic Macro Cells' OLMCs. The OLMCs can be programmed to Combinational Logic or Registered Logic. Combinational Logic is used for combinational circuits, where as Registered Logic is based on Sequential circuits.

The four OLMC configurations are

- Combination Mode with active-low output
- Combinational Mode with active-high output
- Registered Mode with active-low output
- Registered Mode with active-high output

Question No: 20 (Marks: 3)

Explain "Test Vector" in context of ABEL

Test Vectors

Once the Logic circuit design has been entered its operation can be verified by using 'test vectors'. A 'test vector' specifies the inputs and the corresponding outputs. The software simulates the operation of the logic circuit by applying the test vectors and checking the outputs.

Test vectors are essentially the same as Truth Tables. Thus the Test Vector for testing the 2-bit comparator circuit is the same as its truth table.

Question No: 21 (Marks: 3)

For a two bit comparator circuit specify the inputs for which the output A < B is set to 1

This question is answer above in detail.

Question No: 23 (Marks: 5)

Explain the Operation of Odd-Parity Generator Circuit with the help of timing diagram

Operation of Odd-Parity Generator Circuit

The timing diagram shows the operation of the Odd-Parity generator circuit. Figure 14.3. The A, B, C and D timing diagrams represent the changing 4-bit data values. During time interval t0 the 4-bit data value is 0000, during time interval t1, the data value changes to 0001.

Similarly during time intervals t2, t3, t4 up to t8 the data values change to 0010, 0011, 0100 and 1000 respectively. During interval t0 the output of the two XOR gates is 0 and 0, therefore the output of the XNOR gate is 1. At interval t1, the outputs of the two XOR gates is 1 and 0, therefore the output of the XNOR gate is 0. The output P can similarly be traced for intervals t2 to t8.

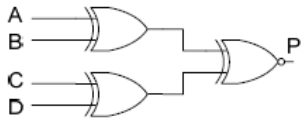


Figure 14.2 Odd-Parity Generator Circuit

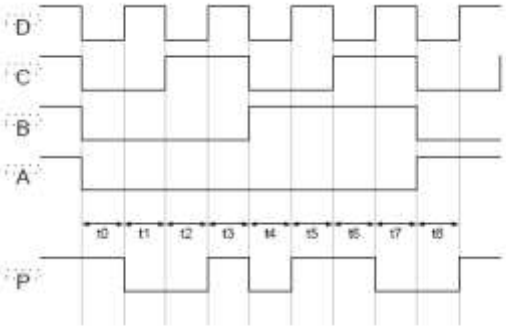


Figure 14.3 Timing Diagram of Odd-Parity Generator Circuit

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Short Question (Set-6)

Question No: 17 (Marks: 1)

How can a PLD be programmed?

PLDs are programmed with the help of computer which runs the programming software. The computer is connected to a programmer socket in which the PLD is inserted for programming. PLDs can also be programmed when they are installed on a circuit board

Question No: 18 (Marks: 1)

How many input and output bits do a Half-Adder contain?

The Half-Adder has a 2-bit input and a 2-bit output.

Question No: 19 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer 2-to-4 Binary Decoder?

The circuit of the 1-to-4 Demultiplexer is similar to the 2-to-4 Binary Decoder described earlier figure 16.9. The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit figure

Question No: 20 (Marks: 3)

Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL.

- Device declaration,
- Pin declarations
- Set declarations

Question No: 21 (Marks: 5)

Explain with example how noise affects Operation of a CMOS AND Gate circuit.

Two CMOS 5 volt series AND gates are connected together. Figure 7.3 The first AND gate has both its inputs connected to logic high, therefore the output of the gate is guaranteed to be logic high. The logic high voltage output of the first AND gate is assumed to be 4.6 volts well within the valid VOH range of 5-4.4 volts. Assume the same noise signal (as described earlier) is added to the output signal of the first AND gate.

Question No: 22 (Marks: 10)

Explain the SOP based implementation of the Adjacent 1s Detector Circuit

Answer:

The Adjacent 1s Detector accepts 4-bit inputs. If two adjacent 1s are detected in The input, the output is set to high. The operation of the Adjacent 1s Detector is represented by the function table. Table 13.6. In the function table, for the input combinations 0011, 0110, 0111, 1011, 1100, 1101, 1110 and 1111 the output function is a 1.

Implementing the circuit directly from the function table based on the SOP form requires 8 AND gates for the 8 product terms (minterms) with an 8-input OR gate. Figure 13.3.

The total gate count is

• One 8 input OR gate
• Eight 4 input AND gates
• Ten NOT gates

The expression can be simplified using a Karnaugh map, figure 13.4, and then the simplified expression can be implemented to reduce the gate count. The simplified expression is AB + CD +BC . The circuit implemented using the expression AB + CD +BC has reduced to 3 input OR gate and 2 input AND gates.

The simplified Adjacent 1s Detector circuit uses only four gates reducing the cost, The size of the circuit and the power requirement. The propagation delay of the circuit is of the order of two gates.

==========>

Short Question (Set-7)

Question No: 17 (Marks: 2)

For what values of A, B, C and D, value of the expression given below will be logic 1. Explain at least one combination A.B + A.B.C.D

Ans:
It is very easy.

Question No: 20 (Marks: 3)

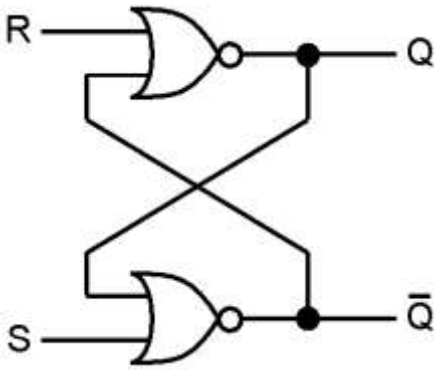
For a two bit comparator circuit specify the inputs for

which A > B
Ans:
1. 01 00,
2. 10 00,
3. 10 01,
4. 11 00,
5. 11 01 and
6. 11 10

Question No: 21 (Marks: 3)

Draw the circuit diagram of NOR based S-R Latch ?

Ans:



Question No: 23 (Marks: 5)

Explain Carry propagation in Parallel binary adder?

Ans:
Parralel binary adder:
A binary adder circuit is described using dynamic transistor logic in which for high speed carry propagation the adder stages are grouped in pairs or larger numbers and additional dynamic logic means is provided in each group to control a single transistor connected in series in the carry propagation path over the group. The transistors used in the specific embodiments are MOS transistors, but some or all of these could be replaced by junction FET's or bipolar transistors.
==========>

Short Question (Set-9)

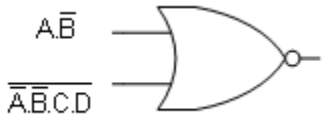
Question No: 18 (Marks: 1)

How standard Boolean expressions can be converted into truth table format.

Standard Boolean expressions can be converted into truth table format using binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.

Question No: 19 (Marks: 2)

What will be the out put of the diagram given below



A.B + A.B.C.D

Question No: 21 (Marks: 5)

Explain “AND” Gate and some of its uses

AND gates are used to combine multiple signals, if all the signals are TRUE then the output will also be TRUE. If any of the signals are FALSE, then the output will be false. ANDs aren't used as much as NAND gates; NAND gates use less components and have the advantage that they be used as an inverter.

Question No: 22 (Marks: 10)

Write down different situations where we need the sequential circuits.

Digital circuits that use memory elements for their operation are known as Sequential circuits. Thus Sequential circuits are implemented by combining combinational circuits with memory elements.

==========>

Short Question (Set-10)

Question No: 18 (Marks: 1)

Briefly state the basic principle of Repeated Multiplication-by-2 Method.

Repeated Multiplication-by-2 Method

An alternate to the Sum-of-Weights method used to convert Decimal fractions to equivalent Binary fractions is the repeated multiplication by 2 method. In this method the number to be converted is repeatedly multiplied by the Base Number to which the number is being converted to, in this case 2. A new number having an Integer part and a Fraction part is generated after each multiplication. The Integer part is noted down and the fraction part is again multiplied with the Base number 2. The process is repeated until the fraction term becomes equal to zero.

Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary. The conversion of Decimal fraction 0.625 into Binary equivalent using the Repeated Multiplication-by-2 method is illustrated in a tabular form. Table 2.4. Reading the Integer column from bottom to top and placing a decimal point in the left most position gives 0.101 the binary equivalent of decimal fraction 0.625

Question No: 19 (Marks: 2)

Draw the circuit diagram of a Tri-State buffer.

See the answer above...

Question No: 20 (Marks: 3)

Add -13 and +7 by converting them in binary system your result must be in binary.

Do at yourself

Hint first conver -13 in 2’s Complemeent Form and then perform subbstration

Question No: 21 (Marks: 5)

Explain “Sum of Weights” method with example for “Octal to Decimal” conversion

1. Sum-of-Weights Method

Sum-of-weights as the name indicates sums the weights of the Binary Digits (bits) of a Binary Number which is to be represented in Decimal. The Sum-of-Weights method can be used to convert a Binary number of any magnitude to its equivalent Decimal representation.
In the Sum-of-Weights method an extended expression is written in terms of the Binary Base Number 2 and the weights of the Binary number to be converted. The weights correspond to each of the binary bits which are multiplied by the corresponding binary value. Binary bits having the value 0 do not contribute any value towards the final sum expression.
The Binary number 101102 is therefore written in the form of an expression having weights 0 1 2 ,2 ,22 ,23 AND 24 corresponding to the bits 0, 1, 1, 0 and 1 respectively.Weights 20AND 23 do not contribute in the final sum as the binary bits corresponding to these weights have the value 0.
101102 = 1 x 24 □ 0 x 23 □ 1 x 22 □ 1 x 21 □ 0 x 20
= 16 + 0 + 4 + 2 + 0
= 22

==========>

Short Question (Set-11)

Question No: 17 (Marks: 1)

Briefly state the basic principle of Repeated Multiplication-by-2 Method.

Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary.

Question No: 18 (Marks: 1)

How standard Boolean expressions can be converted into truth table format.

Standard Boolean expressions can be converted into truth table format using binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.

Question No: 20 (Marks: 3)

When an Input (source) file is created in ABEL a module is created which has three sections. Name These three sections.

Answer:
The three sections are:
1. Declarations
The declaration section generally includes the device declaration, pin declarations and set declarations. Device declaration is used to specify the PLD device that is to be programmed. The device is referred to as the target device.
Decoder device 'P22V10';
2. Logic Descriptions
Logic descriptions include the three methods of describing a logic circuit. Two methods the Boolean equation and the Truth Table method already have been discussed.
3. Test Vectors
The Test Vector format has been described. The Test vector description is used to simulate the logic circuit and verify its operation.

Question No: 21 (Marks: 5)

Explain "AND" Gate and some of its uses

AND gates are used to combine multiple signals, if all the signals are TRUE then the output will also be TRUE. If any of the signals are FALSE, then the output will be false. ANDs aren't used as much as NAND gates; NAND gates use less components and have the advantage that they be used as an inverter.

Question No: 22 (Marks: 2)

Write down different situations where we need the sequential circuits.

Digital circuits that use memory elements for their operation are known as Sequential circuits. Thus Sequential circuits are implemented by combining combinational circuits with memory elements.

Question No: 23 (Marks: 5)

Explain “OR” Gate and some of its uses

OR gates are used to combine multiple signals, if any the signals are TRUE then the output will also be TRUE. If all of the signals are FALSE, then the output will be false. ORs aren't used as much as NOR gates; NOR gates use less components and have the advantage that they be used as an inverter.

==========>

Short Question (Set-12)

==========>

MCQz

MCQz (Set-1)

Question No: 1 (Marks: 1) -

The maximum number that can be represented using unsigned octal system is _____

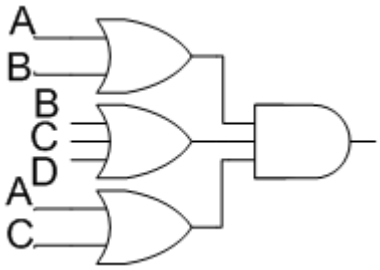
- ► 1
- ► 7
- ► 9
- ► 16

Question No: 2 (Marks: 1) -

If we add “723” and “134” by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

- ► 0
- ► 1
- ► **2**
- ► 3

Question No: 3 (Marks: 1) -
The diagram given below represents _____



- ▶ Demorgans law
- ▶ Associative law
- ▶ **Product of sum form**
- ▶ Sum of product form

Question No: 4 (Marks: 1) -
The range of Excess-8 code is from _____ to _____

- ▶ **+7 to -8 , pg no 34**
- ▶ +8 to -7
- ▶ +9 to -8
- ▶ -9 to +8

Question No: 5 (Marks: 1) -
A non-standard POS is converted into a standard POS by using the rule _____

- ▶ $A+\overline{A}=1$
- ▶ $A\overline{A}=0$
- ▶ $1+A=1$
- ▶ A+B = B+A

Question No: 6 (Marks: 1) -
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

- ▶ 4
- ▶ **8 (Formula, total cell=$2^{\text{(no. of variables)}}$**
- ▶ 12
- ▶ 16

Question No: 7 (Marks: 1) -
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

- ▶ A > B = 1, A < B = 0, A < B = 1

► A > B = 0, A < B = 1, A = B = 0
► **A > B = 1, A < B = 0, A = B = 0 (page 109)**
► A > B = 0, A < B = 1, A = B = 1

Reference pg 109
(The output **A>B is set to** 1 when the input combinations are 01 00, 10 00, **10 01**, **11 00**, 11
01 and 11 10
• The output A=B is set to 1 when the input combinations are 00 00, 01 01, 10 10 and 11 11
• The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01
11 and 10 11

Question No: 8 (Marks: 1) -
A particular Full Adder has

► **3 inputs and 2 output (pg 134)**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 9 (Marks: 1) -
The function to be performed by the processor is selected by set of inputs known as _____

► Function Select Inputs (pg 147)
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) -
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2 pg 160**
► 1
► 3
► 4

Question No: 11 (Marks: 1) -
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic pg 183**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) -
The Quad Multiplexer has _____ outputs

► 4

► 8
► 12
► **16 pg 217**

Question No: 13 (Marks: 1) -
A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law pg 72**

Question No: 14 (Marks: 1) -
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) -
The binary value "1010110" is equivalent to decimal _____

► **86 proof very simple use scientific calculator.**
► 87
► 88
► 89

Question No: 16 (Marks: 1) -
Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► **XOR pg 186**

==========>

MCQz (Set-2)

Select the best possible choice.O

a) A NOR's gate output is HIGH if

I. all inputs are HIGH
II. II. any input is HIGH
III. any input is LOW
IV. all inputs are LOW

b) A demultiplexer has

I. one input and several outputs pg 178

II. one input and one output
III. several inputs and several outputs
IV. several inputs and one output

c) The difference of 111 - 001 equals

I. 100

II. 111
III. 001
IV. 110

e) Which gate is best used as a basic comparator?

I. NOR
II. II. OR
III. exclusive-OR
IV. IV. AND

==========>

MCQz (Set-3)

Question No: 1 (Marks: 1) -

According to Demorgan's theorem:

$\overline{A+B+C} =$

- A.B.C
- $A+\overline{B.C}$
- $\overline{A}.\overline{B}.\overline{C}$
- $\overline{A.B}+C$

Question No: 2 (Marks: 1) -

The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

- 2-bit
- 7-bit
- **8-bit pg 38**
- 16-bit

Question No: 3 (Marks: 1) -

The AND Gate performs a logical _____function

- Addition
- Subtraction
- **Multiplication pg 40**
- Division

Question No: 4 (Marks: 1) -
NOR gate is formed by connecting _____

► **OR Gate and then NOT Gate pg 48**
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 5 (Marks: 1) -
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► **TTL pg 65**
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Question No: 6 (Marks: 1) -
Two 2-bit comparator circuits can be connected to form single 4-bit comparator
► **True pg 154**
► False

Question No: 7 (Marks: 1) -
When the control line in tri-state buffer is high the buffer operates like a _____ gate

► AND
► OR
► **NOT pg 196**
► XOR

Question No: 8 (Marks: 1) -
The GAL22V10 has ____ inputs

► **22 pg 197**
► 10
► 44
► 20

Question No: 9 (Marks: 1) -
The ABEL symbol for “OR” operation is

► !
► &
► **# ref see picture on pg 201**
► $

Logic Operation	ABEL Symbol
NOT	!
AND	&
OR	#
XOR	$

Question No: 10 (Marks: 1) -
The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► **Similar pg 207**
► Different
► Similar with some enhancements
► Depends on the type of PALs input size

Question No: 11 (Marks: 1) -
All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► **" ; " (a semicolon) pg 210**
► " endl " (keyword "endl")

Question No: 12 (Marks: 1) -
The Quad Multiplexer has _____ outputs

► 4
► 8
► 12
► 16

Question No: 13 (Marks: 1) -
"Sum-of-Weights" method is used _____

► **to convert from one number system to other**
► to encode data
► to decode data
► to convert from serial to parralel data

Question No: 14 (Marks: 1) -
Circuits having a bubble at their outputs are considered to have an active-low output.

► False
► **True pg # 128**

Question No: 15 (Marks: 1) -
$(A+B)(A+\overline{B}+C)(\overline{A}+C)$ is an example of _____

► **Product of sum form**

- ► Sum of product form
- ► Demorgans law
- ► Associative law

Question No: 16 (Marks: 1) -
Which one is true:

- ► **Power consumption of TTL is higher than of CMOS pg 58**
- ► Power consumption of CMOS is higher than of TTL
- ► Both TTL and CMOS have same power consumption
- ► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

Question No: 17 (Marks: 1)
Which device performs an operation which is the opposite of the Decoder function?

Ans:
Encoder function. Pg 163

==========>

MCQz (Set-4)

Question No: 1 (Marks: 1) -
A SOP expression is equal to 1 _____

- ► All the variables in domain of expression are present
- ► At least one variable in domain of expression is present.
- ► When one or more product terms in the expression are equal to 0.
- ► **When one or more product terms in the expression are equal to 1. Pg 86**

Question No: 2 (Marks: 1) -
The output A < B is set to 1 when the input combinations is _____

- ► A=10, B=01
- ► A=11, B=01
- ► A=01, B=01
- ► A=01, B=10

The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11 pg 109

Question No: 3 (Marks: 1) -
Two 2-bit comparator circuits can be connected to form single 4-bit comparator

- ► **True**
- ► False

Question No: 4 (Marks: 1) -
High level Noise Margins (V_{NH}) of CMOS 5 volt series circuits is _____

► 0.3 V
► 0.5 V
► **0.9 V pg 65**
► 3.3 V

Question No: 5 (Marks: 1) -
If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____

► 24.582
► **2.4582**
► 24582
► 0.24582

Question No: 6 (Marks: 1) -
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.
► Undefined
► **One in OR , if any is one output is 1**
► Zero
► 10 (binary)

Question No: 7 (Marks: 1) -
If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► **SET pg 220**
► RESET
► Clear
► Invalid

Question No: 8 (Marks: 1) -
3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation
► Fast switching speeds, high power dissipation
► **Fast switching speeds, very low power dissipation pg 61**
► Low switching speeds, very low power dissipation

Question No: 9 (Marks: 1) -
The binary value "1010110" is equivalent to decimal _____

► **86**

- ▶ 87
- ▶ 88
- ▶ 89

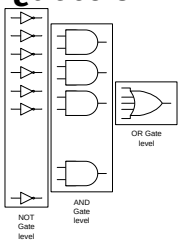
Question No: 10 (Marks: 1) -
The _____ Encoder is used as a keypad encoder.

- ▶ 2-to-8 encoder
- ▶ 4-to-16 encoder
- ▶ BCD-to-Decimal
- ▶ **Decimal-to-BCD Priority pg 166**

Question No: 11 (Marks: 1) -
How many data select lines are required for selecting eight inputs?

- ▶ 1
- ▶ 2
- ▶ 3
- ▶ 4

Question No: 12 (Marks: 1) -



the diagram above shows the general implementation of _____ form

- ▶ boolean
- ▶ arbitrary
- ▶ **POS**
- ▶ SOP

Question No: 13 (Marks: 1) -
The Quad Multiplexer has _____ outputs

- ▶ 4
- ▶ 8
- ▶ 12
- ▶ **16**

Question No: 14 (Marks: 1) -
Demultiplexer has

- ▶ Single input and single outputs.
- ▶ Multiple inputs and multiple outputs.
- ▶ **Single input and multiple outputs.**
- ▶ Multiple inputs and single output.

Question No: 15 (Marks: 1) -

The expression _____ is an example of Commutative Law for Multiplication.

- ► AB+C = A+BC
- ► A(B+C) = B(A+C)
- ► **AB=BA pg 72**
- ► A+B=B+A

Question No: 16 (Marks: 1) -
"Sum-of-Weights" method is used _____

- ► **to convert from one number system to other**
- ► to encode data
- ► to decode data
- ► to convert from serial to parralel data

==========>

MCQz (Set-5)

Question No: 1 (Marks: 1) -
In the binary number "10011" the weight of the most significant digit is ____

- ► **2^4 (2 raise to power 4)**
- ► 2^3 (2 raise to power 3)
- ► 2^0 (2 raise to power 0)
- ► 2^1 (2 raise to power 1)

Question No: 2 (Marks: 1) -
An S-R latch can be implemented by using _____ gates

- ► AND, OR
- ► **NAND, NOR (pg#218,220)**
- ► NAND, XOR
- ► NOT, XOR

Question No: 3 (Marks: 1) -
A latch has _____ stable states

- ► One
- ► **Two pg218**
- ► Three
- ► Four

Question No: 4 (Marks: 1) -
Sequential circuits have storage elements

- ► **True pg398**
- ► False

Question No: 5 (Marks: 1) -

The ABEL symbol for "XOR" operation is

- ► $ pg210
- ► #
- ► !
- ► &

Question No: 6 (Marks: 1) -
A Demultiplexer is not available commercially.

- ► True pg#178
- ► False

Question No: 7 (Marks: 1) -
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

- ► A parallel to serial converter circuit pg#244
- ► A counter circuit
- ► A BCD to Decimal decoder
- ► A 2-to-8 bit decoder

Question No: 9 (Marks: 1) -
The main use of the Multiplexer is to

- ► Select data from multiple sources and to route it to a single Destination pg#167
- ► Select data from Single source and to route it to a multiple Destinations
- ► Select data from Single source and to route to single destination
- ► Select data from multiple sources and to route to multiple destinations

Question No: 11 (Marks: 1) -
The binary value of 1010 is converted to the product term $\overline{A}B\overline{C}D$

- ► True
- ► False because A=1, A(bar)=0

Question No: 12 (Marks: 1) -
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

- ► 4
- ► 8 pg#89
- ► 12
- ► 16

Question No: 13 (Marks: 1) -
Following is standard POS expression
$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$

► True
► **False pg#99 (A +B + C).(A +B + C).(A +B + C).(A +B + C)**

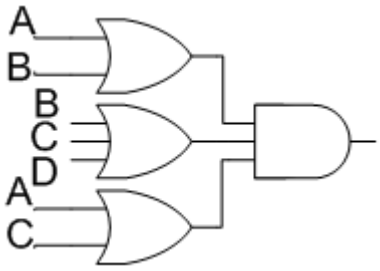
Question No: 14 (Marks: 1) -
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

► Undefined
► **One**
► Zero
► 10 (binary)

Question No: 15 (Marks: 1) -
The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► **8-bit pg#38**
► 16-bit

Question No: 16 (Marks: 1) -
The diagram given below represents _____



► Demorgans law
► Associative law
► **Product of sum form pg#78**
► Sum of product form

==========>

MCQz (Set-6)

Question No: 1 (Marks: 1) -
GAL can be reprogrammed because instead of fuses _____ logic is used in it

► **E^2CMOS pg 192**
► TTL
► CMOS+

► None of the given options

Question No: 3 (Marks: 1) -
If "1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

► 2^{nd}
► 4^{th}
► 14^{th}
► **No output wire will be activated pg 163**

Question No: 4 (Marks: 1) -
Half-Adder Logic circuit contains 2 XOR Gates
► True
► False

Question No: 5 (Marks: 1) -
A particular Full Adder has
► **3 inputs and 2 output pg 34**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 6 (Marks: 1) -
$Sum = A \oplus B \oplus C$
$CarryOut = C(A \oplus B) + AB$
are the Sum and Carry Out expression of
► Half Adder
► Full Adder
► 3-bit parralel adder
► MSI adder cicuit

Question No: 7 (Marks: 1) -
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.
► **True**
► False

Question No: 8 (Marks: 1) -
The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► A=01, B=10
The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11

Question No: 9 (Marks: 1) -
The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

- ▶ 4
- ▶ 8
- ▶ 12
- ▶ **16**

Question No: 10 (Marks: 1) -
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

- ▶ **TTL**
- ▶ CMOS 3.5 series
- ▶ CMOS 5 Series
- ▶ Power dissipation of all circuits increases with time.

Question No: 11 (Marks: 1) -
The decimal "8" is represented as _____ using Gray-Code.

- ▶ 0011
- ▶ **1100** **pg 36**
- ▶ 1000
- ▶ 1010

Question No: 12 (Marks: 1) -
(A+B).(A+C) = _____

- ▶ B+C
- ▶ A+BC
- ▶ AB+C
- ▶ AC+B

Question No: 13 (Marks: 1) -
A.(B + C) = A.B + A.C is the expression of _____

- ▶ Demorgan's Law
- ▶ Commutative Law
- ▶ Distributive Law
- ▶ **Associative Law**

Question No: 14 (Marks: 1) -
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**
► TRUE

Question No: 15 (Marks: 1) -
In ANSI/IEEE Standard 754 "Mantissa" is represented by ___23-bits_____ bits

► 8-bits
► 16-bits
► 32-bits
► 64-bits
23-bits page # 24

Question No: 16 (Marks: 1) -
Caveman number system is Base _5_____ number system

► 2
► **5**
► 10
► 16
==========>

MCQz (Set-7)

Question No: 1
The maximum number that can be represented using unsigned octal system is _____
► 1
► **7**
► 9
► 16
Question No: 2
If we add "723" and "134" by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent
of result will be _____
► 0
► 1
► **2**
► 3
Question No: 4
The range of Excess-8 code is from _____ to _____
► **+7 to -8**
► +8 to -7
► +9 to -8
► -9 to +8
Question No: 6
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
► 4
► **8**
► 12

► 16

Question No: 8

A particular Full Adder has

► **3 inputs and 2 output**

► 3 inputs and 3 output

► 2 inputs and 3 output

► 2 inputs and 2 output

Question No: 9

The function to be performed by the processor is selected by set of inputs known as _____

► **Function Select Inputs**

► MicroOperation selectors

► OPCODE Selectors

► None of given option

Question No: 10

For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2**

► 1

► 3

► 4

Question No: 11

GAL is an acronym for _____.

► Giant Array Logic

► **General Array Logic**

► Generic Array Logic

► Generic Analysis Logic

Question No: 12

The Quad Multiplexer has _____ outputs

► 4

► 8

► 12

► **16**

Question No: 13

A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law

► Distributive Law

► Commutative Law

► **Associative Law**

Question No: 14

2's complement of any binary number can be calculated by

► adding 1's complement twice

► **adding 1 to 1's complement**

► subtracting 1 from 1's complement.

► calculating 1's complement and inverting Most significant bit

Question No: 15

The binary value "1010110" is equivalent to decimal _____

► **86**

► 87

► 88
► 89

Question No: 16

Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► **XOR**

==========>

MCQz (Set-8)

Question No: 2 one

The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► **8-bit**
► 16-bit

Question No: 3 one

The AND Gate performs a logical _____function

► Addition
► Subtraction
► **Multiplication**
► Division

Question No: 4 one

NOR gate is formed by connecting _____

► **OR Gate and then NOT Gate**
► **NOT Gate and then OR Gate**
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 5 one

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► **TTL**
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Question No: 6 one

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► **True**
► False

Question No: 7 one

When the control line in tri-state buffer is high the buffer operates like a _____ gate

► AND
► OR
► NOT
► **XOR**

Question No: 8 one

The GAL22V10 has ____ inputs

► 22
► **10**
► 44
► 20

Question No: 9 one

The ABEL symbol for “OR” operation is

► !
► **&**
► #
► $

Question No: 10one

The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► Similar
► Different
► **Similar with some enhancements**
► Depends on the type of PALs input size

Question No: 11one

All the ABEL equations must end with _____

► “ . “ (a dot)
► “ $ “ (a dollar symbol)
► **“ ; “ (a semicolon)**
► “ endl “ (keyword “endl”)

Question No: 12one

The Quad Multiplexer has _____ outputs

► 4
► 8
► 12
► **16 pg # 217 Quad Multiplexer has 16 inputs, 4 inputs for each Multiplexer.**

Question No: 13one

"Sum-of-Weights" method is used _____

► **to convert from one number system to other**
► to encode data
► to decode data
► to convert from serial to parralel data

Question No: 14one

Circuits having a bubble at their outputs are considered to have an active-low output.

► **True pg 128**
► False

Question No: 15one

(A + B)(A + B + C)(A + C) is an example of _____

► **Product of sum form**
► Sum of product form
► Demorgans law
► Associative law

Question No: 16one

Which one is true:

► **Power consumption of TTL is higher than of CMOS**
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption

► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

==========>

MCQz (Set-9)

Question No: 1 Please choose one
In the binary number "10011" the weight of the most significant digit is ____
► 2 4 (2 raise to power 4)
► 2 3 (2 raise to power 3)
► 2 0 (2 raise to power 0)
► 2 1 (2 raise to power 1)

Question No: 2 Please choose one
An S-R latch can be implemented by using _____ gates
► AND, OR
► NAND, NOR
► NAND, XOR
► NOT, XOR

Question No: 3 Please choose one
A latch has _____ stable states
► One
► Two pg 218
► Three
► Four

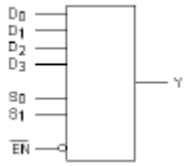
Question No: 4 Please choose one
Sequential circuits have storage elements
► True pg 305 A general Sequential circuit consists of a combinational circuit and a memory circuit (flip-flop).
► False

Question No: 5 Please choose one
The ABEL symbol for "XOR" operation is
► $
► #
► !
► &

Question No: 6 Please choose one
A Demultiplexer is not available commercially.
► True
► False

Question No: 7 Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer
► A parallel to serial converter circuit
► A counter circuit pg 244
► A BCD to Decimal decoder
► A 2-to-8 bit decoder

Question No: 8 Please choose one
The device shown here is most likely a



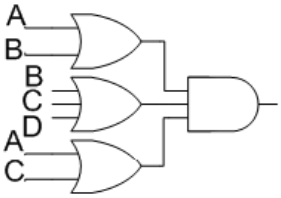
► Comparator
► **Multiplexer**
► Demultiplexer
► Parity generator

Question No: 9 Please choose one
The main use of the Multiplexer is to
► **Select data from multiple sources and to route it to a single Destination**
► Select data from Single source and to route it to a multiple Destinations
► Select data from Single source and to route to single destination
► Select data from multiple sources and to route to multiple destinations

Question No: 11 Please choose one
The binary value of 1010 is converted to the product term
► True
► **False**

Question No: 14 Please choose one
The output of the expression F=A+B+C will be Logic_____ when A=0, B=1, C=1. the symbol'+' here
represents OR Gate.
► Undefined
► **One**
► Zero
► 10 (binary)

Question No: 16 Please choose one
The diagram given below represents _____



► Demorgans law
► Associative law
► **Product of sum form**
► Sum of product form

==========>

MCQz (Set-11)

Question No: 1 (Marks: 1) - Please choose one
GAL can be reprogrammed because instead of fuses _____ logic is used in it
► **E²CMOS page191**
► TTL
► CMOS+
► None of the given options

Question No: 3 (Marks: 1) - Please choose one
If "1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

- ▶ 2^{nd}
- ▶ 4^{th}
- ▶ 14^{th}
- ▶ **No output wire will be activated**

Question No: 4 (Marks: 1) - Please choose one
Half-Adder Logic circuit contains 2 XOR Gates

- ▶ True
- ▶ **False**

Question No: 5 (Marks: 1) - Please choose one
A particular Full Adder has

- ▶ **3 inputs and 2 outputs**
- ▶ 3 inputs and 3 output
- ▶ 2 inputs and 3 output
- ▶ 2 inputs and 2 output

Question No: 6 (Marks: 1) - Please choose one
$Sum = A \oplus B \oplus C$
$CarryOut = C(A \oplus B) + AB$
are the Sum and CarryOut expression of

- ▶ Half Adder
- ▶ **Full Adder**
- ▶ 3-bit parralel adder
- ▶ MSI adder cicuit

Question No: 7 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

- ▶ **True**
- ▶ False

Question No: 11 (Marks: 1) - Please choose one
The decimal "8" is represented as _____ using Gray-Code.

- ▶ 0011
- ▶ **1100**
- ▶ 1000
- ▶ 1010

Question No: 12 (Marks: 1) - Please choose one
(A+B).(A+C) = _____

- ▶ B+C
- ▶ **A+BC**

► AB+C
► AC+B

Question No: 13 (Marks: 1) - Please choose one
A.(B + C) = A.B + A.C is the expression of _____

► Demorgan's Law
► Commutative Law
► **Distributive Law**
► Associative Law

Question No: 14 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**
► TRUE

Question No: 16 (Marks: 1) - Please choose one
Caveman number system is Base _5_____ number system

► 2
► **5**
► 10
► 16

==========>

MCQz (Set-12)

Question No: 2 (Marks: 1) - Please choose one
An S-R latch can be implemented by using _____ gates

► AND, OR
► **NAND, NOR**
► NAND, XOR
► NOT, XOR

Question No: 3 (Marks: 1) - Please choose one
A latch has _____ stable states

► One
► **Two**
► Three
► Four

Question No: 4 (Marks: 1) - Please choose one
Sequential circuits have storage elements

► **True**
► False

Question No: 6 (Marks: 1) - Please choose one
A Demultiplexer is not available commercially.
- ► **True**
- ► False

Question No: 7 (Marks: 1) - Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer
- ► A parallel to serial converter circuit
- ► **A counter circuit flip flop**
- ► A BCD to Decimal decoder
- ► A 2-to-8 bit decoder

Question No: 13 (Marks: 1) - Please choose one
Following is standard POS expression
$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$
- ► **True**
- ► False

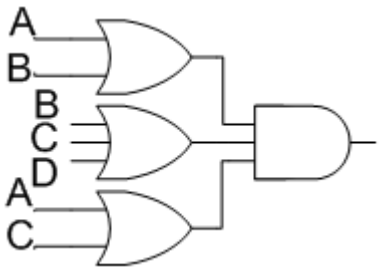
Question No: 14 (Marks: 1) - Please choose one
The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

- ► Undefined
- ► **One**
- ► Zero
- ► 10 (binary)

Question No: 15 (Marks: 1) - Please choose one
The ASCII Code (American Standard Code for Information Interchange) is a _____ code

- ► 2-bit
- ► **7-bit**
- ► 8-bit
- ► 16-bit

Question No: 16 (Marks: 1) - Please choose one
The diagram given below represents _____



- ► Demorgans law

- Associative law
- **Product of sum form**
- Sum of product form

==========>

MCQz (Set-13)

Question No: 1 (Marks: 1) - Please choose one
According to Demorgan's theorem:

$\overline{A+B+C}$ = _____

- A.B.C
- $A+\overline{B.C}$
- $\overline{A}.\overline{B}.\overline{C}$
- $\overline{A.B}+C$

Question No: 3 (Marks: 1) - Please choose one
The AND Gate performs a logical _____function

- Addition
- Subtraction
- **Multiplication**
- Division

Question No: 4 (Marks: 1) - Please choose one
NOR gate is formed by connecting _____

- **OR Gate and then NOT Gate**
- NOT Gate and then OR Gate
- AND Gate and then OR Gate
- OR Gate and then AND Gate

Question No: 5 (Marks: 1) - Please choose one
Generally, the Power dissipation of _____ devices remains constant throughout their operation.

- **TTL**
- CMOS 3.5 series
- CMOS 5 Series
- Power dissipation of all circuits increases with time.

Question No: 7 (Marks: 1) - Please choose one
When the control line in tri-state buffer is high the buffer operates like a _____ gate

- AND

► OR
► NOT
► **XOR**

Question No: 8 (Marks: 1) - Please choose one
The GAL22V10 has ____ inputs

► **22**
► 10
► 44
► 20

Question No: 10 (Marks: 1) - Please choose one
The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10
► **Similar**
► Different
► Similar with some enhancements
► Depends on the type of PALs input size

Question No: 11 (Marks: 1) - Please choose one
All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► **" ; " (a semicolon)**
► " endl " (keyword "endl")
==========>

MCQz (Set-14)

Question No: 7 Please choose one
The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?
► **A > B = 1, A < B = 0, A < B = 1**
► A > B = 0, A < B = 1, A = B = 0
► A > B = 1, A < B = 0, A = B = 0
► A > B = 0, A < B = 1, A = B = 1

Question No: 8 Please choose one
A particular Full Adder has
► **3 inputs and 2 output**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 9 Please choose one
The function to be performed by the processor is selected by set of inputs known as _____
► **Function Select Inputs**
► MicroOperation selectors

► OPCODE Selectors
► None of given option

Question No: 10 Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?
► **2**
► 1
► 3
► 4

Question No: 11 Please choose one
GAL is an acronym for _____.
► Giant Array Logic
► General Array Logic
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 Please choose one
The Quad Multiplexer has _____ outputs
► 4
► 8
► 12
► **16**

Question No: 13 Please choose one
A.(B.C) = (A.B).C is an expression of _____
► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law**

Question No: 14 Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement**
► subtracting 1 from 1's complement.
► calculating 1's complement and inverting Most significant bit

Question No: 16 Please choose one
Tri-State Buffer is basically a/an _____ gate.
► AND
► OR
► NOT
► **XOR**

==========>

MCQz (Set-15)

Question No: 1 Please choose one
Which of the number is not a representative of hexadecimal system
► 1234
► ABCD
► 1001
► **DEFH hexa does not have H as remainder**

Question No: 2 Please choose one
The Unsigned Binary representation can only represent positive binary numbers

► True
► False

Question No: 3 Please choose one

The values that exceed the specified range can not be correctly represented and are considered as_____

► **Overflow**
► Carry
► Parity
► Sign value

Question No: 4 Please choose one

The 4-bit 2's complement representation of "-7" is _____

► 0111
► 1111
► 1001
► 0110

Question No: 7 Please choose one

The output of an AND gate is one when _____

► **All of the inputs are one**
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Question No: 8 Please choose one

The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► 16

Question No: 9 Please choose one

A BCD to 7-Segment decoder has

► 3 inputs and 7 outputs
► **4 inputs and 7 outputs pg 103**
► 7 inputs and 3 outputs
► 7 inputs and 4 outputs

Question No: 10 Please choose one

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.

► 4-input, 8-bit
► 4-input, 16-bit
► 2-input, 8-bit
► 2-input, 4-bit

Question No: 11 Please choose one

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

► **AND pg 182**
► OR
► NOT
► XOR

Question No: 12 Please choose one

In ABEL the variable 'A' is treated separately from variable 'a'

► **True**

► False

Question No: 14 Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► **SET**

► RESET

► Clear

► Invalid

Question No: 15 Please choose one

Demultiplexer has

► Single input and single outputs.

► Multiple inputs and multiple outputs.

► **Single input and multiple outputs.**

► Multiple inputs and single output.

==========>

MCQz (Set-16)

Question No: 1 Please choose one

A SOP expression is equal to 1 _____

► All the variables in domain of expression are present

► At least one variable in domain of expression is present.

► When one or more product terms in the expression are equal to 0.

► **When one or more product terms in the expression are equal to 1.**

Question No: 4 Please choose one

High level Noise Margins (VNH) of CMOS 5 volt series circuits is _____

► 0.3 V

► 0.5 V

► **0.9 V**

► 3.3 V

Question No: 5 Please choose one

If we multiply "723" and "34" by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____

► 24.582

► 2.4582

► 24582

► 0.24582

Question No: 10 Please choose one

The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder

► 4-to-16 encoder

► BCD-to-Decimal

► **Decimal-to-BCD Priority**

Question No: 11 Please choose one

How many data select lines are required for selecting eight inputs?

► 1
► 2
► 3
► 4

Question No: 12 Please choose one

the diagram above shows the general implementation of _____ form

► boolean
► arbitrary
► POS
► SOP

Question No: 13 Please choose one

The Quad Multiplexer has _____ outputs

► 4
► 8
► 12
► 16

Question No: 14 Please choose one

Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► **Single input and multiple outputs.**
► Multiple inputs and single output.

Question No: 15 Please choose one

The expression _____ is an example of Commutative Law for Multiplication.

► AB+C = A+BC
► A(B+C) = B(A+C)
► AB=BA
► A+B=B+A

==========>

MCQz (Set-17)

Question No: 3 Please choose one

If "1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

► 2nd
► 4th
► 14th
► **No output wire will be activated**

Question No: 4 Please choose one

Half-Adder Logic circuit contains 2 XOR Gates

► True
► **False**

Question No: 5 Please choose one

A particular Full Adder has

► **3 inputs and 2 output**
► 3 inputs and 3 output
► 2 inputs and 3 output

► 2 inputs and 2 output

Question No: 6 Please choose one

Sum □ A □B □C

CarryOut □ C(A □B) □ AB

are the Sum and CarryOut expression of

► Half Adder

► **Full Adder**

► 3-bit parralel adder

► MSI adder cicuit

Question No: 7 Please choose one

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True**

► False

Question No: 13 Please choose one

A.(B + C) = A.B + A.C is the expression of _____

► Demorgan's Law

► Commutative Law

► **Distributive Law**

► Associative Law

Question No: 14 Please choose one

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**

► TRUE

==========>

MCQz (Set18)

Question No: 10 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

► Two AND gates, two OR gates, two inverters

► Three AND gates, two OR gates, one inverter

► **Two AND gates, one OR gate, two inverters**

► Two AND gates, one OR gate

Question No: 13 (Marks: 1) - Please choose one

Following is standard POS expression

$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$

► **True**

► False

==========>

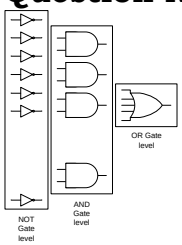
MCQz (Set-19)

Question No: 1 (Marks: 1) - Please choose one

A SOP expression is equal to 1 _____

► All the variables in domain of expression are present
► At least one variable in domain of expression is present.
► When one or more product terms in the expression are equal to 0.
► **When one or more product terms in the expression are equal to 1.**

Question No: 2 (Marks: 1) - Please choose one
The output A < B is set to 1 when the input combinations is _____
► A=10, B=01
► A=11, B=01
► A=01, B=01
► A=01, B=10

Question No: 12 (Marks: 1) - Please choose one


the diagram above shows the general implementation of _____ form
► boolean
► arbitrary
► POS
► SOP

Question No: 13 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► 4
► 8
► 12
► **16**

Question No: 14 (Marks: 1) - Please choose one
Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► **Single input and multiple outputs. Pag 178**
► Multiple inputs and single output.

Question No: 15 (Marks: 1) - Please choose one
The expression _____ is an example of Commutative Law for Multiplication.

► AB+C = A+BC
► A(B+C) = B(A+C)
► AB=BA
► A+B=B+A

==========>

MCQz (Set-20)

Question No: 1 (Marks: 1) - Please choose one
GAL can be reprogrammed because instead of fuses _____ logic is used in it

- ► **E^2CMOS**
- ► TTL
- ► CMOS+
- ► None of the given options

Question No: 3 (Marks: 1) - Please choose one
If "1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

- ► 2^{nd}
- ► 4^{th}
- ► 14^{th}
- ► **No output wire will be activated**

Question No: 4 (Marks: 1) - Please choose one
Half-Adder Logic circuit contains 2 XOR Gates

- ► True
- ► **False**

Question No: 5 (Marks: 1) - Please choose one
A particular Full Adder has

- ► **3 inputs and 2 output**
- ► 3 inputs and 3 output
- ► 2 inputs and 3 output
- ► 2 inputs and 2 output

Question No: 6 (Marks: 1) - Please choose one
$Sum = A \oplus B \oplus C$
$CarryOut = C(A \oplus B) + AB$
are the Sum and CarryOut expression of

- ► Half Adder
- ► **Full Adder**
- ► 3-bit parralel adder
- ► MSI adder cicuit

==========>

MCQz (Set-21)

Question No: 1 (Marks: 1) - Please choose one

Question No: 4 (Marks: 1) - Please choose one

NOR gate is formed by connecting _____

- ▶ OR Gate and then NOT Gate
- ▶ NOT Gate and then OR Gate
- ▶ AND Gate and then OR Gate
- ▶ OR Gate and then AND Gate

==========>

MCQz (Set-22)

Question No: 5 (Marks: 1) - Please choose one

A non-standard POS is converted into a standard POS by using the rule _____

- ▶ $A+\overline{A}=1$
- ▶ $A\overline{A}=0$
- ▶ $1+A=1$
- ▶ A+B = B+A

Question No: 6 (Marks: 1) - Please choose one

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

- ▶ 4
- ▶ **8**
- ▶ 12
- ▶ 16

Question No: 7 (Marks: 1) - Please choose one

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

- ▶ **A > B = 1, A < B = 0, A < B = 1**
- ▶ A > B = 0, A < B = 1, A = B = 0
- ▶ A > B = 1, A < B = 0, A = B = 0
- ▶ A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one

A particular Full Adder has

- ▶ **3 inputs and 2 output**
- ▶ 3 inputs and 3 output
- ▶ 2 inputs and 3 output
- ▶ 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one
The function to be performed by the processor is selected by set of inputs known as _____

► **Function Select Inputs**
► MicroOperation selectors
► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2**
► 1
► 3

► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► 4
► 8
► 12
► **16**

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law**

Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement**

- ► subtracting 1 from 1's complement.
- ► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one
The binary value "1010110" is equivalent to decimal _____

- **► 86**
- ► 87
- ► 88
- ► 89

Question No: 16 (Marks: 1) - Please choose one
Tri-State Buffer is basically a/an _____ gate.

- ► AND
- ► OR
- ► NOT
- **► XOR**

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MCQz (Set-23)

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