[1] COMPOSED BY SADIA ALI SADIIII☺

MIDTERM EXAMINATION
Spring 2009
CS302- Digital Logic Design (Session - 1)

Question No: 1 (Marks: 1) - Please choose one

In the binary number "10011" the weight of the most significant digit is ____

► **2^4 (2 raise to power 4)**
► 2^3 (2 raise to power 3)
► 2^0 (2 raise to power 0)
► 2^1 (2 raise to power 1)

Question No: 2 (Marks: 1) - Please choose one

An S-R latch can be implemented by using _____ gates

► AND, OR
► **NAND, NOR**
► NAND, XOR
► NOT, XOR

Question No: 3 (Marks: 1) - Please choose one

A latch has _____ stable states

► One
► **Two**
► Three
► Four

Question No: 4 (Marks: 1) - Please choose one

Sequential circuits have storage elements

► **True**
► False

Question No: 5 (Marks: 1) - Please choose one

The ABEL symbol for "XOR" operation is

► **$**
► #

► !
► &

Question No: 6 (Marks: 1) - Please choose one

A Demultiplexer is not available commercially.

► **True**
► False

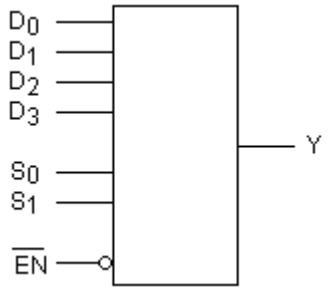
Question No: 7 (Marks: 1) - Please choose one

Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

► A parallel to serial converter circuit
► **A counter circuit**
► A BCD to Decimal decoder
► A 2-to-8 bit decoder

Question No: 8 (Marks: 1) - Please choose one

The device shown here is most likely a



► Comparator
► **Multiplexer**
► Demultiplexer
► Parity generator

Question No: 9 (Marks: 1) - Please choose one

The main use of the Multiplexer is to

► **Select data from multiple sources and to route it to a single Destination**
► Select data from Single source and to route it to a multiple

COMPOSED BY SADIA ALI SADIIII☺

Destinations

► Select data from Single source and to route to single destination

► Select data from multiple sources and to route to multiple destinations

Question No: 10 (Marks: 1) - Please choose one

A logic circuit with an output <PRIVATE "TYPE=PICT;ALT= mcq5_01700.gif"> $X = \overline{A}BC + A\overline{B}$ consists of _____.

► two AND gates, two OR gates, two inverters

► three AND gates, two OR gates, one inverter

► **two AND gates, one OR gate, two inverters**

► two AND gates, one OR gate

Question No: 11 (Marks: 1) - Please choose one

The binary value of 1010 is converted to the product term $\overline{A}B\overline{C}D$

► True

► **False**

Question No: 12 (Marks: 1) - Please choose one

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4

► **8**

► 12

► 16

Question No: 13 (Marks: 1) - Please choose one

Following is standard POS expression

$(A+\overline{B}+C+\overline{D})(A+\overline{B}+C+D)(A+B+\overline{C}+\overline{D})(A+B+C+\overline{D})(A+\overline{B}+\overline{C}+D)$

► **True**

► False

Question No: 14 (Marks: 1) - Please choose one

COMPOSED BY SADIA ALI SADIIII☺

The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol'+' here represents OR Gate.

- ► Undefined
- ► **One**
- ► Zero
- ► 10 (binary)

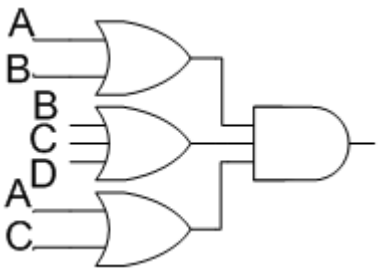
Question No: 15 (Marks: 1) - Please choose one

The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

- ► 2-bit
- ► **7-bit**
- ► 8-bit
- ► 16-bit

Question No: 16 (Marks: 1) - Please choose one

The diagram given below represents _____



- ► Demorgans law
- ► Associative law
- ► **Product of sum form**
- ► Sum of product form

Question No: 17 (Marks: 1)

How can a PLD be programmed?

PLDs are programmed with the help of computer which runs the programming software. The computer is connected to a programmer socket in which the PLD is inserted for programming. PLDs can also be programmed when they are installed on a circuit board

Question No: 18 (Marks: 1)

How many input and output bits do a Half-Adder contain?
The Half-Adder has a 2-bit input and a 2-bit output.

Question No: 19 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer 2-to-4 Binary Decoder?
The circuit of the 1-to-4 Demultiplexer is similar to the 2-to-4 Binary Decoder
described earlier figure 16.9. The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit figure

Question No: 20 (Marks: 3)

Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL.
Device declaration, pin declarations and set declarations.

Question No: 21 (Marks: 5)

Explain with example how noise affects Operation of a CMOS AND Gate circuit.
Two CMOS 5 volt series AND gates are connected together. Figure 7.3
The first AND gate has both its inputs connected to logic high, therefore the output of the gate is guaranteed to be logic high. The logic high voltage output of the first AND gate is assumed to be 4.6 volts well within the valid V_{OH} range of 5-4.4 volts. Assume the same noise signal (as described earlier) is added to the output signal of the first AND gate.

Question No: 22 (Marks: 10)

explain the SOP based implementation of the Adjacent 1s Detector Circuit

The Adjacent 1s Detector accepts 4-bit inputs. If two adjacent 1s are detected in the
input, the output is set to high. The operation of the Adjacent 1s Detector is represented by the
function table. Table 13.6. In the function table, for the input combinations 0011, 0110, 0111,
1011, 1100, 1101, 1110 and 1111 the output function is a 1.
Implementing the circuit directly from the function table based on the SOP form
requires 8 AND gates for the 8 product terms (minterms) with an 8-input OR gate. Figure 13.3.
The total gate count is

COMPOSED BY SADIA ALI SADIIII☺

One 8 input OR gate
Eight 4 input AND gates
Ten NOT gates
The expression can be simplified using a Karnaugh map, figure 13.4, and then the
simplified expression can be implemented to reduce the gate count. The simplified expression
isAB + CD +BC . The circuit implemented using the expression AB + CD +BC has reduced
to 3 input OR gate and 2 input AND gates.
The simplified Adjacent 1s Detector circuit uses only four gates reducing the cost, the
size of the circuit and the power requirement. The propagation delay of the circuit is of the order of two gates

MIDTERM EXAMINATION
Spring 2009
CS302- Digital Logic Design (Session - 1)

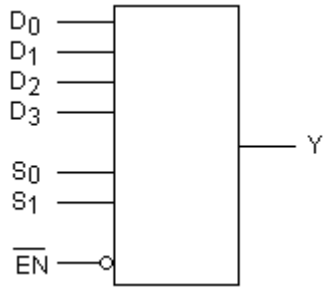
Question No: 1 (Marks: 1) - Please choose one

GAL can be reprogrammed because instead of fuses _____ logic is used in it

► **E²CMOS**
► TTL
► CMOS+
► None of the given options

Question No: 2 (Marks: 1) - Please choose one

The device shown here is most likely a



► Comparator

COMPOSED BY SADIA ALI SADIIII☺

► **Multiplexer**
► Demultiplexer
► Parity generator

Question No: 3 (Marks: 1) - Please choose one

If "1110" is applied at the input of BCD-to-Decimal decoder which output pin will be activated:

► 2nd
► 4th
► 14th
► **No output wire will be activated**

Question No: 4 (Marks: 1) - Please choose one

Half-Adder Logic circuit contains 2 XOR Gates

► True
► **False**

Question No: 5 (Marks: 1) - Please choose one

A particular Full Adder has

► **3 inputs and 2 output**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 6 (Marks: 1) - Please choose one

$Sum = A \oplus B \oplus C$
$CarryOut = C(A \oplus B) + AB$
are the Sum and CarryOut expression of

► Half Adder
► **Full Adder**
► 3-bit parralel adder
► MSI adder cicuit

Question No: 7 (Marks: 1) - Please choose one

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

► **True**
► False

COMPOSED BY SADIA ALI SADIIII☺

Question No: 8 (Marks: 1) - Please choose one

The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► **A=01, B=10**

Here output combination should A < B

Question No: 9 (Marks: 1) - Please choose one

The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► **16**

Question No: 10 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► **TTL**
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Question No: 11 (Marks: 1) - Please choose one

The decimal "8" is represented as _____ using Gray-Code.

► 0011
► **1100**
► 1000
► 1010

Question No: 12 (Marks: 1) - Please choose one

(A+B).(A+C) = _____

► B+C

COMPOSED BY SADIA ALI SADIIII☺

► **A+BC**
► AB+C
► AC+B

Question No: 13 (Marks: 1) - Please choose one

A.(B + C) = A.B + A.C is the expression of _____

► Demorgan's Law
► Commutative Law
► **Distributive Law**
► Associative Law

Question No: 14 (Marks: 1) - Please choose one

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

► **FALSE**
► TRUE

Question No: 15 (Marks: 1) - Please choose one

In ANSI/IEEE Standard 754 "Mantissa" is represented by ___32-bits_____ bits

► 8-bits
► 16-bits
► **32-bits**
► 64-bits

Question No: 16 (Marks: 1) - Please choose one

Caveman number system is Base _5_____ number system

► 2
► **5**
► 10
► 16

Question No: 17 (Marks: 1)

Briefly state the basic principle of **Repeated Multiplication-by-2** Method.

Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary.

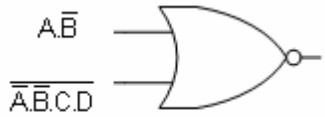
Question No: 18 (Marks: 1)

How standard Boolean expressions can be converted into truth table format.

Standard Boolean expressions can be converted into truth table format using

binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.

Question No: 19 (Marks: 2)



What will be the out put of the diagram given below
A.B + A.B.C.D

Question No: 20 (Marks: 3)

When an Input (source) file is created in ABEL a module is created which has three sections. Name These three sections.

Answer:

The three sections are:
Boolean Equations
Truth Tables
State Diagrams

Question No: 21 (Marks: 5)

Explain "AND" Gate and some of its uses

AND gates are used to combine multiple signals, if all the signals are TRUE then the output will also be TRUE. If any of the signals are FALSE, then the output will be false. ANDs aren't used as much as NAND gates; NAND gates use less components and have the advantage that they be used as an inverter.

Question No: 22 (Marks: 10)

Write down different situations where we need the sequential circuits.
Digital circuits that use memory elements for their operation are known as Sequential circuits. Thus Sequential circuits are implemented by combining combinational circuits with memory elements.

MIDTERM EXAMINATION
Fall 2009
CS302- Digital Logic Design (Session - 2)
Time: 60 min

11 COMPOSED BY SADIA ALI SADIIII☺

Marks: 38

Student Info	
StudentID:	_
Center:	**OPKST**
ExamDate:	**12/7/2009 12:00:00 AM**

For Teacher's Use Only									
Q No.	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**Total**
Marks									
Q No.	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	
Marks									
Q No.	**17**	**18**	**19**	**20**	**21**	**22**	-	-	
Marks									

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 1 (Marks: 1) - Please choose one

Which of the number is not a representative of hexadecimal system

► 1234
► ABCD
► 1001
► DEFH

Question No: 2 (Marks: 1) - Please choose one

The Unsigned Binary representation can only represent positive binary numbers

► True
► False

Question No: 3 (Marks: 1) - Please choose one

The values that exceed the specified range can not be correctly represented and are considered as _____

► Overflow
► Carry
► Parity
► Sign value

Question No: 4 (Marks: 1) - Please choose one

The 4-bit 2's complement representation of "-7" is _____

► 0111
► 1111
► 1001
► 0110

L-2

Question No: 5 (Marks: 1) - Please choose one

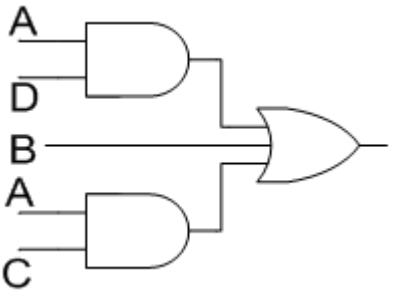
$\overline{A}B + \overline{A}B\overline{C} + AC$ is an example of _____

► Product of sum form
► Sum of product form
► Demorgans law
► Associative law

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 6 (Marks: 1) - Please choose one

The diagram given below represents



► Demorgans law
► Associative law
► Product of sum form
► Sum of product form

Question No: 7 (Marks: 1) - Please choose one

The output of an AND gate is one when _____

► All of the inputs are one
► Any of the input is one
► Any of the input is zero
► All the inputs are zero

Question No: 8 (Marks: 1) - Please choose one

The 4-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► 8
► 12
► 16

Question No: 9 (Marks: 1) - Please choose one

A BCD to 7-Segment decoder has

► 3 inputs and 7 outputs
► 4 inputs and 7 outputs
► 7 inputs and 3 outputs
► 7 inputs and 4 outputs

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 10 (Marks: 1) - Please choose one

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.

► 4-input, 8-bit
► 4-input, 16-bit
► 2-input, 8-bit
► 2-input, 4-bit

Question No: 11 (Marks: 1) - Please choose one

The PROM
consists of a fixed non-programmable _____ Gate array configured as a decoder.

► AND
► OR
► NOT
► XOR

Question No: 12 (Marks: 1) - Please choose one

In ABEL the variable 'A' is treated separately from variable 'a'

► True
► False

Question No: 13 (Marks: 1) - Please choose one

The ABEL notation equivalent to Boolean expression A+B is:

► A & B
► A ! B
► A # B
► A $ B

L-21

Question No: 14 (Marks: 1) - Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► SET
► RESET
► Clear
► Invalid

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 15 (Marks: 1) - Please choose one

Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► Single input and multiple outputs.
► Multiple inputs and single output.

Question No: 16 (Marks: 1) - Please choose one

Which one is true:

► Power consumption of TTL is higher than of CMOS
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption
► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

Question No: 17 (Marks: 1)

Briefly state the basic principle of **Repeated Division-by-2** method.

Repeated Division-by-2

Repeated Division-by-2 method allows decimal numbers of any magnitude to be converted into binary. In this method the Decimal number to be converted into its Binary equivalent is repeatedly divided by 2. The divisor is selected as 2 because the decimal number is being converted into Binary a Base-2 Number system. Repeated division method can be used to convert decimal number into any Number system by repeated division by the Base-Number. For example, the decimal number can be converted into the Caveman Number system by repeatedly dividing by 5, the Base number of the Caveman Number System. The Repeated Division method will be used in latter lectures to convert decimal into Hexadecimal and Octal Number Systems.
In the Repeated-Division method the Decimal number to be converted is divided

by the Base Number, in this particular case 2. A quotient value and a remainder value is
generated, both values are noted done. The remainder value in all subsequent divisions
would be either a 0 or a 1. The quotient value obtained as a result of division by 2 is
divided again by 2. The new quotient and remainder values are again noted down. In each
step of the repeated division method the remainder values are noted down and the
quotient values are repeatedly divided by the base number. The process of repeated
division stops when the quotient value becomes zero. The remainders that have been
noted in consecutive steps are written out to indicate the Binary equivalent of the Original
Decimal Number.

Question No: 18 (Marks: 1)

Briefly state the basic principle of **Repeated Multiplication-by-2** Method.

Repeated Multiplication-by-2 Method

An alternate to the Sum-of-Weights method used to convert Decimal fractions to
equivalent Binary fractions is the repeated multiplication by 2 method. In this method the
number to be converted is repeatedly multiplied by the Base Number to which the
number is being converted to, in this case 2. A new number having an Integer part and a
Fraction part is generated after each multiplication. The Integer part is noted down and
the fraction part is again multiplied with the Base number 2. The process is repeated until
the fraction term becomes equal to zero.
Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be
easily converted into binary. The conversion of Decimal fraction 0.625 into Binary
equivalent using the Repeated Multiplication-by-2 method is illustrated in a tabular form.
Table 2.4. Reading the Integer column from bottom to top and placing a decimal point in

the left most position gives 0.101 the binary equivalent of decimal fraction 0.625

Question No: 19 (Marks: 2)

Draw the circuit diagram of a Tri-State buffer.

Question No: 20 (Marks: 3)

Add -13 and +7 by converting them in binary system your result must be in binary.

Question No: 21 (Marks: 5)

Explain “Sum of Weights” method with example for “Octal to Decimal” conversion

1. Sum-of-Weights Method

Sum-of-weights as the name indicates sums the weights of the Binary Digits (bits)
of a Binary Number which is to be represented in Decimal. The Sum-of-Weights method
can be used to convert a Binary number of any magnitude to its equivalent Decimal
representation.
In the Sum-of-Weights method an extended expression is written in terms of the
Binary Base Number 2 and the weights of the Binary number to be converted. The
weights correspond to each of the binary bits which are multiplied by the corresponding
binary value. Binary bits having the value 0 do not contribute any value towards the final
sum expression.
The Binary number 10110_2 is therefore written in the form of an expression
having weights $2^0, 2^1, 2^2, 2^3$ AND 2^4 corresponding to the bits 0, 1, 1, 0 and 1 respectively.
Weights 2^0 AND 2^3 do not contribute in the final sum as the binary bits corresponding to
these weights have the value 0.

$10110_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$
$= 16 + 0 + 4 + 2 + 0$
$= 22$

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 22 (Marks: 10)

Explain the Implementation of an Odd-Parity Generator Circuit i.e by drawing function table, maping it to K-map and then simplifying the expression.

MIDTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design

Time: 60 min
Marks: 38

Question No: 1 (Marks: 1) - Please choose one

A SOP expression is equal to 1 _____

► All the variables in domain of expression are present
► At least one variable in domain of expression is present.
► When one or more product terms in the expression are equal to 0.
► When one or more product terms in the expression are equal to 1.

Question No: 2 (Marks: 1) - Please choose one

The output A < B is set to 1 when the input combinations is _____

► A=10, B=01
► A=11, B=01
► A=01, B=01
► A=01, B=10

Question No: 3 (Marks: 1) - Please choose one

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► True
► False

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 4 (Marks: 1) - Please choose one

High level Noise Margins (V_{NH}) of CMOS 5 volt series circuits is _____

► 0.3 V
► 0.5 V
► 0.9 V
► 3.3 V

Question No: 5 (Marks: 1) - Please choose one

If we multiply “723” and “34” by representing them in floating point notation i.e. by first, converting them in floating point representation and then multiplying them, the value of mantissa of result will be _____

► 24.582
► 2.4582
► 24582
► 0.24582

Question No: 6 (Marks: 1) - Please choose one

The output of the expression F=A+B+C will be Logic _____ when A=0, B=1, C=1. the symbol’+’ here represents OR Gate.

► Undefined
► One
► Zero
► 10 (binary)

Question No: 7 (Marks: 1) - Please choose one

If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.

► SET
► RESET
► Clear
► Invalid

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 8 (Marks: 1) - Please choose one

3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

► Low switching speeds, high power dissipation
► Fast switching speeds, high power dissipation
► Fast switching speeds, very low power dissipation
► Low switching speeds, very low power dissipation

Question No: 9 (Marks: 1) - Please choose one

The binary value “1010110” is equivalent to decimal _____

► 86
► 87
► 88
► 89

Question No: 10 (Marks: 1) - Please choose one

The _____ Encoder is used as a keypad encoder.

► 2-to-8 encoder
► 4-to-16 encoder
► BCD-to-Decimal
► Decimal-to-BCD Priority

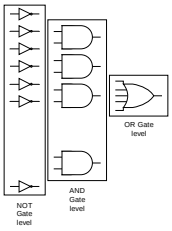
Question No: 11 (Marks: 1) - Please choose one

How many data select lines are required for selecting eight inputs?

► 1
► 2
► 3
► 4

Question No: 12 (Marks: 1) - Please choose one

 COMPOSED BY SADIA ALI SADIIII☺



the diagram above shows the general implementation of _____ form

► boolean
► arbitrary
► POS
► SOP

Question No: 13 (Marks: 1) - Please choose one

The Quad Multiplexer has _____ outputs

► 4
► 8
► 12
► 16

Question No: 14 (Marks: 1) - Please choose one

Demultiplexer has

► Single input and single outputs.
► Multiple inputs and multiple outputs.
► Single input and multiple outputs.
► Multiple inputs and single output.

Question No: 15 (Marks: 1) - Please choose one

The expression _____ is an example of Commutative Law for Multiplication.

► AB+C = A+BC
► A(B+C) = B(A+C)
► AB=BA
► A+B=B+A

Question No: 16 (Marks: 1) - Please choose one

"Sum-of-Weights" method is used _____

► to convert from one number system to other
► to encode data
► to decode data

 COMPOSED BY SADIA ALI SADIIII☺

► to convert from serial to parralel data

Question No: 17 (Marks: 2)

Why a 2-bit comparator is called parallel comparator?

Question No: 18 (Marks: 2)

Explain at least two advantages of the circuit having low power consumption

Question No: 19 (Marks: 2)

Name the four OLMC configurations

Question No: 20 (Marks: 3)

Explain "Test Vector" in context of ABEL

Question No: 21 (Marks: 3)

For a two bit comparator circuit specify the inputs for which the output A < B is set to 1

Question No: 22 (Marks: 5)

Explain Tri-State Buffers with the help of block diagram

Question No: 23 (Marks: 5)

Explain the Operation of Odd-Parity Generator Circuit with the help of timing diagram

MIDTERM EXAMINATION
Fall 2009
CS302- Digital Logic Design (Session - 5)

Ref No: 1022709
Time: 60 min
Marks: 38

Question No: 1 (Marks: 1) - Please choose one

According to Demorgan's theorem:

$\overline{A + B + C}$ = _____

► A.B.C

► $A + \overline{B.C}$

 COMPOSED BY SADIA ALI SADIIII☺

► $\overline{A}.\overline{B}.\overline{C}$

► $\overline{A.B} + C$

Question No: 2 (Marks: 1) - Please choose one

The Extended ASCII Code (American Standard Code for Information Interchange) is a _____ code

► 2-bit
► 7-bit
► 8-bit
► 16-bit

Question No: 3 (Marks: 1) - Please choose one

The AND Gate performs a logical _____function

► Addition
► Subtraction
► Multiplication
► Division

Question No: 4 (Marks: 1) - Please choose one

NOR gate is formed by connecting _____

► OR Gate and then NOT Gate
► NOT Gate and then OR Gate
► AND Gate and then OR Gate
► OR Gate and then AND Gate

Question No: 5 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

► TTL
► CMOS 3.5 series
► CMOS 5 Series
► Power dissipation of all circuits increases with time.

Question No: 6 (Marks: 1) - Please choose one

Two 2-bit comparator circuits can be connected to form single 4-bit comparator

► True
► False

Question No: 7 (Marks: 1) - Please choose one

When the control line in tri-state buffer is high the buffer operates like a _____ gate

► AND
► OR
► NOT
► XOR

Question No: 8 (Marks: 1) - Please choose one

The GAL22V10 has ____ inputs

► 22
► 10
► 44
► 20

Question No: 9 (Marks: 1) - Please choose one

The ABEL symbol for “OR” operation is

► !
► &
► #
► $

Question No: 10 (Marks: 1) - Please choose one

The OLMC of the GAL16V8 is _____ to the OLMC of the GAL22V10

► Similar
► Different
► Similar with some enhancements
► Depends on the type of PALs input size

Question No: 11 (Marks: 1) - Please choose one

All the ABEL equations must end with _____

► " . " (a dot)
► " $ " (a dollar symbol)
► " ; " (a semicolon)
► " endl " (keyword "endl")

Question No: 12 (Marks: 1) - Please choose one

The Quad Multiplexer has _____ outputs

► 4
► 8
► 12
► 16

Question No: 13 (Marks: 1) - Please choose one

"Sum-of-Weights" method is used _____

► to convert from one number system to other
► to encode data
► to decode data
► to convert from serial to parralel data

Question No: 14 (Marks: 1) - Please choose one

Circuits having a bubble at their outputs are considered to have an active-low output.

► True
► False

Question No: 15 (Marks: 1) - Please choose one

$(A+B)(A+\overline{B}+C)(\overline{A}+C)$ is an example of _____

► Product of sum form

► Sum of product form
► Demorgans law
► Associative law

Question No: 16 (Marks: 1) - Please choose one

Which one is true:

► Power consumption of TTL is higher than of CMOS
► Power consumption of CMOS is higher than of TTL
► Both TTL and CMOS have same power consumption
► Power consumption of both CMOS and TTL depends on no. of gates in the circuit.

Question No: 17 (Marks: 1)

Which device performs an operation which is the opposite of the Decoder function?

Ans:
Encoder function.

Question No: 18 (Marks: 1)

Name any two modes in which PALs are programmed.
Ans:

PAL devices are programmed by blowing the fuses permanently using over voltage.

Question No: 19 (Marks: 2)

Explain Combinational Function Devices?
Ans;
Xor,Xnor,NAND,NOR are combinational function devices.

Question No: 20 (Marks: 3)

Differentiate between hexadecimal and octal number system

octal - base 8
hexadecimal - base 16
Octal and hex are used to represent numbers instead of decimal because there is a very easy and direct way to convert from the "real" way that computers store numbers (binary) to something easier for humans to handle (fewer symbols). To translate a binary number to octal, simply group the binary digits three at a time and convert each group. For hex, group the binary digits four at a time.

Question No: 21 (Marks: 5)

Explain “Sum-of-Weights Method” for Hexadecimal to Decimal

27 COMPOSED BY SADIA ALI SADIIII☺

Conversion with at least one example ?

Ans:
The hexadecimal (Hex) numbering system provides even shorter notation than octal. Hexadecimal uses a base of 16. It employs 16 digits: number 0 through 9, and letters A through F, with A through F substituted for numbers 10 to 15, respectively,
Hexadecimal numbers can be expressed as their decimal equivalents by using the sum of weights method, as shown in the following example:

Weight 2 1 0
Hex. Number 1 B 7

$7 \times 16^0 = 7 \times 1$

$= 7$

$11 \times 16^1 = 11 \times 16$

$= 176$

$1 \times 16^2 = 1 \times 256$

$= 256$

Sum of products

439_{10}

Like octal numbers, hexadecimal numbers can easily be converted to binary or vise versa. Conversion is accomplished by writing the 4-bit binary equivalent of the hex digit for each position, as illustrated in the following example:

Hex. Number 1 B 7

0001 1011 0111 Binary number

Hexadecimal	Binary	Decimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7

8	1000	8
9	1001	9
A	1010	10
B	1011	11
C	1100	12
D	1101	13
E	1110	14
F	1111	15

Question No: 22 (Marks: 10)

Draw the function table of two-bit comparator circuit, map it to K-Map and derive the expression for (A > B)

Ans:

X_1	X_0	Y_1	Y_0	X<Y	X=Y	X>Y
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

.

0100090000037800000002001c0000000000040000000301080005000000b020000000005000
0000c023504080704000000 2e0118001c000000fb02100007000000000bc0200000000010202
2253797374656d000408070000c2010000985c110004ee8339681625050c020000040000002d0
1000004000000020101001c000000fb02ceff000000000009001000000000440001254696d657
3204e657720526f6d616e000000000000000000000000000000000040000002d010100050000
000902000000020d000000320a2c0000000100040000000000807330420cb1600040000002d0

 COMPOSED BY SADIA ALI SADIIII☺

The circuit has inputs X_1X_0 and Y_1Y_0 and outputs X > Y,

the expression for > is $X_1\overline{Y_1} + X_0\overline{Y_1}\,\overline{Y_0} + X_1X_0\overline{Y_0}$

time is out……

MIDTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design (Session - 6)

Ref No: 1351363
Time: 60 min
Marks: 38

COMPOSED BY SADIA ALI SADIIII☺

Question No: 1 (Marks: 1) - Please choose one

The maximum number that can be represented using unsigned octal system is _____

► 1
► **7**
► 9
► 16

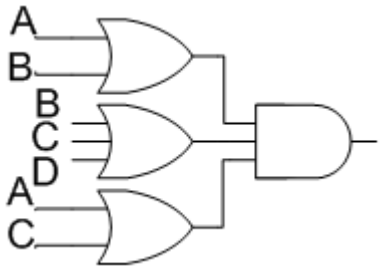
Question No: 2 (Marks: 1) - Please choose one

If we add “723” and “134” by representing them in floating point notation i.e. by first, converting them in floating point representation and then adding them, the value of exponent of result will be _____

► 0
► 1
► **2**
► 3

Question No: 3 (Marks: 1) - Please choose one

The diagram given below represents _____



► Demorgans law
► Associative law
► **Product of sum form**
► Sum of product form

Question No: 4 (Marks: 1) - Please choose one

The range of Excess-8 code is from _____ to _____

► **+7 to -8**
► +8 to -7
► +9 to -8
► -9 to +8

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 5 (Marks: 1) - Please choose one

A non-standard POS is converted into a standard POS by using the rule _____

► $A+\overline{A}=1$
► $A\overline{A}=0$
► $1+A=1$
► A+B = B+A

Question No: 6 (Marks: 1) - Please choose one

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

► 4
► **8**
► 12
► 16

Question No: 7 (Marks: 1) - Please choose one

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

► **A > B = 1, A < B = 0, A < B = 1**
► A > B = 0, A < B = 1, A = B = 0
► A > B = 1, A < B = 0, A = B = 0
► A > B = 0, A < B = 1, A = B = 1

Question No: 8 (Marks: 1) - Please choose one

A particular Full Adder has

► **3 inputs and 2 output**
► 3 inputs and 3 output
► 2 inputs and 3 output
► 2 inputs and 2 output

Question No: 9 (Marks: 1) - Please choose one

The function to be performed by the processor is selected by set of inputs known as _____

► **Function Select Inputs**
► MicroOperation selectors

► OPCODE Selectors
► None of given option

Question No: 10 (Marks: 1) - Please choose one
For a 3-to-8 decoder how many 2-to-4 decoders will be required?

► **2**
► 1
► 3
► 4

Question No: 11 (Marks: 1) - Please choose one
GAL is an acronym for _____.

► Giant Array Logic
► **General Array Logic**
► Generic Array Logic
► Generic Analysis Logic

Question No: 12 (Marks: 1) - Please choose one
The Quad Multiplexer has _____ outputs

► 4
► 8
► 12
► **16**

Question No: 13 (Marks: 1) - Please choose one
A.(B.C) = (A.B).C is an expression of _____

► Demorgan's Law
► Distributive Law
► Commutative Law
► **Associative Law**

Question No: 14 (Marks: 1) - Please choose one
2's complement of any binary number can be calculated by
► adding 1's complement twice
► **adding 1 to 1's complement**
► subtracting 1 from 1's complement.

► calculating 1's complement and inverting Most significant bit

Question No: 15 (Marks: 1) - Please choose one

The binary value “1010110” is equivalent to decimal _____

► **86**
► 87
► 88
► 89

Question No: 16 (Marks: 1) - Please choose one

Tri-State Buffer is basically a/an _____ gate.

► AND
► OR
► NOT
► **XOR**

Question No: 17 (Marks: 2)

For what values of A, B, C and D, value of the expression given below will be logic 1. Explain at least one combination.

$$\overline{A.\overline{B} + \overline{A}.\overline{B}.C.D}$$

Ans:

Question No: 18 (Marks: 2)

provide some of the inputs for which the adjacent 1s detector circuit have active high output?

Ans:
The Adjacent 1s Detector accepts 4-bit inputs.
If two adjacent 1s are detected in the input, the output is set to high.
input combinations will be

1. **0011,**

2. **0110,**
3. **0111,**
4. **1011,**
5. **1100,**
6. **1101,**
7. **1110 and**
8. **1111**

the output function is a 1.

Question No: 19 (Marks: 2)

Draw the Truth-Table of NOR based S-R Latch

S	R	Action
0	0	Keep state
0	1	Q=0
1	0	Q=1
1	1	Restricted combination

Question No: 20 (Marks: 3)

For a two bit comparator circuit specify the inputs for which A > B

Ans:

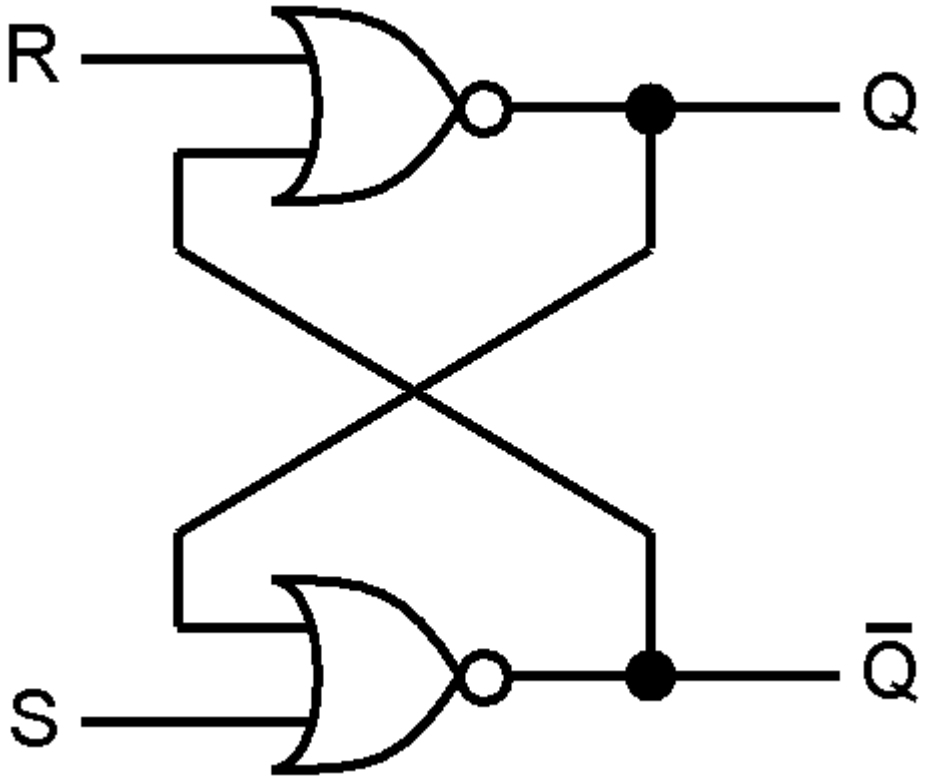
1. **01 00,**
2. **10 00,**
3. **10 01,**
4. **11 00,**
5. **11 01 and**
6. **11 10**

 COMPOSED BY SADIA ALI SADIIII☺

Question No: 21 (Marks: 3)

Draw the circuit diagram of NOR based S-R Latch ?

Ans:



 COMPOSED BY SADIA ALI SADIIII☺

Question No: 22 (Marks: 5)

One of the ABEL entry methods uses logic equations; explain it with at least a single example.

Ans:

In ABEL any letter or combination of letters and numbers can be used to identify variables.
ABEL however is case sensitive,
thus variable 'A' is treated separately from variable 'a'.

All ABEL equations must end with ';'

Boolean expression F = AB' + AC +(BD)' is written in ABEL as F = A & !B # A & C # !B & !D;

Question No: 23 (Marks: 5)

Explain Carry propagation in Parallel binary adder?

Ans:
Parralel binary adder:

A binary adder circuit is described using dynamic transistor logic in which for high speed carry propagation the adder stages are grouped in pairs or larger numbers and additional dynamic logic means is provided in each group to control a single transistor connected in series in the carry propagation path over the group.

The transistors used in the specific embodiments are MOS transistors, but some or all of these could be replaced by junction FET's or bipolar transistors.

was my CS302_DLD paper. Total 23 questions out of which 16

[37] COMPOSED BY SADIA ALI SADIIII☺

MCQ's.

2 questions of two marks each were from the topic Adder.
A boolian expression wes given and had to find a logic 1 for it.
One 5 marks question from parity method.

2day was my 2nd paper of cs302
this was my papers

SOP to POS conversion__3mark
S-R latch Diagram_____5mark
Nor gate table_____3mark
8 t0 3 bit encoder____5mark
Tri-stuff diagram_____3mark

mcqz zyda tar_start lec mn say aye thay
binary additin
2's complemnt
k-map

Assalam o Alaikum

Today I attempted CS302 paper

Paper was of 38 marks.
16 MCQs and 22 marks paper comprised of long questions.
2 marks question was "Write the uses of multiplexer".

2 marks question was "Write any two advantages of boolean expressions".

2 marks question was "Draw the diagram of odd parity generator circuit".

3 marks question was "What does a 8-bit adder/subtracter circuit do"?

 COMPOSED BY SADIA ALI SADIIII☺

3 marks question was "Draw the function table of 3 to 8 decoder".

5 marks question was "Describe 16 bit ALU".

5 marks question was "Describe in your own words about latches".