S501 MIDTERM PAPERS LATEST ALL IN ONE THREAD FALL 2011 MONTH OF MAY
PAPER#1

1. What is relation b/w data path and control unit in SRC processors…….2marks
2. Define Pre-fetching…….2marks
3. Write the structural RTL for " in ra, rb" …….3marks
4. What is difference between Latency and Throughput……3marks
5. Write the Structural RTL for "call ra, rb"…….5marks
6. What are the pipeline problems. Describe each briefly…. 5marks

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How can you define microprogram? (2 Marks)
A question about to define the shift right instruction? (2 Marks)
What is the utility of reset operation and when it is required? (3 Marks)
Structural RTL instructions definition? (3 Marks)
Write the Structural RTL description for un-conditional jump instruction for uni-bus data path implementation. (5 Marks)
Define two hazard in pipelining and how can to overcome these. (5 Marks)

Q no 1
Define Control unit. (2 marks)
Q no 2
How can you define Microprogram (2 marks)
Q no 3
Instruction fetch say tha yad nahin (3 marks)
rel Ra
Q no 4
what is the utility of reset operation when it is required (3 marks)

Q no5

what are the types of SRC?Name them? also explain its format? (5 marks)

Q no 6
yad nahin muggar uni- bus say related tha (5 marks)

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1. How many types of instructions are available in SRC? Name them. What is the format of each of these instructions…….5marks

2. Write the Structural RTL for the call instruction for uni-bus data path implementation.
call ra, rb……...5 marks

3. Write the Structural RTL for the mov instruction for uni-bus data path implementation.
mov ra, rb……...3 marks

4. How many stages are in the pipelined version of SRC? Name them……...3 marks

5. How can you define microprogram?.....2 marks

6. Write the Structural RTL for the 'not instruction'…….2 marks

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Question No: 19 (Marks: 2)
How can you define microprogram?

Question No: 20 (Marks: 3)
What is the role of timing step generator in a processor?
Question No: 21 (Marks: 3)
What is the utility of reset operation and when it is r
Question No: 22 (Marks: 5)
Write the Structural RTL description for un-conditional jump
uni-bus data path implementation.
jump [ra+c2]
Question No: 23 (Marks: 5)
What function is performed by the reset operation of a processor? What are the
two types of reset operations?
2nd paper
There were 23 questions 1-14 are mcqs others are questions
Q : DEFINE HARD RESET AND SOFT RESET OPERATIONS IN SRC
Q : Write two pipelining problem and define them briefly.
Q : What information is provided by the addressing modes of some processors?
Q : eLEBORATE PRE-FATCHING CONCEPT?
Q : Write RTL functions and there was a rb +rc instruction.
Q : how we speed-up a computer?
Q : Write execution time of an instruction(there was a description too)
Q : Types of instructions
Q : How you represent register data field?

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mid term fall 2011 on 29-11-11

1. Define pre-fetching. (02 marks)

2. Structural RTL was given and simple syntax was required. (02 marks) **ANSWER add ra, rb, rc**
3. Give strcuctrual RTL of in ra, c2. (03 marks)

4. How exceptions generated? Differentiate between internal and external exceptions. (03 marks)

5. Make structural RTL of shiftr ra, rb, c1 (05 marks)

6. What functions are performed by RESET? Diff b/w hard reset and soft reset. (05 marks)

Q1- What is Reset operation describe it types
Q2- Describe super scaler and VILW.
Q3- Write RTL functions and there was a rb +rc instruction
Q4- Write RTL functions and there was a rb +rc instruction
Q5-. Write the structural RTL for " in ra, rb"

Write the Structural RTL description for un-conditional jump instruction for
uni-bus data path implementation. (5 Marks)

My Papers on 27-11-2011.
Total 26 Questions of total 40 Marks.
20 MCQs
6 Short question
All MCQs were from this file compilation.
Control Unit Functionality mention only 3 , 3 Marks
RTL Notation.
Define Prefetching.
Jump ra+c2 in RTL notation , 5 Marks.
Describe to ways to increase the number instruction execution in a
given time .Ecplain one in detail. , 5 Mark

My paper on 29-11-2011

Total 26 Questions and 20 MCQs.

Define Pre-Fetching 2 Mks

Define NOP Instruction 2 MKs

Show the given register in RTL.. 4 question 2 Mks

Structural RTL for unibus In svc 3 Mks

Instruction Fetch using structural RTL

No of ways to increase no of instruction execution in given time

Objective was complete from old papers

Wish you good luck

Midterm paper of CS501_Advance Computer Architecture
Campus: VKHI02
Date: 28 November, 2011

1. What function is performed by the reset operation of a processor and differentiate Hard reset and Soft reset? [5 marks]

2. Write the Structural RTL for the mov instruction for uni-bus data path implementation.
mov ra, rb [3 marks]

3. Write the Structural RTL for shift right instruction. [Question was not exactly like that. Every thing was written[i mean structure was already written] we just have to arrange the sequences of the steps.][2 marks only :( ]

4. What is the use of "NOP" instruction in pipelining? [3 marks]

Ask As MCQs.

1). LPC: This control signal will enable write of the Program Counter, thus the new, incremented value can be written into the PC if it is made available on the “in” bus. Note that the ALSU is assumed to include an INC4 function.

2). Anything that interrupts the normal flow of execution of instructions in the processor is called an exception.

3).What is the size of the memory space that is available to FALCON-A processor?
Select correct option:
2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes

4). What is the working of Processor Status Word (PSW)?
Select correct option:

To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing
To hold the address of the next instruction in memory that is to be executed

5). What is the instruction length of the FALCON-E processor?
Select correct option:
8 bits
16 bits
32 bits
64 bits

6). Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:
Address
Instruction code
Opcode
Operand

7). Which instruction is used to store register to memory using relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction
I don't know its answer but they are from topic: SRC instruction format.

8). Which type of instructions help in changing the flow of the program as and when required?
Select correct option:
Arithmetic
Control
Data transfer
Floating point

9). A MCQ about Power PC

10). which one of the following is 0-address based machine.

11). There was a very long MCQ not remember now but the options are [this is so strange.]
VCON
FCON
ACON
LCON
I already found all of them keywords on handouts but there is nothing like this.

My today cs501 paper all msqs from past papers except 2 total 20 mcqs. and subjective is
Which register holds the instruction that is being executed? 2marks
Which technique is used for overlapping multiple instructions simultaneously?2 marks
Write the Structural RTL for the "mov" instruction i.e. mov ra, rb. 3marks
Write the Structural RTL for the "mov" instruction i.e. mov ra, rb. 3marks
Write the related timing steps requirements and data path implementations of Instruction Fetch procedure using structural RTL 5marks
How many types of exceptions can occur in a machine? Explain any two of them. 5marks

Full paper Moaz ke files mai se aya hai.....

20 mcq's thae r 6 Question thae

2 marks ke 2 Question

3 marks ke 2 Quuestion

5 mzrks ke bi 2 Question

compare bus width of FALCON-A and SRC

What do you know about Machine Exception?

What function is performed by the reset operation of a processor and differentiate Hard reset and Soft reset?

structural RTL out ra,c2 3marks

Consider the following sequence of the instructions giving through the pipelined version of SRC
200:shl r6,r3,5
204:str r7,30
208:sub r2,r4,r5
2012:add r1,r2,r3
216:id r7,48

.Write the structure RTL description for the uni-bus data path implementation Jump[ra+2] (5 Marks)

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Which register holds the instruction that is being executed? 2marks

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Write the Structural RTL for the "mov" instruction i.e. mov ra, rb. 3marks

Write the related timing steps requirements and data path implementations of Instruction Fetch procedure using structural RTL 5marks

How many types of exceptions can occur in a machine? Explain any two of them. 5marks

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timing step requirement and data path implementation of instruction fetch in structural RTL [5 MARKS]

Structural RTL for the out instruction out ra,c2. [3MARKS]

how many type of Exception ? define two. [5 MARKS]

(4)Arrange pipelining verification of SRC [3 MARKS]

ALU operation

Instruction fetch

Memory access

Register write

Define external and internal Exception. [2MARKS]

compare the uni bus implementation of FALCON-A with SRC with respect to number of registers. [2 MARKS]

MID-Term Exam FALL-2011 (30-11-11)

Total Question was 26;
MCQs was mostly from quizzed taken in session!
and from hazard there was 2-3 mcqs.
Like what are type of hazard, data, segment or branch ....

Unconditional Jump's STL representation! 5 Marks
MBA and MAR! 5 marks

Control Unit! 2 marks
STL representation of basic operations like ADD, SUB, NOT etc.! 3 marks

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CS501 Current Paper 27-11-2011

Total 26 Questions of total 40 Marks.
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6 Short question
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RTL Notation.
Define Prefetching.
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Describe to ways to increase the number instruction execution in a
given time .Ecplain one in detail. , 5 Mark

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1. What is relation b/w data path and control unit in SRC processors…….2marks

2. which processor uses super scaler? name two. .... 2 marks

3. Write the Structural RTL for the mov instruction for uni-bus data path implementation. Mov ra, c2……..3 mark

4. What are the three main functionalities of control unit? .... 3 marks

5. Write the Structural RTL description for un-conditional jump [ra + c2] instruction for uni-bus data path implementation. (5 Marks)

6. What are the pipeline problems? Describe each briefly…. 5mark

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CS501_Midterm_Nov, 2011
By Nadeempomy

Q 1

For any of the instructions that are a part of the instruction set of the SRC, there are cerain_____required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

- Register
- **Control signals**
- Memory
- None of the given

Q 2

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC _____wide.

- 8-bits
- 16-bits
- **32-bits**
- 64-bits

Q 3

What is the instruction longth of the FALCON-A processor?

- 8-bits
- **16-bits**
- 32-bits
- 64-bits

Q 4

_____control signals enable the input to the PC for receiving a value that is currently on the internal processor bus.

- **LPC**
- INC4
- LC
- I

Q 5

Which one of the following is a bi-stable device, capable of storing one bit of information?

- Decoder
- **Flip-Flop**
- Multiplexer
- Diplexer

Q 6

Which instruction is used to store register to memory using relative address?

- ld instruction
- ldr instruction
- lar instruction
- **str instruction**

Q 7

Which field of the machine language instruction is the “type of operation” that is to be performed?

- **Op-code (or the operation code)**
- CPU registers
- Momory cells
- I/O locations

Q 8

The instruction _____ will load the register R3 with the contenets of the m\emory location M [PC+56]

___Add R3, 56

___lar R3, 56

___ldr R3, 56
___str R3, 56

Q 9

_____ operation is required to change the processor's state to a known, defined value.

- Change
- **Reset**
- Update
- None of the given

Q 10

which type of instructions help in changing the flow of the program as and when required?

- Arithmetic
- **Control**
- Data transfer
- Floating point

Q 11

Which one of the following registers holds the address of the next instruction to be executed?

- Accumulator
- Address Mask
- Instruction Register
- Program Counter

Which one of the following is the memory organization of EAGLE processor?

- 8-bits
- **16-bits**
- 32-bit
- 64-bits

Q 12

The external interface of FALCON-A constists of a _____address bus and _____a data bus.

- 8-bit. 8-bit
- **16-bit. 16-bit**
- 16-bit. 24-bit

- 16-bit. 32-bit

Q 13

Type A of SRC has which of the following instructions? A) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction

- & (b)
- (b) & (c)
- & (e)
- **(b) & (e)**

Short Questions

Write the structural RTL for the call instruction for uni-bus path implementation

call ra, rb (5)

Write the structural RTL for call ret ra

Define pre-fetching (2)

Describe three main functions of control unit. (3)

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Midterm paper of CS501_Advance Computer Architecture

Campus: VKHI02

Date: 28 November, 2011

1. What function is performed by the reset operation of a processor and differentiate Hard reset and Soft reset? [5 marks]

2. Write the Structural RTL for the mov instruction for uni-bus data path implementation.

mov ra, rb [3 marks]

3. Write the Structural RTL for shift right instruction. [Question was not exactly like that. Every thing was written[i mean structure was already written] we just have to arrange the sequences of the steps.][2 marks only :( ]

4. What is the use of "NOP" instruction in pipelining? [3 marks]

Ask As MCQs.

1). LPC: This control signal will enable write of the Program Counter, thus the new,
incremented value can be written into the PC if it is made available on the “in”
bus. Note that the ALSU is assumed to include an INC4 function.

2). Anything that interrupts the normal flow of execution of instructions in the
processor is called an exception.

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Select correct option:

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4). What is the working of Processor Status Word (PSW)?

Select correct option:

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CS501 Current Paper 27-11-2011

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Define Prefetching.
Jump ra+c2 in RTL notation , 5 Marks.
Describe to ways to increase the number instruction execution in a given time .Ecplain one in detail. , 5 Mark

---

Q1- What is Reset operation describe it types
Q2- Describe super scaler and VILW.
Q3- Write RTL functions and there was a rb +rc instruction
Q4- Write RTL functions and there was a rb +rc instruction
Q5-. Write the structural RTL for " in ra, rb"

Write the Structural RTL description for un-conditional jump instruction for
uni-bus data path implementation. (5 Marks)

Total 26 Questions of total 40 Marks.
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Write the Structural RTL description for un-conditional jump instruction for
uni-bus data path implementation. (5 Marks)

What do you know about Machine Exception?

.Write the structure RTL description for the uni-bus data path implementation Jump[ra+2] (5 Marks)

Consider the following sequence of the instructions giving through the pipelined version of SRC
200:shl r6,r3,5
204:str r7,30
208:sub r2,r4,r5
2012:add r1,r2,r3
216:id r7,48

What function is performed by the reset operation of a processor and differentiate Hard reset and Soft reset?

structural RTL out ra,c2 3marks

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my paper

What is NOP instruction and its significance in pipelining? 3

Which register hold the instruction that is being executed? 2

Write the structural RTL for the mov immediate instruction for the mov immediate instruction for uni-bus data path implement Mov ra,c2 3 marks

structural RTL out ra c2 nu instruction? 5 marks

Which register hold the address of the next instruction to be executed in the processor?

What do you aboyt Machie Exception ?

My todays paper 10th december 2012

mcqs sary moaaz ki files mein se aye thy u guys just need to prepare from subjective and objective files of moaazz it is really good i just prepare from it and done 100 % paper

Q1. Which register holds the address of the next instruction to be executed in the processor? (2 Marks)
Answer:-
The program counter (PC) that holds the address of the next instruction in memory that is to be executed.

Write the main functions of the branch instruction
calculate the target address to evolutes the condition
3.Write the Structural RTL for the "mov" instruction i.e. mov ra, rb. 3marks
4.what is the utility of reset operation when it is required (3 marks)
Answer:- (Page 194)
Reset operation is required to change the processor's state to a known, defined value. The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

5. Write the Structural RTL description for un-conditional jump uni-bus data path implementation. jump [ra+c2]. 5 marks

6. solution of data dependencies briefly explain. 5 marks

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cs501:current Midterm paper

My paper was as follwes:

9-10 mcqs were from past papers remaining were new.

Q#1: comparison b/w FALCON-A and SRC w.r.t. registers. (2 marks)
Q#2: Define Exception. (2 marks)
Q#3:Write stuctural RTL for movi..... (3 marks)
Q#4: Write essential Reset operations..... (3 marks)
Q#5: Types of Exception.... (5 marks)
Q#6:Stuctural RTL description for shift.....(5 marks)

1.Insrtuction Fetch 2)
2.Arithmetic logic unit 2)
3.Memory access 3)
4.Pipeline Problems 3)

5.Related things steps requirements and data path implementation of IF procedure using RTL 5)

6.Role of step generator in a processor 5)

My 2day cs501 Midterm Paper
My Today cs501 Midterm Paper
20 Mcq's from lecture 20,21,22

Not from Previous Paper
Subjective
Q1:
structural RTL for mov ra, rb
Q2:
Which register holds the address of the next instruction to b executed in the processor?
Q3:
Write the structural RTL for the mov immediate instruction for the mov immediate instruction for uni-bus data path implementation Movi ra,c2
Q4:
Consider the following sequence of the instructions giving through the pipelined version of SRC
200:shl r6,r3,5

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216:id r7,48
Q5:
Write the structure RTL description for the uni-bus data path implementation Jump[ra+2]
Q6:
Write the Structural RTL for the 'not instruction

Today my paper

For any of the instructions that are a part of the instruction set of the SRC, there are certain_____required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

►Register

►**Control signals**
►Memory

►None of the given

What is the instruction length of the FALCON-A processor?

►8-bits

►**16-bits**
►32-bits

►64-bits

The instruction _____ will load the register R3 with the contenets of the m\emory location M [PC+56]

►Add R3, 56

►lar R3, 56

►**ldr R3, 56**
►str R3, 56

_____ operation is required to change the processor's state to a known, defined value.

►Change

►**Reset**
►Update

►None of the given

which type of instructions help in changing the flow of the program as and when required?

►Arithmetic

►**Control**
►Data transfer

►Floating point

The external interface of FALCON-A consists of a _____address bus and _____a data bus.

►8-bit. 8-bit

►**16-bit. 16-bit**
►16-bit. 24-bit

►16-bit. 32-bit

Which one of the following is the memory organization of **FALCON-E processor?**

- ► 2^8 * 8 bits
- ► **2^{16} * 8 bits**
- ► 2^{32} * 8 bits
- ► 2^{64} * 8 bits

"If P = 1, then load the contents of register R1 into register R2".
This statement can be written in RTL as:

- ► R1 ¬ R2
- ► P: R1 ¬ R2
- ► **P: R2 ¬ R1**
- ► P: R2 ¬ R1, P: R1 ¬ R2

There are _____ types of reset operations in SRC

- ► **Two**
- ► Three
- ► Four
- ► Five

_____ controller controls the sequence of the flow of microinstructions.

- ► Multiplexer
- ► **Microprogram**
- ► ALU
- ► None of the given

Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?

Select correct option:

- ►**:=**
- ►&
- ►%
- ►©

What functionality is performed by the instruction "str R8, 34" of SRC?

- ►It will load the register R8 with the contents of the memory location M [PC+34]
- ►It will load the register R8 with the relative address itself (PC+34).
- ►**It will store the register R8 contents to the memory location M [PC+34]**
- ►No operation

Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

►Instruction Register
►Memory address register
►Memory Buffer Register
►**Registers A and C**
subjective question

Write the structure RTL description for the uni-bus data path implementation Jump[ra+2]

Cs501 Current Midterm Papers:
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How many types of exceptions can occur in a machine? Explain any two of them. 5marks

Paper 2
Full paper Moaz ke files mai se aya hai.....
20 mcq's thae r 6 Question thae
2 marks ke 2 Question
3 marks ke 2 Quuestion
5 mzrks ke bi 2 Question
compare bus width of FALCON-A and SRC
What do you know about Machine Exception?
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216:id r7,48
.Write the structure RTL description for the uni-bus data path implementation Jump[ra+2] (5 Marks)

Paper 3
MY PAPER
(1)compare the uni bus implementation of FALCON-A with SRC with respect to number of registers. [2 MARKS]

(2) Define external and internal Exception. [2MARKS]

(3) Structural RTL for the out instruction out ra,c2. [3MARKS]

(4)Arrange pipelining verification of SRC [3 MARKS]
ALU operation
Instruction fetch
Memory access
Register write

(5) timing step requirement and data path implementation of instruction fetch in structural RTL [5 MARKS]

(6) how many type of Exception ? define two. [5 MARKS]

Paper 4
Which register store previous calculated value.
Differrence between latency and throughput.

Write two important features of reset operation.
write structural RLT for return instruction ret ra.
Difference between sigma = (a,b)

Paper 5
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Which technique is used for overlapping multiple instructions simultaneously?2 marks

Write the Structural RTL for the "mov" instruction i.e. mov ra, rb. 3marks

Write the related timing steps requirements and data path implementations of Instruction Fetch procedure using structural RTL 5marks

How many types of exceptions can occur in a machine? Explain any two of them. 5marks

Paper 6
timing step requirement and data path implementation of instruction fetch in structural RTL [5 MARKS]

Structural RTL for the out instruction out ra,c2. [3MARKS]

how many type of Exception ? define two. [5 MARKS]

(4)Arrange pipelining verification of SRC [3 MARKS]

ALU operation

Instruction fetch

Memory access

Register write

Define external and internal Exception. [2MARKS]

compare the uni bus implementation of FALCON-A with SRC with respect to number of registers. [2 MARKS]

Paper 7
What do you know about Machine Exception?

.Write the structure RTL description for the uni-bus data path implementation Jump[ra+2] (5 Marks)

Consider the following sequence of the instructions giving through the pipelined version of SRC
200:shl r6,r3,5
204:str r7,30
208:sub r2,r4,r5
2012:add r1,r2,r3
216:id r7,48

What function is performed by the reset operation of a processor and differentiate Hard reset and Soft reset?

structural RTL out ra,c2 3marks

Paper 8
my paper
What is NOP instruction and its significance in pipelining? 3
Which register hold the instruction that is being executed? 2
Write the structural RTL for the mov immediate instruction for the mov immediate instruction for uni-bus data path implement Mov ra,c2 3 marks
structural RTL out ra c2 nu instruction? 5 marks
Which register hold the address of the next instruction to be executed in the processor?
What do you aboyt Machie Exception ?

Paper 9
My paper was as follwes:

9-10 mcqs were from past papers remaining were new.

Q#1: comparison b/w FALCON-A and SRC w.r.t. registers. (2 marks)
Q#2: Define Exception. (2 marks)
Q#3:Write stuctural RTL for movi..... (3 marks)
Q#4: Write essential Reset operations..... (3 marks)
Q#5: Types of Exception.... (5 marks)
Q#6:Stuctural RTL description for shift.....(5 marks)

Paper 10
Q1. Which register holds the address of the next instruction to be executed in the processor? (2 Marks)
Answer:-
The program counter (PC) that holds the address of the next instruction in memory that is to be executed.
Write the main functions of the branch instruction
calculate the target address to evolutes the condition
3.Write the Structural RTL for the "mov" instruction i.e. mov ra, rb. 3marks
4.what is the utility of reset operation when it is required (3 marks)
Answer:- (Page 194)
Reset operation is required to change the processor's state to a known, defined value. The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.
5. Write the Structural RTL description for un-conditional jump uni-bus data path implementation. jump [ra+c2]. 5 marks
6. solution of data dependencies briefly explain. 5 marks

Paper 11
1.Insrtuction Fetch 2)
2.Arithmetic logic unit 2)
3.Memory access 3)
4.Pipeline Problems 3)
5.Related things steps requirements and data path implementation of IF procedure using RTL 5)
6.Role of step generator in a processor 5)

Paper 12
My Today cs501 Midterm Paper
20 Mcq's from lecture 20,21,22
Not from Previous Paper

Subjective
Q1:
structural RTL for mov ra, rb
Q2:
Which register holds the address of the next instruction to b executed in the processor?
Q3:
Write the structural RTL for the mov immediate instruction for the mov immediate instruction for uni-bus data path implementation Movi ra,c2
Q4:
Consider the following sequence of the instructions giving through the pipelined version of SRC
200:shl r6,r3,5
204:str r7,30
208:sub r2,r4,r5
2012:add r1,r2,r3
216:id r7,48
Q5:
Write the structure RTL description for the uni-bus data path implementation Jump[ra+2]
Q6:
Write the Structural RTL for the 'not instruction

---

mcq past past paper.20 marks
1.differenc b/w external nd internal interupt by the sysytem clock? 2 marks
2. how compiler solution to hazards? 2 marks
3. data hazard detection and correction? 3 marks
4. roll of timer generator in the processor. 3 marks
5. structural RTL for fetch instruction? 5 marks
6. Detect the hazard in the given instruction and then resolved them? 5 marks
200: shl r6, r3, 2
204: str r3, 32
208: sub r2, r4,r5
212: add r1,r2,r3
216: ld r7, 48
so easyyyyyyyyyy

How many stages are in the pipelined version of SRC? Name them…(3)
Write the structural vulearners.com RTL for the call instruction for the uni data path implementation?
Call ra, rb(5)
Q - Difference between Memory Address Register and Memory Buffer Register? [2 Marks
Q2. What do you know about Machine Exception? (2 Marks)
Which register holds the address of the next instruction to be executed in the processor?(3)
types of Machine Exception explain any two(5)

---

todays 27-05-2013 paper of CS501 VU Mid Term Paper Spring 2013
All MCQ are from past papers . 20 marks

Compare uni-bus implementation of FALCON-A with that of SRC memory size with respect to number of bits ? 2 marks

What you understand by machine exception? 2 marks

Define 3 functionality of unit control? 3 marks

Define RTL description of Mov ra,rb ? 3 marks

Define RTL description of Shiftr ra,rb,c1? 5 marks

Detect the hazard in the given instruction and then resolved them? 5 marks

200: shl r6, r3, 2

204: str r3, 32

208: sub r2, r4,r5

212: add r1,r2,r3

216: ld r7, 48

CS 501 Midterm Spring 2013

Objective mostly from previous papers.

Subjective:

Data path and Control Unit relation.---------- 2 marks
Define Two main Function of Branch Instructions.---------- 2 marks
Write RTL Structure for "movi ra, c2" ---------- 3 marks
How compiler can detect and correct hazard, why not preferred- 3 marks
Write RTL Structure for shift instruction for "shiftr ra, rb, rc ----- 5 marks
How many types of exceptions, explain. ---------- 5 marks

How many stages are in the pipelined version of SRC? Name them…(3)
Write the structural RTL for the call instruction for the uni data path implementation?
Call ra, rb(5)
Q - Difference between Memory Address Register and Memory Buffer Register? [2 Marks
Q2. What do you know about Machine Exception? (2 Marks)
Which register holds the address of the next instruction to be executed in the processor?(3)
types of Machine Exception explain any two(5)

My current paper.....
Compare unibus implementation of FALCON-A with that of SRC with respect to number of bits……2
In which stage of pipe lining the effective memory address is calculated.....2
Differentiate between Memory Address Register and Memory Buffer Register……..3
Define 3 functionality of control unit…….3
How many types of Machine Exception? Explain any two……5
Write RTL description for unconditional jump instruction
Jump [ra+c2]…….5

My 2dy papr of cs501...

70 % objective from MOAAZ file...

Q - Write a structural RTL for Shift instruction for Uni-Bus data path implementation.
shiftr ra, rb, c1 [5 Marks]

Q. Write the Structural RTL for shift right instruction. 2 marks

Q. what is pipelinin?

Q.pipeline hazard

bs itna hi yad hy...

My today's paper. (date 7-6-2014 time 8:30am)Mostly mcq's were from moaaz mcq's file and the subjective portion is

QUESTION 1: List three types of hazards that are caused by pipelining .
ANS:
Classification of Hazards

There are three categories of hazards

1. Branch Hazard

2. Structural Hazard

3. Data Hazard

Branch hazards
The instruction following a branch is always executed whether or not the branch is taken. This is called the branch delay slot. The compiler might issue a nop instruction in the branch delay slot. Branch delays cannot be avoided by forwarding schemes.

Structural hazards
A structural hazard occurs when attempting to access the same resource in different ways at the same time. It occurs when the hardware is not enough to implement pipelining properly e.g. when the machine does not support separate data and instruction memories.

QUESTION 2: Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly?
Ans:
There are two ways to increase the number of instructions executed in a given time by a processor

1. By increasing clock speed
2. By increasing number of instructions that can execute in parallel

Increasing the clock speed
• Increasing the clock speed is an IC design issue and depends on the advancements in chip technology.

• The computer architect or logic designer can not thus manipulate clock speeds to increase the throughput of the processor.

Increasing parallel execution of instructions
The computer architect cannot increase the clock speed of a microprocessor however he/she can increase the number of instructions processed per unit time. In pipelining we discussed that a number of instructions are executed in a staggered fashion, i.e. various instructions are simultaneously executing in different segments of the pipeline. Taking this concept a step further we have multiple data paths hence multiple pipelines can execute simultaneously.

QUESTION 3: Explain [c←A+c2(sign extend)]
Ans:
In this step we would add the constant c2 after sign extension to the contents of temporary register A. As a result we would have the effective address in the buffer register C, to which we need to jump.

QUESTION 4: Function of register A and C and ALSU.
QUESTION 5: RTL discription for unconditional jump
Jump(ra+c2)

QUESTION 6: What do you understand by machine exception.
Ans:
• Anything that interrupts the normal flow of execution of instructions in the processor is called an exception.

• Exceptions may be generated by an external or internal event such as a mouse click or an attempt to divide by zero etc.

• External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

Pray for me and if u realyy want to help your VU friendz then plz share your papers

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My cs501 paper. (07-06-14)

Mcqs were mostly from past papers.

Subjective questions were:

Q: Which technique is used for overlapping multiple instructions in time? (2 marks)

Q:Which register stores a previously calculated value or a value loaded from the main memory?(2 marks)

Q: What are functions of register 'A and C' and ALSU 'Arithematic Logic Shift Unit'?(3 marks)

Q: Define reset operation.What are the two operations that the reset perform?(3 marks)

Q: Write the steps involve in the processor design process.(5 marks)

Q: Identify the hazard.also how this hazard will be resolved. (5 marks)

204:str r7,30

208:sub r2,r4,r5

212:add r1,r2,r3

216:id r7,48
Regards: Amna Mishal

MY TODAYS PAPER CS501 MAY 28 SPRING 2013
Azhar bhatti email id (mbhatti2244@gmail.com)

MCQ'S only five questions from maaz file

Q 21: Write name of Two approaches for control unit. (2 marks)

Q 22: Compare unibus implementation of FALCON-A with that of SRC with respect to number of bits of PC and IR. (2 MARKS)

Q 23: How compilers can detect and correct hazards? why is not preferable?3marks

Q 24: Write the structural RTL for the mov immediate instruction for the mov immediate instruction for uni-bus data path implementation Movi ra,c2 (3marks)

Q25: Identify the Hazards in the following and also minimize them according to the certain conditions? (5)

200 sh1 r6,r3,5

204 str r7,30

208 sub r2 ,r4 , r5

212 add r1 , r2 , r3

216 id r7 ,48

Q 26: Write the Structural RTL description for un-conditional jump uni-bus data path implementation. jump [ra+c2] (5marks)

Cs50 today paper

MCQs were v ez all frm moz filez

Q1 What kind of machine exception occur ? explain 2 of them? 5mrks

Q2 write RTL of shiftr ra,rb,c1? 5mrks

Q3 write RTL of out R[ra] , c2 3mrks

Q4 What are two important features of Reset operation? 3

Q5 what are internal and external exception w.r. clock cycle time? 2

Q6 write unibus datapath registers detail of SRC and FALCON A w.r.t no. of bits and size ? 2

Good luck

100% solved

Which instruction is used to store register to memory using relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction

What is the working of Processor Status Word (PSW)?
Select correct option:
To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing
To hold the address of the next instruction in memory that is to be executed

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

What functionality is performed by the instruction “lar R3, 36” of SRC?
Select correct option:
It will load the register R3 with the contents of the memory location M [PC+36]
It will load the register R3 with the relative address itself (PC+36).
It will store the register R3 contents to the memory location M [PC+36]
No operation

In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

Which field of the machine language instruction is the "type of operation” that is to be performed?

Select correct option:
Op-code (or the operation code)
CPU registers
Memory cells
I/O locations

What functionality is performed by the instruction “str R8, 34” of SRC?
Select correct option:
It will load the register R8 with the contents of the memory location M [PC+34]
It will load the register R8 with the relative address itself (PC+34).
It will store the register R8 contents to the memory location M [PC+34]
No operation

Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction
Select correct option:
(a)& (b)
(b)&(c)
(a)&(e)
(b)&(e)

Execution time of a program with respect to the processor is calculated as:
Select correct option:
Execution Time = IC x CPI x MIPS
Execution Time = IC x CPI x T
Execution Time = CPI x T x MFLOPS
Execution Time = IC x T

Which one of the following is a bi-stable device, capable of storing one bit of Information?
Decoder
Flip-flop
Multiplexer
Diplexer

Almost every commercial computer has its own particular ————- language
3GL
English language
Higher level language
assembly language

For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory
Jump
Control
load/store
None of the given

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
Jump and branch format instructions
Immediate format instructions
Register format instructions

_____ operation is required to change the processor’s state to a known, defined value.
Change

Reset
Update
None of the given

CS501 today's 28-05-2013 Mid Term paper Spring 2013
mcq past past paper.20 marks
1.differenc b/w external nd internal interupt by the sysytem clock? 2 marks
2. how compiler solution to hazards? 2 marks
3. data hazard detection and correction? 3 marks
4. roll of timer generator in the processor. 3 marks
5. structural RTL for fetch instruction? 5 marks
6. Detect the hazard in the given instruction and then resolved them? 5 marks
200: shl r6, r3, 2
204: str r3, 32
208: sub r2, r4,r5
212: add r1,r2,r3
216: ld r7

Cs501 All current Midterm Papers Spring 2013
My today Paper of CS501 at 9 am

All MCQs for past papers just 2 mcqs are new about SCR bytes.

Subjective:

How exception may be generated write the difference between external and internal exceptions?
(3marks)
Answer:- (Page 197)
External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

Write a structural RTL for Shift instruction for Uni-Bus data path implementation.
shiftr ra, rb, c1 [5 Marks]

vi) Structural RTL for shiftr ra,rb,c1? 5marks

Write the Structural RTL for the 'not instruction' 2 marks
What is the role of timing step generator in a processor?
Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly?
Write the types of Exceptions in a machine?Write any two briefly?5marks

---

Todays Paper

20 MCQs

For which class WPF are derived? 2

What is the purpose of WPF 2D transform classes? 2

WPF combines the best attribute of some systems. write the names of three. 3

Nmea 5 built in 2D transform which are supported by "System.Window.Media" namespace. 5
Consider the following code snipple and write the output:

XmlDocument xmlDoc = new XmlDocument();

xmlDoc.LoadXml("<uni name=\'Virtual\'> university Node</uni.");

consol.writeLine(xmldoc.DocumentElement.Name);
consol.writeLine(xmldoc.DocumentElement.InnerText);

consol.readline();

---

my today paper...

80% objective from past papers of moaaz file.
Subjective:

1. what is the superscaler architecture?
2. Write the structural RTL for the call instruction for the uni data path implementation? Call ra, rb.
3.Write the structure RTL description for out instruction i.e out ra c2.
4. defirence between branch hazard and structural hazard.
5. define reset operation and its features.

best of luck.....
plzzzzzz,,,, remember in ur prayers....

CS501

My today's paper

Total 20 MCQs

all the mcqs from moazz file

Total 6 Q/A

Q1. Differentiate between uni-bus implementation of FALCON-A and SRC with respect to bus width? (2 marks)

Q2. What are branch instructions? (2 marks)

Q3. Differentiate between PC and IR? (3 marks)

Q4. Explain horizontal and vertical microcode? (3 marks)

Q5. Write structural RTL for shftr ra, rb, c1? (5 marks)

Q6. Name 3 hazards of pipeline and explain any two of them? (5 marks)

---

all paper frome mozz fil subjective and object

1)resaet opration names

2)

Detect the hazard in the given instruction and then resolved them? 5 marks

200: shl r6, r3, 2

204: str r3, 32

208: sub r2, r4,r5

212: add r1,r2,r3

216: ld r7, 48

3)Define RTL description of Shiftr ra,rb,c1? 5 marks
4)RTL given and identfy and chnage into assembly .

ans"sub RTL

5)difference latency and throughtput

6)Define RTL description of Mov ra,rb ?

My Today's paper CS501 5 June 2013

Note: (Overall paper was from past paper + current papers. 2-3 mcqs were new and one 5 marks question was new)

MCQS:

1. FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC _____wide. ►8-bits ►16-bits ►**32-bits (Page 157)** ►64-bits

1. _____control signals enable the input to the PC for receiving a value that is currently on the internal processor bus. ►**LPC (Page 172)** ►INC4 ►LC ►I

1. _____ operation is required to change the processor‟s state to a known, defined value. ►Change ►**Reset (Page 194)** ►Update ►None of the given

1. Which one of the following is a bi-stable device, capable of storing one bit of information? ►Decoder ►**Flip-Flop (Page 76)** ►Multiplexer ►Diplexer

1. The external interface of FALCON-A consists of a _____address bus and _____a data bus. ►8-bit. 8-bit ►**16-bit. 16-bit** Click here for detail ►16-bit. 24-bit ►16-bit. 32-bit

1. **What is the instruction length of the SRC processor?** ► 8 bits ► 16 bits ► **32 bits (Page 134)** ► 64 bits
2. **P: R3 ¬ R5 MAR ¬ IR** These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously? ► Arrow ¬ ► Colon : ► **Comma , (Page 69)** ► Parentheses ()

1. Prefetching can be considered a primitive form of---------- **Pipelining (Page 42)** ► Exception ► Self-execution ► Multi-processing ►

1. There are _____ types of reset operations in SRC ► **Two (Page 195)** ► Three ► Four ► Five

1. What is the working of Processor Status Word (PSW)? ►**To hold the current status of the processor. (Page 28)** ►To hold the address of the current process ►To hold the instruction that the computer is currently processing ►To hold the address of the next instruction in memory that is to be executed

1. Almost every commercial computer has its own particular ---------- language ►3GL ►English language ►Higher level language ►**assembly language**

1. Which of the instruction is used to load register from memory using a relative address? ►ld instruction ►**ldr instruction (Page 47)** ►lar instruction ►str instruction

1. Which one of the following portions of an instruction represents the operation to be performed? ►Address ►Instruction code ►Opcode ►**Operand**

1. Which one of the following registers holds the address of the next instruction to be executed?

Accumulator
Address Mask
Instruction Register
Program Counter

1. Which one of the following circuit design levels is called the gate level?
   Select correct option:

   Logic Design Level
   Circuit Level
   Mask Level
   None of the given

1. For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
   Select correct option:

   Registers
   Control signals
   Memory
   None of the given

1. Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?

Select correct option:

Arithmetic

Control

Data transfer
Floating point

Subjective paper:

1. **1. What function is performed by the reset operation of a processor? 2 marks**

Answer:- (Page 194)
Reset operation is required to change the processor's state to a known, defined value. The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

1. **What is relation b/w data path and control unit in SRC processors? 2 marks**

Answer:- (Page 186)
By means of the control signals, the control unit instructs the data path what to do in every clock cycle during the execution of instructions.

1. **Describe three main functions of control unit. 3 marks**

Answer:-

• It carries out many tasks such as decoding, fetching, handling the execution and finally storing the results.

• It interprets the instructions.

• It regulates the time controls of the processor

1. **Write the structural RTL for the mov instruction for the uni data path implementation? mov ra, rb 3 marks**

Answer:- (Page 164)

1. **Write the structural RTL for the call instruction for the uni data path implementation?**

Call ra, rb 5 marks

Answer:- (Page 165)

1. **6. Data dependency is a cause of hazards in pipelining. What are the different techniques used to resolve data dependency? 5 marks**

Pipeline stalls

Consider the following sequence of instructions going through the SRC pipeline

200: shl r6, r3, 2

204: str r3, 32

208: sub r2, r4,r5

212: add r1,r2,r3

216: ld r7, 48

There is a data hazard between instruction three and four that can be resolved by using pipeline stalls or bubbles

When using pipeline stalls, nop instructions are placed in between dependent instructions.

The logic behind this scheme is that if opcode in stage 2 and 3 are both alu, and if ra in stage 3 is the same as rb or rc in stage 2, then a pause signal is issued to insert a bubble between stage 3 and 2. Similar logic is used for detecting hazards between stage 2 and 4 and stage 4 and 5.

Data Forwarding

By adding data forwarding mechanism to the SRC data path, the stalls can be completely eliminated at least for the ALU instructions. The hazard detection is required between stages 3 and 4, and between stages 3 and 5. The testing and forwarding circuits employ wider IRs to store the data required in later stages. The logic behind this method is that if the ALU is activated for both 3 and 5 and ra in 5 is the same as rb in 3 then Z5 which hold the currently loaded or calculated result is directly forwarded to X3. Similarly, if both are ALU operations and instruction in stage 3 does not employ immediate operands then value of Z5 is transferred to Y3. Similar logic is used to forward data between stage 3 and 4.

Just got back from paper, it was quite lengthy, not tough not easy though...50% mcqs were from moaz file , 50% new.

New MCQs

1. Superscalers don't have branch hazard.

True or False

2. Intel P6 has _____

a four pipelines. b multiple IU,FPU units. c multiple IU,FPU and BPU units. d only BPU.

3. VLIW deals efficiently with branch hazards

true or false

4. processor can be overclocked by replacing oscillators

true or false

5 RISC processor can execute complex instructions as CISC does

true or false

6. For Time critical applications we use

RISC

CISC

Both

None of above

subjective

1. Structural RTL for unibus SRC for not ra,rb. write all steps from T0 to onward. 2Marks

2. what are stalls? where we shoud use?? what is impact of using stalls? 2 Marks

3. Write the all stages of pipeline, and explain each briefly? 3 Marks

4. What do you know about execution roll back? when and where we use it? 3 Marks

5. Write Structural RTL and control signals detail for all timing for instruction fetch? 5 Marks

6.a. How can we increase processor speed? explain all methods briefly? b. How parallelism achieved, give brief detail and example? 5 Marks

---

my today too much ezzz

mostly mcqz were new but too much ez n some mcq's from moaz file

subjective b mostly past paper me se he tha

1. write the structure RTL for not instruction?

2: difference between hardwired and microcoded contorl unit?

3: difference between pipeline and instruction level parallelism?

4write the name of two approches to achieve instruction level parallelism?

5:list the control signal of the RTL sturucture add ra, rb ,rc?

6:write the name of five exmple can occure in excution?

---

today Paper CS501
Total question = 23

2 short question = 2 marks for each

3 Long question = 5 marks for each

Mcqs from moazz file

q1: calculate the word size from given instruction

q2: mechanism use to control data unit .. write name

q3: Main characteristic of d-flip flop and its truth table

q4: 5 Characteristic of EAGLE processor

q5: How many exception are there ? explain any 2

Cs501 today paper .
50% mcqs was from past moaaz file.
Questions:
1:Reset operation.3mrks
2:Exception ...explain 2 types of exception.5mrks
3:Nop and reset are from which categroy of instructions.3mark
4:Table was given.....calculate Ic and execution speed .s5marks
5:5th question mn b table given tha ...kch find krna tha yad ni a ra .5marks ka tha
Cs501 today paper 9/12/2017
Mcq's 90% past papers ma sa thay
2 Q. 3 marks and 3 Q.5 marks k thy
Q.1 what is relative address and how can we represent it in structural RTL? 3 marks
Q.2 Diffence b/w Hardwired control unit and Microcoded control unit? 3 marks
Q.3 write four characteristics of SPARC register window? 5 marks
q.5 write 2 address and 3 address of expression
a=(b+c)*d_e? 5 marks
Best of luck

---

1. Write down any four characteristics of SPARC Register Windows.

2. What are the differences between pipelining and instruction level parallelism?

3. Suppose that an instruction set architecture has an immediate instruction format with the following fields and sizes:

You need to calculate instruction word size for the above instruction format.

Very very very easy paper

All mcqs was from Past paper No new mcqs (Moaaz file + past quizes 2014 and 2013)

Subjective

Which technique is used for overlapping multiple instructions in time? (2 marks)

Explain [c←A+c2(sign extend)] (2 marks)

Write any three stages of designing and implemention phase of pipelining (3 marks)

Dif b/w PC and IR (3marks)

Which registers are used in every steps of pipelining (5 marks)

RTL for Jz ra (c2) (5 marks)

Best of Luck ..... :) :)

Today Paper @ 2:30 PM.

Paper was very easy..

Almost all MCQs from Past Papers..

Subjective:

What is the Function of microprogram? (2)

Structured RTL for "mov" ra, rb? (3)

Describe the working of a general micro-coded controller? (3)

Write name of all the registers used in the task of pipe lining? (5)

Structured RTL for add operation? (5)

Which technique is used for overlapping multiple instructions in time? (2 marks)

Ans:

Pipeline technique is used for overlapping multiple instructions in time

Explain [c←A+c2(sign extend)] (2 marks)

In this step we would add the constant c2 after sign extension to the contents of temporary register A. As a result we would have the effective address in the buffer register C, to which we need to jump.

Write any three stages of designing and implementation phase of pipelining (3 marks)

Adapting the instructions to pipelined execution
Designing the pipelined data path
Generating control signals

Dif b/w PC and IR (3marks)
Two special registers, the Program Counter (PC) and the Instruction Register (IR). PC points to the next instruction to be executed, and the IR holds the current instruction.

Which registers are used in every steps of pipelining (5 marks)

RTL for Jz ra (c2) (5 marks)

Best of Luck ..... :) :)

Paper was very easy..

Almost all MCQs from Past Papers..

Subjective:

What is the Function of microprogram? (2)
Ans:

A collection of microinstructions is called a microprogram. These microprograms generate the sequence of necessary control signals required to process an instruction. These microprograms are stored in a memory called the control store.

Structured RTL for "mov" ra, rb? (3)

Describe the working of a general micro-coded controller? (3)
Ans:
Working of a general microcoded controller

A microcoded controller works in the same way as a small general purpose computer.

1. Fetch a micro-instruction and increment micro-PC.

2. Execute the instruction present in micro-IR.

3. Fetch the next instruction and so on…

Write name of all the registers used in the task of pipe lining? (5)
Ans:

IR2,IR3,IR4,IR5,PC2,X3,Y3,Z4,Z5,MD3,MD4

Today my paper

80% objective from Moaaz file and subjective is below.

Explain horizontal and vertical microcode? (3 marks)

Ans;

Horizontal and vertical microcode schemes
In horizontal microcode schemes, there are no intermediate decoders and the control word bits are directly connected to their destination i.e. each bit in the control word is directly connected to some control signal and the total number of bits in the control word is equal to the total number of control signals in the CPU. Vertical microcode schemes employ an extra level of decoding to reduce the control word width. From an n bit control word we may have 2n bit signal values. However, a completely vertical scheme is not feasible because of the high degree of fan out.

3. Write the structure RTL description for out instruction i.e out ra, c2. 3 Marks
Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly?5 Marks

Ans:
There are two ways to increase the number of instructions executed in a given time by a processor

1. By increasing clock speed
2. By increasing number of instructions that can execute in parallel

Increasing the clock speed
• Increasing the clock speed is an IC design issue and depends on the advancements in chip technology.

• The computer architect or logic designer cannot thus manipulate clock speeds to increase the throughput of the processor.

Increasing parallel execution of instructions
The computer architect cannot increase the clock speed of a microprocessor however he/she can increase the number of instructions processed per unit time. In pipelining we discussed that a number of instructions are executed in a staggered fashion, i.e. various instructions are simultaneously executing in different segments of the pipeline. Taking this concept a step further we have multiple data paths hence multiple pipelines can execute simultaneously.

Question 1: which technique is used for overlapping multiple instructions simultaneously ? (2)
Question 2: what is the functionality of LMBR control signal in SRC ? (2)
Question 3: What are the two ways to increase increasing a processor's throughput ?Explain each one briefly (5)
Question 4: What is the Function of micro and macro programs ? (2)

MCQs Moaaz ki file sy he thy thory sy baki sb new

90% mcq's was from moaz file.

and the subjective was also easy.

the question which i have remembered,below these are:

1-Difference b/w branch and structural hazards.(5 marks)

2-Which registers are used in every steps of pipelining (5 marks)
3-Write any two stages of designing and implementation phase of pipelining (2 marks)
4-Structured RTL for "mov" ra, rb? (3 marks)

5-SRC five-stage pipeline. arranged them,These stages were given.Those five stages are given below:

1. Instruction Fetch
2. Instruction decode/operand fetch
3. ALU operation
4. Memory access
5. Register write

and these are arranged,i have copied from the handouts as it is.(3 marks)

sorry,1 question of 2 marks...i forgot .
And All the best to all the Students

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mine t0day paper!!!!

-0bective-
alm0st fr0m past pperz !!
-subjective-
Q#01: write bout mechine execution ? (2)
Q#02: Two approaches for control unit (2)

Q#03: Register a & c Nd alsu (3)

Q#04: micro-c0ntr0lled register (3)

Q#05: structural RTL for mov ra, rb (5)

Q#06: Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly? (5)

(i ain't remember the xact statement! but i thought itz Literally

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CS501_Midterm paper fall 2014 (Held On Dated 19-JAN-2015)
Total Questions: 26 Total Marks: 40
Objective: 20 marks, Subjective 20 marks
Q.21 Write difference between external and internal exceptions? (2 marks)

Answer:
External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

Q.22 what is relation between data path and control unit in SRC processors? (2 marks)
Answer:
By means of the control signals, the control unit instructs the data path what to do in every clock cycle during the execution of instructions.
Q.23 Describe role of timing step generator? (3 marks)
Answer:
Timing Step Generator
To ensure the correct and controlled execution of instructions in a program, and all the related operations, a timing device is required. This is to ensure that the operations of essentially different instructions do not mix up in time. There exists a „timing step generator" that provides mutually exclusive and sequential timing intervals.

Q.24 Explain horizontal and vertical microcode schemes? (3 marks)
Answer: (page 41)
Horizontal and vertical microcode schemes
In horizontal microcode schemes, there are no intermediate decoders and the control word bits are directly connected to their destination i.e. each bit in the control word is directly connected to some control signal and the total number of bits in the control word is equal to the total number of control signals in the CPU. Vertical microcode schemes employ an extra level of decoding to reduce the control word width. From an n bit control word we may have 2n bit signal values. However, a completely vertical scheme is not feasible because of the high degree of fan out.

Q.25 Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly? (5 marks)
Answer:
There are two ways to increase the number of instructions executed in a given time by a processor
1. By increasing clock speed
2. By increasing number of instructions that can execute in parallel
Increasing the clock speed
• Increasing the clock speed is an IC design issue and depends on the advancements in chip technology.
• The computer architect or logic designer cannot thus manipulate clock speeds to increase the throughput of the processor.

Q.26 Write boolean equation of the logic circuit ?(page 189 or 201) (5 marks)

Answer: -
PCout=T0+T3.(OP20+OP22)+T4.(OP16+OP17+OP18+OP19)

All objective from past papers mostly from moaaz file
Remember me in your Prayers!

My Recent paper of cs501 Advance computer architecture
20 objective Questions
Subjective :
Question 21:
What is the functionality of LMBR control signals in SRc?
Question 22:

Write the function of the rest operation of a processor?
Question 23:
Write the main difference between the MAR/MBR?
Question 24:
What is the two approvhes to achieve instruction level parallelism?
Question 25:
Write the related timmings steps of register to register add operation using RTL?
Question 26:
Write two ways to increase increasing process through out?

Wish u best of luck All of u

CS 501 Solved Current paper
Solved by Aysha Ashi and Precious Girl

Q.1 Write difference between external and internal exceptions? (2 marks)
Answer:

External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

Q.2 what is relation between data path and control unit in SRC processors? (2 marks)
Answer:

By means of the control signals, the control unit instructs the data path what to do in every clock cycle during the execution of instructions.

Q.3 Describe role of timing step generator? (3 marks)
Answer:

Timing Step Generator
To ensure the correct and controlled execution of instructions in a program, and all the related operations, a timing device is required. This is to ensure that the operations of essentially different instructions do not mix up in time. There exists a „timing step generator" that provides mutually exclusive and sequential timing intervals.

Q.4 Explain horizontal and vertical microcode schemes? (3 marks)
Answer: (page 41)

Horizontal and vertical microcode schemes
In horizontal microcode schemes, there are no intermediate decoders and the control word bits are directly connected to their destination i.e. each bit in the control word is directly connected to some control signal and the total number of bits in the control word is equal to the total number of control signals in the CPU. Vertical microcode schemes employ an extra level of decoding to reduce the control word width. From an n bit control word we may have 2n bit signal values. However, a completely vertical scheme is not feasible because of the high degree of fan out.

Q.5 Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly? (5 marks)
Answer:

There are two ways to increase the number of instructions executed in a given time by a processor
1. By increasing clock speed
2. By increasing number of instructions that can execute in parallel

Increasing the clock speed
• Increasing the clock speed is an IC design issue and depends on the advancements in chip technology.
• The computer architect or logic designer cannot thus manipulate clock speeds to increase the throughput of the processor.

Q.6 Write boolean equation of the logic circuit ?(5 marks)

Answer: -

PCout=T0+T3.(OP20+OP22)+T4.(OP16+OP17+OP18+OP19)

Q#7: structural RTL for mov ra, rb (5)
Q#8: Two approaches for control unit (2)

Answer:Additionally, there are two different approaches to the control unit design; it can be either hard-wired or microprogrammed.

Question 9: which technique is used for overlapping multiple instructions simultaneously ? (2)
Which technique is used for overlapping multiple instructions in time? (2 marks)
Ans:
Pipeline technique is used for overlapping multiple instructions in time.

QNo 10 Explain [c←A+c2(sign extend)] (2 marks)

In this step we would add the constant c2 after sign extension to the contents of temporary register A. As a result we would have the effective address in the buffer register C, to which we need to jump.

Q #11 Write any three stages of designing and implementation phase of pipelining?
(3 marks)
Ans:
Adapting the instructions to pipelined execution

Designing the pipelined data path

Generating control signals

Q#12 Dif b/w PC and IR (3marks)

Two special registers, the Program Counter (PC) and the Instruction Register (IR). PC points to the next instruction to be executed, and the IR holds the current instruction.

Q#13 What is the Function of microprogram? (2)
Ans:
A collection of microinstructions is called a microprogram. These microprograms generate the sequence of necessary control signals required to process an instruction. These microprograms are stored in a memory called the control store.

Q#14Describe the working of a general micro-coded controller? (3)
Ans:
Working of a general microcoded controller

A microcoded controller works in the same way as a small general purpose computer.

1. Fetch a micro-instruction and increment micro-PC.

2. Execute the instruction present in micro-IR.

3. Fetch the next instruction and so on…

Q#15Write name of all the registers used in the task of pipe lining? (5)
Ans:
IR2,IR3,IR4,IR5,PC2,X3,Y3,Z4,Z5,MD3,MD4

Q no16
Explain horizontal and vertical microcode? (3 marks)
Ans;
Horizontal and vertical microcode schemes

In horizontal microcode schemes, there are no intermediate decoders and the control word bits are directly connected to their destination i.e. each bit in the control word is directly connected to some control signal and the total number of bits in the control word is equal to the total number of control signals in the CPU. Vertical microcode schemes employ an extra level of decoding to reduce the control word width. From an n bit control word we may have 2n bit signal values. However, a completely vertical scheme is not feasible because of the high degree of fan out.

What are the two ways to increase increasing a processor's throughput ?Explain each one briefly (5)
Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly?5 Marks
Ans:
There are two ways to increase the number of instructions executed in a given time by a processor

By increasing clock speed

By increasing number of instructions that can execute in parallel

Increasing the clock speed
• Increasing the clock speed is an IC design issue and depends on the advancements in chip technology.

• The computer architect or logic designer cannot thus manipulate clock speeds to increase the throughput of the processor.

Increasing parallel execution of instructions
The computer architect cannot increase the clock speed of a microprocessor however he/she can increase the number of instructions processed per unit time. In pipelining we discussed that a number of instructions are executed in a staggered fashion, i.e. various instructions are simultaneously executing in different segments of the pipeline. Taking this concept a step further we have multiple data paths hence multiple pipelines can execute simultaneously.

Write any three stages of designing and implemention phase of pipelining (3 marks)
3-Write any two stages of designing and implementation phase of pipelining (2 marks)
These stages were given.Those five stages are given below:

Instruction Fetch
2. Instruction decode/operand fetch
3. ALU operation
4. Memory access
5. Register write

1-Difference b/w branch and structural hazards.(5 marks)
There are three categories of hazards

1. Branch Hazard 2. Structural Hazard 3. Data Hazard

Branch hazards

The instruction following a branch is always executed whether or not the branch is taken. This is called the branch delay slot. The compiler might issue a nop instruction in the branch delay slot. Branch delays cannot be avoided by forwarding schemes.

Structural hazards

A structural hazard occurs when attempting to access the same resource in different ways at the same time. It occurs when the hardware is not enough to implement pipelining properly e.g. when the machine does not support separate data and instruction memories.

Data hazards

Data hazard occur when an instruction attempts to access some data value that has not yet been updated by the previous instruction.

Structured RTL for add operation? (5)

RTL for Jz ra (c2) (5 marks)

not ra, rb

what is the functionality of LMBR control signal in SRC ? (2)

LMBR is the control signal to enable write of the MBR (Memory Buffer Register). It will obtain its value from the CPU external data bus.

What is the Function of micro and macro programs ? (2)

Solution:
Macro: In assembler language, a macro definition defines how to expand a single language statement or computer instruction into a number of instructions.
Micro: A collection of microinstructions is called a microprogram. These microprograms generate the sequence of necessary control signals required to process an instruction

Which registers are used in every steps of pipelining (5 marks)

Ans: Temporary pipelining registers are used in every steps of pipelining. Registers are IR2,IR3,IR4,IR5,PC2,X3,Y3,Z4,Z5,MD3,MD4.

write about mechine execution ? (2)

non-pipelined machine there is a single instruction

add r4, r2, r3 being processed at a given time, while in a pipelined machine, five

different instructions are being processed simultaneously

Q#03: Register A & c and ALSU (3)

Solution:
ALSU: There is a 32-bit Arithmetic Logic Shift Unit, as shown in the diagram. It takes input from memory or registers via the bus, computes the result according to the

control signals applied to it, and places it in the register C, from where it is finally

transferred to its destination.

Registers A and C
The registers A and C are required to hold an operand or result value while the

bus is busy transmitting some other value. Both these registers are programmer

invisible.

What is Latency & throughput
Solution:
Latency is defined as the time required to process a single instruction, while throughput is

defined as the number of instructions processed per second.

Write the structure RTL description for out instruction i.e out ra, c2. 3 Marks

Solution:

What is diff b/w MAR and MBR?

MAR: The Memory Address Register takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that

location onto the memory sub-system.

MBR: The Memory Buffer Register has a bi-directional connection with both the memory sub-system and the registers and ALSU. It holds the data during its

transmission to and from memory.

Over all 17 mcqs from moaz file ,5 subjective from also moaz file

i) How many stages are in the pipelined version of SRC? Name them 3 marks

ii)Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly? 5 mark

struclal RTL of instruction fetching sa related tha ....5 marks

differentiate Hard reset and Soft reset?.....2marks

Comparing the uni-bus implementation of FALCON-A with that of SRC results in width 2marks

Ek question bhol gya

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my today paper

90% mcqs from moeez file

subjective are from past papers

1- Two approaches for control unit.
Answer:- (Page 150)
Additionally, there are two different approaches to the control unit design; it can be either hard-wired or microprogrammed
Write the structural RTL for the following instruction for the uni- bus path implementation in ra,rc ?3
3 marks
What function is performed by the reset operation of a processor?2
what is trace and debugging exception?3

Write the structure RTL description for the uni-bus data path implementation Jump[ra+2] (5 Marks)

My toady paper,

1: which register holds the address of the next instruction to be executed?

2: which technique is used to overlapping multiple instruction simultaniously?

3: RTL for call ra,rb?

4: Rtl for in ra,c2

5: reset operation sy tha sawal

6: difference between branch hazard ans structual hazard....

best of luck

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cs501 Current Midterm Paper
40% paper from past papers:
5,6 mcqz from FALCON 's topic.
1.Write features of FALOCON-E. (3)
2.Describe the "Trace and debugging" exception.
(3)
3.FALCON -E k according likhna tha
i.Number of register
ii)size of register
iii)Memory space between word (5)
4.Pipelining ke implementation (5

1.Write features of FALOCON-E. (3)
The following features characterize the FALCON-E
• Fixed instruction size, which is 32 bits. So the instruction size is 1 word.
• All ALU instructions have three operands
• Memory access is possible only through the load and store instructions. Also, only
a limited addressing modes are supported by the FALCON-E

4.Pipelining ke implementation (5
ANS:
three parts:
1. Adapting the instructions to pipelined execution
2. Designing the pipelined data path
3. Generating control signals

Q3: briefly explain instruction decode/operand fetch stage of pipeline.
Ans:
In this stage the instruction are fetched from the register file.
If the instruction is add r1, r2, r3 the
registers r2 and r3 will be read into the temporary pipeline
registers.
Q3 : How many types of Exception occurs in a machine? ecplain it.

ANS:
external and internal exceptions

External exceptions generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock
Q6 Write 2 difference Eagle and modified eagle.
Ans:
The EAGLE

is an accumulator-based machine. It is a simple processor that will help us in our understanding of the processor design process.
The Modified EAGLE
The modified EAGLE is an improved version of the processor EAGLE.
It is a processor that will help us in our understanding simple, yet complex enough to illustrate the various concepts of a processor design.

Q1: any 3 instructions which belong to type B instruction format of falcon-E processor.
Ans:
push (op-code = 8)
pop (op-code = 9)
ld (op-code = 10)
st (op-code = 12)

1. What do you understand about machine exception.
Ans:• Anything that interrupts the normal flow of execution of instructions in the processor is called an exception.
• Exceptions may be generated by an external or internal event such as a mouse click or an attempt to divide by zero etc.
• External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)
Q1 : Write any 3 Step involved in designing and implemntation of Pipeline machine.
1. Instruction fetch
the instruction is fetched from the
instruction memory in this stage.
.
2. Instruction decode/operand fetch
In this stage the instruction are fetched from the register file.
If the instruction is add r1, r2, r3 the
registers r2 and r3 will be read pipeline
registers.
3. ALU5 operation
the instruction is fetched from the ALU
such as addition,subtraction, etc.

The result is stored into temporary pipeline
registers. In case of a memory access such as a load or a store
instruction, the ALU calculates the effective memory address
in this stage.

FALCON stands for First Architecture for Learning Computer Organization and

Networks. FALCON-E is a General-Purpose

Register machine that is simple, yet is able to elucidate the fundamentals of computer

design and architecture.

The FALCON-E is characterized by the following

- • Eight General Purpose Registers (GPRs), named R0, R1…R7. Each registers is 4 bytes long (32-bit registers).
- • Two special purposes registers, named BP and SP. These registers are also 32-bit in length.
- • Two special registers, the Program Counter (PC) and the Instruction Register (IR). PC points to the next instruction to be executed, and the IR holds the current

instruction.

- • Memory word size is 32 bits (4

bytes).

- • Memory space is 232 bytes
- • Memory is organized as 1-byte

cells, and hence it is 232 x 8

bits.

- • Memory is accessed in 32-bit

words (4-byte chunks, or 4 consecutive cells)

nop (op-code = 0)
This instruction instructs the processor to do nothing. It is generally useful in pipelining. (if you take a look at pipelining topic you will understand op-code)

The use of RTL (an acronym for the Register Transfer Language) to describe the FALCON-A is discussed in this section. FALCON-A is the sample machine we are building in order to enhance our understanding of processors and their architecture.

Q3: Answer on page 163

My Today cs501 Paper @ 10:30 Muhammad Shahroz Munir :)
Q.1 Structural RTL for addition
instruction
add ra, rb, rc
Q.2 Structural RTL for add immediate instruction
addi ra, rb, c1
Q3 Write down any four characteristics of SPAC register windows.
5 marks
Q4 difference between external and internal exceptions?
Q5 uni- bus path implementation difference between PC and IR
Q6 Which register holds the address of the next instruction to be executed in the processor?

Mcqs were 90% from moaaz file

1. Define Lmbr.
2. role of timing step generator
3. Differentiate between external and internal exceptions.
4. List three types of hazards that are caused by pipelining .
5. Make structural rtl for register to register add instruction
6. Difference between program exception and hardware exception.
   pray for me and work hard bht easy paper th

Today Paper
Total Questions = 26
Total Marks = 40
Total MCQs of 1 Mark = 20
Short Subjective Question of 2 Marks = 2
Subjective Question of 3 Marks = 2
Subjective Questions of 5 Marks = 2

Which register holds the instruction that is being executed? 2marks
Which technique is used for overlapping multiple instructions simultaneously?2 marks
Write the Structural RTL for the "mov" instruction i.e. mov ra, rb. 3marks
Write the Structural RTL for the "mov" instruction i.e. mov ra, rb. 3marks

Write the related timing steps requirements and data path implementations of Instruction Fetch procedure using structural RTL 5marks
How many types of exceptions can occur in a machine? Explain any two of them. 5marks

---

ASSALAM O ALAIKUM,.....

MY PPR WAS DONE OK BY THE GRACE OF ALLAH ALMIGHTY.

mcqs 70% from moazz file rather some are new 2 are from latency and throughput.

How many types of exceptions can occur in a machine? Explain any two of them. 5marks

types of exceptions

- Program Exceptions
- Hardware Exceptions
- Trace and debugging Exceptions
- Nonmaskable Exceptions
- Interrupts (External Exceptions)

Program Exceptions
These are exceptions raised during the process of decoding and executing the instruction. Examples are illegal instruction, raised in response to executing an instruction which does not belong to the instruction set. Another example would be the privileged instruction exception.
• Hardware Exceptions
There are various kinds of hardware exceptions. An example would be of a timer which raises an exception when it has counted down to zero.
2nd is structural RTL out ra,c2 3marks Answer:- (Page 164)

Write the structural RTL for the mov immediate instruction for the mov immediate instruction for uni-bus data path implementation Movi ra,c2 (3marks)
Answer:- (Page 164)

one is define hard reset and soft reset.2

Write approaches to achieve instruction level parallelism2.

best of luck alls

My today's Paper
Total Questions = 26
Total Marks = 40
Total MCQs of 1 Mark = 20
Short Subjective Question of 2 Marks = 2
Subjective Question of 3 Marks = 2
Subjective Questions of 5 Marks = 2

MCQ's totally from past papers

Subjective paper..

1. Explain [c <-- A+C2 (Sign extend);] Marks(2)
2. In which stage of pipeline,the effective memory Address is calculated? (2)
3. what are three categories of pipeline Hazards? (3)
4. Write the structural RTL for the following instruction for the uni-bus path implementation? in ra,rc (3)
5. Write the structure RTL description for the uni-bus data path implementationJump[ra+2] (5)
6. Write five stages of pipeline and their registers which use in pipeline stages step by step (5)

Overall paper bht bht easy tha

MCQs were mostly from Moaz File and below is the subjective questions with solution;

Q1: Which register is used to hold source operand and the result of the arithmetic or logical operation?
Solution:
Accumulator Register.

Q2: Briefly explain the types of branch?
Solution
Branch:
Branch instruction branches to address In Rb depending on the condition in rc.

Branch with link:
Branch link branches to address in Rb depending on condition in rc Additionally, it copies the PC into ra before branching.

Q3: What function is performed by the reset operation of a processor and differentiate Hard reset and Soft reset.
Solution:
Two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Hard Reset:
The SRC should perform a hard reset upon receiving a start (strt) signal. This initializes the PC and the general registers.

Soft Reset:
The SRC should perform a soft reset upon receiving a reset (rst) signal. The soft reset results in initialization of PC only.

Q4: Structural RTL for in ra, c2
Solution:

Time Step	**RTL**
T0 to T2	Instruction Fetch
T3	C<-IO[c2]
T4	R[ra]<-C

Q5: Write RTL and control signal notation for following add instruction:
add ra, rb, rc;
Solution:

Time Step	**RTL**	**Control Signal**
T0 to T2	Instruction Fetch	As before
T3	A<- R[rb];	RBE, R2BUS, LA
T4	C<-A+R[rc];	RCE, R2BUS, ADD, LC
T5	R[ra]<-C	Cout, RAE, BUS2R

Q6: Describe 5 examples of exception when it occur?
Solution:
Program Exceptions
These are exceptions raised during the process of decoding and executing the instruction. Examples are illegal instruction, raised in response to executing an instruction which does not belong to the instruction set. Another example would be the privileged instruction exception.

Hardware Exceptions
There are various kinds of hardware exceptions. An example would be of a timer which raises an exception when it has counted down to zero.

Trace and debugging Exceptions
Variable trace and debugging is a tricky task. An easy approach to make it possible is through the use of traps. The exception handler which would be called after each instruction execution allows examination of the program variables.

Nonmaskable Exceptions

These are high priority exceptions reserved for events with catastrophic consequences such as power loss. These exceptions cannot be suppressed by the processor under any condition. In case of a power loss the processor might try to save the system state to the hard drive, or alert an alternate power supply.

Interrupts (External Exceptions)
Exception handlers may be written for external interrupts, thus allowing programs to respond to external events such as keyboard or mouse events.

MY CS501 PAPER

1. Compare FALCON-A eith SRC bits of MAR and MBR? 2Marks
2. Difference b/w executing machine instructions with and without pipelining?
3. Structural RTL for "out" out,ra,c2 3 Marks
4. Name of 3 step of designing and implementation a pipeline machine?
5. Structural RTL for "un conditional jump" jump[ra,c2] 5Marks
6. Diference pipelining and instruction level parallelism?

MCQS 12 previous say thay 8 new thy 2 ,3 may nay tukkay
lagay new may baki saray mujay aatay thay
1-which register holds the address of the next instruction to be executed? 2
2-Differentiate between hardwired n microcoded control system 2
3-AC,PC,IR define them. 3
4-hazard how complie detect,correct,why complier correction iz not conside good?
5-Write the two ways to increase the number of instruction in a
given time by the processor? Explain each one briefly? 5 marks
6-add,ra,rb,rc 5
