MIDTERM EXAMINATION
Spring 2012
CS501- Advance Computer Architecture

1- Two approaches for control unit.

Answer:- (Page 150)

Additionally, there are two different approaches to the control unit design; it can be either hard-wired or micro-programmed

2- What is micro program?

Answer:- (Page 222)

A collection of microinstructions is called a microprogram. These microprograms generate the sequence of necessary control signals required to process an instruction. These microprograms are stored in a memory called the control store.

3- structural RTL for mov ra, rb

Answer:- (Page 164)

Step	RTL
T0-T2	Instruction fetch
T3	C ← R[rb];
T4	R[ra] ← C;

دنیا میں سب سے مشکل کام اپنی اصلاح اور سب سے آسان کام دوسروں پر نکتہ چینی کرنا ہے

4- Structural RTL and explanation for instruction fetch.

Answer:- (Page 152)

The instruction fetch procedure takes three time steps as shown in the table. During the first time step, T0, address of the instruction is moved to the Memory Address Register (MAR) and value of PC is incremented. In T1 the instruction is brought from the memory into the Memory Buffer Register (MBR), and the incremented PC is updated. In the third and final timestep of the instruction fetch phase, the instruction from the memory buffer register is written into the IR for execution. What follows the instruction fetch phase, is the instruction execution phase. The number of timing steps taken by the execution phase generally depends on the type and function of instruction. The more complex the instruction and its implementation, the more timing steps it will require completing execution. In the following discussion, we will take a look at various types of instructions, related timing steps requirements and data path implementations of these in terms of the structural RTL.

	Step	RTL
Instruction Fetch	T0	MAR ← PC, C ← PC + 4;
	T1	MBR ← M[MAR], PC ← C;
	T2	IR ← MBR;

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Q1. Which register holds the address of the next instruction to be executed in the processor? (2 Marks)

Answer:- (Page 28)

The program counter (PC) that holds the address of the next instruction in memory that is to be executed.

Q2. What do you know about Machine Exception? (2 Marks)

Answer:- (Page 197)

• Anything that interrupts the normal flow of execution of instructions in the processor is called an exception.
• Exceptions may be generated by an external or internal event such as a mouse click or an attempt to divide by zero etc.
• External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

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Q3. How exception may be generated write the difference between external and internal exceptions? (3marks)

Answer:- (Page 197)

External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

Q4. Write the structure RTL description for mov instruction (3 Marks)

Answer:- (Page 164)

In mov instruction the data in register rb, which is the source register, is to be moved in the register ra, which is the destination register. In first three steps, mov instruction is fetched. In step T3 the contents of register rb are placed in buffer register C through the ALSU unit while in step T4 the buffer register C transfers the data to register ra through internal uni-bus.

Q5. Write the structure RTL description for shift instruction? (5 Marks)

Answer:- (Page 157)

Shift instructions are rather complicated in the sense that they require extra hardware to hold and decrement the count. For an ALSU that can perform only single bit shifts, the data must be repeatedly cycled through the ALSU and the count decremented until it reaches zero. This approach presents some timing problems, which can be overcome by employing multiple-bit shifts using a barrel shifter.

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Q - Write a structural RTL for Shift instruction for Uni-Bus data path implementation.
shiftr ra, rb, c1 [5 Marks]

Answer:- (Page 163)

Step	RTL
T0-T2	Instruction fetch
T3	n<4..0> ← IR<4..0>;
T4	C ← (Nα0) © R[rb]<15..N>;
T5	R[ra] ← C;

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Q - Write down one Advantage and Disadvantage of Microprogramming? [3 Marks]
Answer:- Click here for detail
Advantages
Great sophistication in the user instruction set can be achieved for relatively low cost. Adding new instructions is cheap.

Disadvantages
For a simple machine, the extra hardware needed for the control store and sequencer may be more complex than hardwiring.

Q - Difference between Memory Address Register and Memory Buffer Register? [2 Marks]
Answer:- (Page 151)
MAR
The Memory Address Register takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system.

MBR
The Memory Buffer Register has a bi-directional connection with both the memory sub-system and the registers and ALSU. It holds the data during its transmission to and from memory.

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Which register holds the address of the next instruction to b executed in the processor? 2 marks
Answer:- Rep

Write the structural RTL for the following instruction for the uni- bus path implementation? in ra,rc 3 marks

How exception may b generated write the difference between external and internal exceptions? 3 marks
Answer:- Rep

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Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly? 5 marks

Answer:- (Page 219)

There are two ways to increase the number of instructions executed in a given time by a processor

- By increasing the clock speed
- By increasing the number of instructions that can execute in parallel

Increasing the clock speed

• Increasing the clock speed is an IC design issue and depends on the advancements in chip technology.

• The computer architect or logic designer can not thus manipulate clock speeds to increase the throughput of the processor.

Increasing parallel execution of instructions

The computer architect cannot increase the clock speed of a microprocessor however he/she can increase the number of instructions processed per unit time. In pipelining we discussed that a number of instructions are executed in a staggered fashion, i.e. various instructions are simultaneously executing in different segments of the pipeline. Taking this concept a step further we have multiple data paths hence multiple pipelines can execute simultaneously.

Write the structural RTL for the call instruction for the uni data path implementation?

Call ra, rb

Answer:- (Page 165)

Step	RTL
T0-T2	Instruction Fetch
T3	C ← PC;
T4	R[ra] ← C;
T5	C ← R[rb];
T6	PC ← C;

بری صحبت سے تنہائی بہتر ہے اور تنہائی سے نیک صحبت بہتر ہے

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Which registers hold the instructions that is being executed?(2 Marks)
Answer:- (Page 152)
The Instruction Register holds the instruction that is being executed.

What do you understand by the machine exceptions?(2 Marks)
Answer:- Rep

Write the structural RTL for the mov immediate instruction for the mov immediate instruction for uni-bus data path implementation Movi ra,c2 (3marks)
Answer:- (Page 164)

Step	RTL
T0-T2	Instruction fetch
T3	C ← (8αc2<7>) © c2<7..0>;
T4	R[ra] ← C;

What is NOP instruction and its significance in pipelining? (3 Makrs)
Answer:- (Page 93)
This instruction is to instruct the processor to 'do nothing', or, in other words, do 'no operation'. This instruction is generally useful in pipelining. The NOP opcode causes a synchronization of the pipeline

Consider the following sequence of the instructions giving through the pipelined version of SRC
200:shl r6,r3,5
204:str r7,30
208:sub r2,r4,r5
2012:add r1,r2,r3
216:id r7,48
Answer:- (Page 216)
There is a data hazard between instruction three and four that can be resolved by using pipeline stalls or bubbles When using pipeline stalls, nop instructions are placed in between dependent instructions. The logic behind this scheme is that if opcode in stage 2 and 3 are both alu, and if ra in stage 3 is the same as rb or rc in stage 2, then a pause signal is issued to insert a bubble between stage 3 and 2. Similar logic is used for detecting hazards between stage 2 and 4 and stage 4 and 5.

6.Write the structure RTL description for the uni-bus data path implementation Jump[ra+2] (5 Marks)

ایماندار کو غصہ دیر سے آتا ہے اور جلدی دور ہو جاتا ہے

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i) difference between latency and throughput 2marks
Answer:- (Page 203)
Latency is defined as the time required processing a single instruction, while throughput is defined as the number of instructions processed per second.

ii) Which register holds the instruction that is being executed? 2marks IR(instruction register)
Answer:- Rep

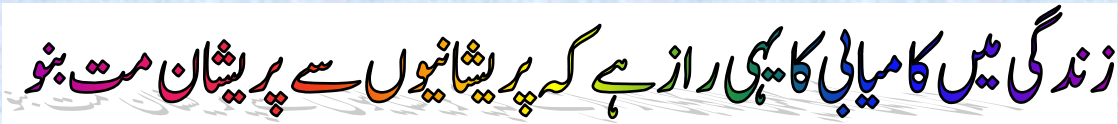
iii)structural RTL out ra,c2 3marks
Answer:- (Page 164)

Step	RTL
T0-T2	Instruction fetch
T3	C ← R[ra];
T4	IO[c2] ← C

iv) How compilers can detect and correct hazards? why is not preferable?3marks page 215
Answer:- (Page 215)
Data hazards can be detected easily as they occur when the destination register of an instruction is the same as the source register of another instruction in close proximity.
Hazards can be detected by the compiler, by analyzing the instruction sequences and dependencies. The compiler can inserts bubbles (nop instruction) between two instructions that form a hazard, or it could reorder instructions so as to put sufficient distance between dependent instructions. The compiler solution to hazards is complex, expensive and not very efficient as compared to the hardware solution.

v) 2ways to increase no. of instructions executed in giveb time? 5marks page 219
Answer:- Rep

vi) Structural RTL for shiftr ra,rb,c1? 5marks
Answer:- Rep



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MIDTERM EXAMINATION
Spring 2012
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Write down two processors name of superscalar architecture mark 2
Answer:- (Page 221)
o PowerPC 601
o Intel P6

How can you define microprogram?.....2 marks
Answer:- Rep

How exception may b generated write the difference between external and internal exceptions? 3 marks
Answer:- Rep

How many stages are in the pipelined version of SRC? Name them……..3 marks
Answer:- (Page 206)
five stages are given below:
1. Instruction Fetch
2. Instruction decode/operand fetch
3. ALU operation
4. Memory access
5. Register write

What are the pipeline problems? Describe each briefly…. 5marks
Answer:- (Page 214)
Classification of Hazards
There are three categories of hazards
1. Branch Hazard
2. Structural Hazard
3. Data Hazard

Branch hazards
The instruction following a branch is always executed whether or not the branch is taken. This is called the branch delay slot. The compiler might issue a nop instruction in the branch delay slot. Branch delays cannot be avoided by forwarding schemes.

Structural hazards
A structural hazard occurs when attempting to access the same resource in different ways at the same time. It occurs when the hardware is not enough to implement pipelining properly e.g. when the machine does not support separate data and instruction memories.

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Data hazards
Data hazard occur when an instruction attempts to access some data value that has not yet been updated by the previous instruction.

Write the structure RTL description for the uni-bus data path implementation Jump[ra+2] (5 Marks)

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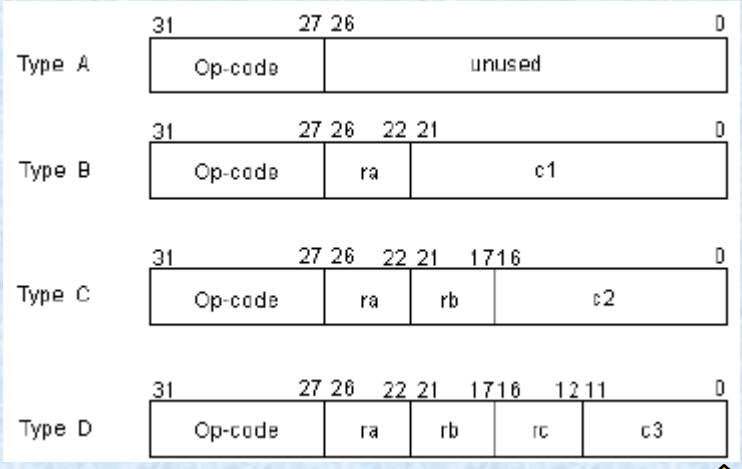
Write the Structural RTL for the 'not instruction' 2 marks
Answer:- (Page 154)

Step	RTL
T0-T2	Instruction fetch
T3	C ← !(R[rb]);
T4	R[ra] ← C;

How many types of instructions are available in SRC? Name them. What is the format of each of these instructions…….5marks
Answer:- (Page 47)
Four types of instructions are supported by the SRC. Their representation is given in the figure shown.



دنیا کی سب سے بڑی فتح نفس پر قابو رکھنا ہے

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Write the Structural RTL for the call instruction for uni-bus data path implementation.call ra, rb…5 marks
Answer:- Rep

Write the Structural RTL for the mov instruction for uni-bus data path implementation.mov ra, rb
Answer:- Rep

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Which register holds the address of the next instruction to b executed in the processor? 2 marks
Answer:- Rep
.
Write the main functions of the branch instruction? 2 marks
Answer:- not confirmed
calculate the target address to evolutes the condition

Write the structural RTL for the following instruction for the uni- bus path implementation in ra,rc ? 3 marks
Answer:- not confirmed

Steps	RTL
T0-T2	Instruction fetch
T3	C ← io[2]
T4	R[ra] ← C

How exception may b generated write the difference between external and internal exceptions? 3 marks
Answer:- Rep

Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly? 5 marks
Answer:- Rep

Write the structural RTL for the call instruction for the uni data path implementation?
Call ra, rab
Answer:- Rep

عقل مند کہتا ہے میں کچھ نہیں جانتا جبکہ بے وقوف کہتا ہے کہ میں سب کچھ جانتا ہوں

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MIDTERM EXAMINATION
Fall 2011
CS501- Advance Computer Architecture

1. What function is performed by the reset operation of a processor and differentiate Hard reset and Soft reset? [5 marks]

Answer:- (Page 194-195)

The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Hard Reset

The SRC should perform a hard reset upon receiving a start (Strt) signal. This initializes the PC and the general registers.

Soft Reset

The SRC should perform a soft reset upon receiving a reset (rst) signal. The soft reset results in initialization of PC only.

The reset signal in SRC is assumed to be external and asynchronous.

2. Write the Structural RTL for the mov instruction for uni-bus data path implementation.

mov ra, rb 3 marks

Answer:- Rep

3. Write the Structural RTL for shift right instruction. 2 marks

Answer:- (Page 185)

Step	RTL for shr
T0-T2	Instruction Fetch
T3	n<4..0> ← IR<4..0>;
T4	(N = 0) : (n<4..0> ← R[rc]<4..0>);
T5	C ← (Nα0) ©R[rb]<31..N>;
T6	R[ra] ← C;

جو لوگوں کے سامنے فخر کرتا ہے وہ لوگوں کی نظروں سے گر جاتا ہے

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4. What is the use of "NOP" instruction in pipe lining? 3 marks
Answer:- (Page 194-195)
Miscellaneous instructions
(op<4..0>= 0) , No operation (nop)
If the op-code is 0, no operation is carried out for that clock period. This instruction is used as a stall in pipelining.

MIDTERM EXAMINATION
Fall 2011
CS501- Advance Computer Architecture

Q1- What is Reset operation describe it types
Answer:- Rep

Q2- Describe super scaler and VILW.
Answer:- (Page 185)
Superscalar Architecture
A scalar processor that can issue multiple instructions simultaneously is said to be superscalar.

VLIW Architecture
A VLIW processor is based on a very long instruction word. VLIW relies on instruction scheduling by the compiler. The compiler forms instruction packets which can run in parallel without dependencies.

Q5-. Write the structural RTL for " in ra, rb"
Answer:- Rep

Write the Structural RTL description for un-conditional jump instruction for uni-bus data path implementation. (5 Marks)

بہترین تجربہ وہ ہے جس سے نصیحت حاصل ہو

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MIDTERM EXAMINATION
Fall 2011
CS501- Advance Computer Architecture

Define pre-fetching (2)
Answer:- Click here for detail
In computer architecture, instruction prefetch is a technique used in microprocessors to speed up the execution of a program by reducing wait states.

Describe three main functions of control unit. (3)
Answer:- Click here for detail
• It carries out many tasks such as decoding, fetching, handling the execution and finally storing the results.
• It interprets the instructions.
• It regulates the time controls of the processor

MIDTERM EXAMINATION
Fall 2011
CS501- Advance Computer Architecture

1. What is relation b/w data path and control unit in SRC processors…….2marks
Answer:- (Page 186)
By means of the control signals, the control unit instructs the data path what to do in every clock cycle during the execution of instructions.

2. Define Pre-fetching…….2marks
Answer:- Rep

3. Write the structural RTL for " in ra, rb" …….3marks
Answer:- Rep

4. What is difference between Latency and Throughput……3marks
Answer:- Rep

5. Write the Structural RTL for "call ra, rb"…….5marks
Answer:- Rep

جو شخص ناکامیوں سے ڈر کر بھاگتا ہے کامیابی اُس سے ڈر کر بھاگتی ہے

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MIDTERM EXAMINATION
Fall 2011
CS501- Advance Computer Architecture

Q no 1:-Define Control unit. (2 marks)
Answer:- (Page 186)
The control unit is responsible for generating control signals as well as the timing signals. Hence the control unit is responsible for the synchronization of internal as well as external events.

Q no 2:-How can you define Microprogram (2 marks)
Answer:- Rep

Q no 3:-Instruction fetch say tha yad nahin (3 marks)
rel Ra
Answer:- Rep

Q no 4:- what is the utility of reset operation when it is required (3 marks)
Answer:- (Page 194)
Reset operation is required to change the processor's state to a known, defined value. The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Q no5:- what are the types of SRC?Name them? also explain its format? (5 marks)
Answer:- Rep

MIDTERM EXAMINATION
Fall 2011
CS501- Advance Computer Architecture

Question No: 19 (Marks: 2)
How can you define microprogram?
Answer:- Rep

بدصورت چہرہ بدصورت دماغ سے بہتر ہے

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Question No: 20 (Marks: 3)
What is the role of timing step generator in a processor?
Answer:- (Page 152)
To ensure the correct and controlled execution of instructions in a program, and all the related operations, a timing device is required. This is to ensure that the operations of essentially different instructions do not mix up in time. There exists a 'timing step generator' that provides mutually exclusive and sequential timing intervals.

Question No: 21 (Marks: 3)
What is the utility of reset operation and when it is r
Answer:- Rep

Question No: 22 (Marks: 5)
Write the Structural RTL description for un-conditional jump uni-bus data path implementation. jump [ra+c2]

Question No: 23 (Marks: 5)
What function is performed by the reset operation of a processor? What are the two types of reset operations?
Answer:- Rep

MIDTERM EXAMINATION
Fall 2011
CS501- Advance Computer Architecture

Q : What information is provided by the addressing modes of some processors?
Answer:- (Page 39)
Addressing modes are the different ways in which the CPU generates the address of operands. In other words, they provide access paths to memory locations and CPU registers.

Q : how we speed-up a computer?
Answer:- (Page 232)
If a memory device is slow compared to the CPU, the CPU's speed can be made compatible by inserting wait states in the bus cycle.

خوبصورتی علم وادب سے ہوتی ہے لباس و حسن سے نہیں

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Control Unit Functionality mention only 3 (3 Marks)
Answer:- Rep

RTL Notation.
Answer:- (Page 66)
RTL stands for Register Transfer Language. The Register Transfer Language provides a formal way for the description of the behavior and structure of a computer. The RTL facilitates the design process of the computer as it provides a precise, mathematical representation of its functionality.

MIDTERM EXAMINATION
Spring 2010
CS501- Advance Computer Architecture (Session - 5)

Question No: 17 (Marks: 2)
Write the following statement of an Arithmetic Instruction using RTL.
If op-code is 0, the instruction is 'add'. The values in register rb and rc are added and the result is stored in register rc
Answer:- (Page 109)
(op<4..0>=0) : R[ra] ← R[rb] + R[rc],

Question No: 18 (Marks: 2)
Given below are the various fields of an SRC instruction register.
operation code field : **op<4..0>**
target register field : **ra<4..0>**
operand, address index, or branch target register : **rb<4..0>**
second operand, conditional test, or shift count register: **rc<4..0>**
Rewrite these various fields of an SRC instruction, using the **RTL.**
Answer:- (Page 67)
op<4..0>: = IR<31..27>; operation code field
ra<4..0>: = IR<26..22>; target register field
rb<4..0>: = IR<21..17>; operand, address index
rc<4..0>: = IR<16..12>; second operand, conditional test

Question No: 19 (Marks: 2)
How can you define microprogram?
Answer:- Rep

عقل مند آدمی اس وقت تک نہیں بولتا جب تک خاموشی نہیں ہو جاتی

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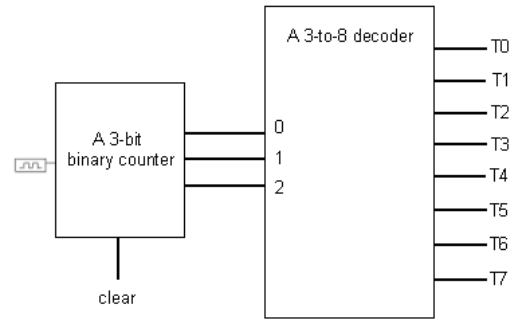
Question No: 20 (Marks: 3)
What is the role of timing step generator in a processor?



Answer:- Rep

Question No: 21 (Marks: 3)
What is the utility of reset operation and when it is required?
Answer:- Rep

Question No: 22 (Marks: 5)
Write the **Structural RTL description for un-conditional jump instruction for uni-bus data path implementation.**

jump [ra+c2]

Answer:- Rep

Question No: 23 (Marks: 5)
What function is performed by the reset operation of a processor? What are the two types of reset operations?
Answer:- Rep

تم اچھا کرو زمانہ تم کو برا سمجھے یہ اس سے بہتر ہے کہ تم برا کرو اور زمانہ تم کو اچھا سمجھے

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