

Question No : 1 of 26

Marks: 1 (Budgeted Time 1 Min)

Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?

Answer (Please select your correct option)

- Arithmetic
- Control
- Data transfer
- Floating point

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Question No : 2 of 26

Marks: 1 (Budgeted Time 1 Min)

What functionality is performed by the instruction "lar R3, 36" of SRC?

Answer (Please select your correct option)

- it will load the register R3 with the contents of the memory location M [PC+36]
- It will load the register R3 with the relative address itself (PC+36).
- It will store the register R3 contents to the memory location M [PC+36]
- No operation

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Question No : 3 of 26

Marks: 1 (Budgeted Time 1 Min)

What is the instruction length of the FALCON-A processor?

Answer (Please select your correct option)

- 8 bits
- 16 bits
- 32 bits
- 64 bits

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Question No : 4 of 26

Marks: 1 (Budgeted Time 1 Min)

What is the instruction length of the SRC processor?

Answer (Please select your correct option)

- 8 bits
- 16 bits
- 32 bits
- 64 bits

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Question No : 5 of 26

Marks: 1 (Budgeted Time 1 Min)

Type A format of SRC uses -----instructions

Answer (Please select your correct option)

- two
- three
- four
- five

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Question No : 6 of 26

Marks: 1 (Budgeted Time 1 Min)

P: $R3 \leftarrow R6$
MAR \leftarrow IR

These two are instructions written using RTL. If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

Answer (Please select your correct option)

- Arrow \leftarrow
- Colon $:$
- Comma $,$
- Parentheses $()$

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Question No : 7 of 26

Marks: 1 (Budgeted Time 1 Min)

Motorola MC68000 is an example of -----microprocessor.

Answer (Please select your correct option)

CISC



RISC

SRC

FALCON

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Question No : 8 of 26

Marks: 1 (Budgeted Time 1 Min)

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.

8-bits

24-bits

32-bits

64-bits



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Question No : 9 of 26

Marks: 1 (Budgeted Time 1 Min)

Which one of the following register holds the instruction that is being executed?

Accumulator

Address Mask

Instruction Register

Program Counter



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Question No : 10 of 26

Marks: 1 (Budgeted Time 1 Min)

Which one of the following design levels is called the gate level?

Logic Design Level



Circuit Level

Mask Level

Register transfer Level

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Question No : 11 of 26

Marks: 1 (Budgeted Time 1 Min)

Which one of the following is called 1-address machine?

Accumulator based machines



Stack based machines

General purpose register machines

CISC machines

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Question No : 12 of 26

Marks: 1 (Budgeted Time 1 Min)

For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory

Jump

Control

load/store



Arithmetic/Logic

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Question No : 13 of 26

Marks: 1 (Budgeted Time 1 Min)

_____ is/are defined as the number of instructions processed per second

Answer (Please select your correct option)

- Throughput
- Latency
- Hazards
- Throughput and Latency

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Question No : 14 of 26

Marks: 1 (Budgeted Time 1 Min)

The _____ instruction is completed once memory access has been made and the memory location has been written to.

- Store
- Branch
- Load
- Control

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Question No : 15 of 26

Marks: 1 (Budgeted Time 1 Min)

Type B format of SRC uses -----instructions

- Two
- Three
- Four
- Five

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Question No : 16 of 26

Marks: 1 (Budgeted Time 1 Min)

Anything that interrupts the normal flow of execution of instructions in the processor is called a/an

Answer (Please select your correct option)

Function

Exception

Assembler

Machine

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Question No : 17 of 26

Marks: 1 (Budgeted Time 1 Min)

PowerPC 601 is an example of

Answer (Please select your correct option)

FALCON-A

EAGLE

Superscalar processor

SRC

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Question No : 18 of 26

Marks: 1 (Budgeted Time 1 Min)

Which of the following register(s) takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system?

Answer (Please select your correct option)

Instruction Register

Memory address register

Memory Buffer Register

Registers A and C

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Question No : 19 of 26

Marks: 1 (Budgeted Time 1 Min)

For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required, which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

Answer (Please select your correct option)

DMA controllers

Memory

Control signals

Registers

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Question No : 20 of 26

Marks: 1 (Budgeted Time 1 Min)

Which of the following hazard occur when an instruction attempts to access some data value that has not yet been updated by the previous instruction?

Data hazard

Structural hazard

Branch hazard

Complex hazard

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Question No : 21 of 26

Marks: 2 (Budgeted Time 4 Min)

Differentiate between the superscalar architecture and VLIW architecture.

Answer (Please [click here](#) to Add Answer)

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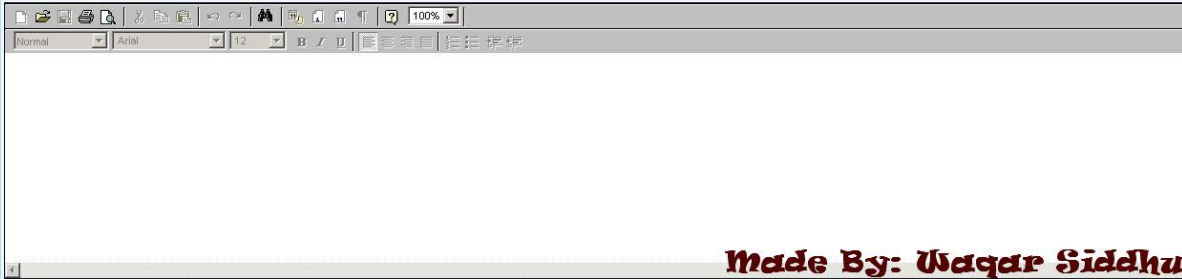
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Question No : 22 of 26

Marks: 2 (Budgeted Time 4 Min)

Which register stores a previously calculated value or a value loaded from the main memory?

Answer (Please [click here](#) to Add Answer)



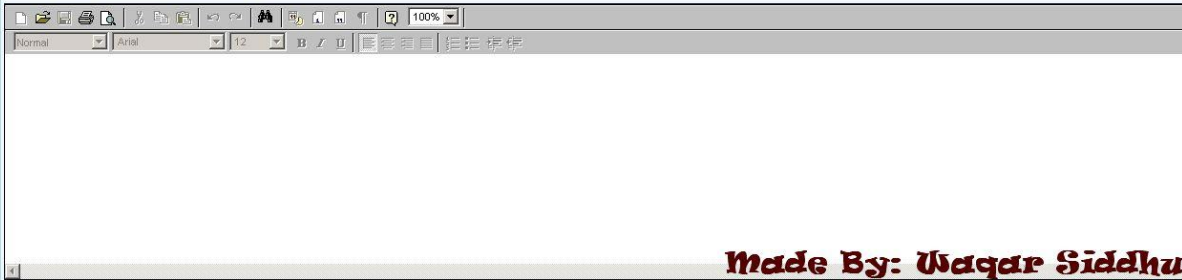
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Question No : 23 of 26

Marks: 3 (Budgeted Time 6 Min)

Write at least one advantage and one disadvantage of microprogramming.

Answer (Please [click here](#) to Add Answer)




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Question No : 24 of 26

Marks: 3 (Budgeted Time 6 Min)

What is the role of timing step generator in a processor?

Answer (Please [click here](#) to Add Answer)



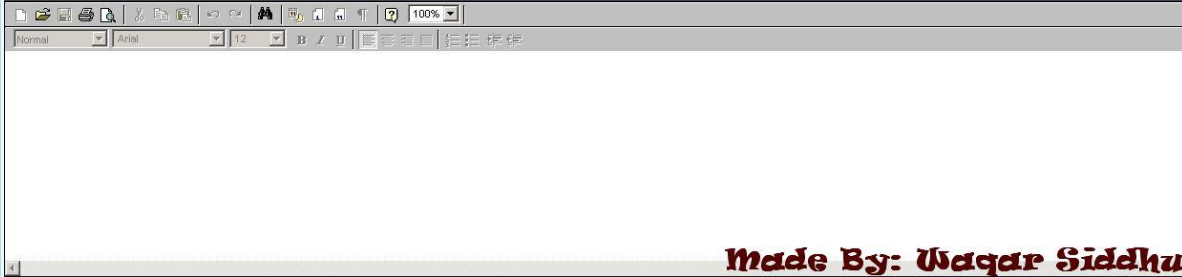
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Question No : 25 of 26

Marks: 5 (Budgeted Time 10 Min)

Write the related timing steps requirements and data path implementations of **Instruction Fetch** procedure using **structural RTL**.

Answer (Please [click here to Add Answer](#))



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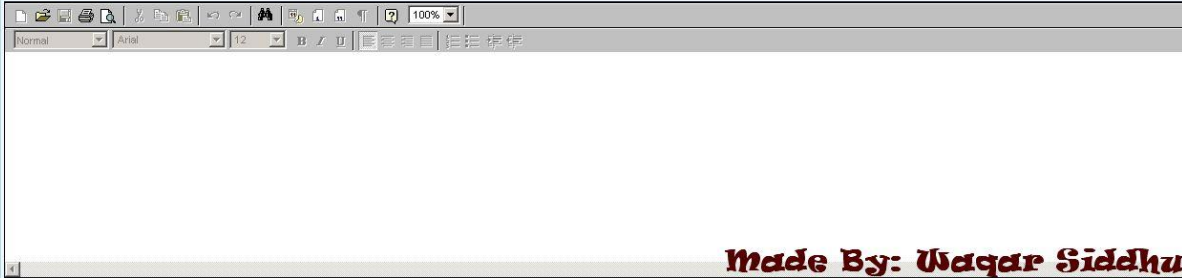
Question No : 26 of 26

Marks: 5 (Budgeted Time 10 Min)

Identify the hazard in the following sequence of instructions going through the pipelined version of SRC and explain how this hazard can be resolved?

```
200: str r3, 32
204: add r2, r4, r5
208: sub r1, r2, r3
212: ld r7, 48
```

Answer (Please [click here to Add Answer](#))



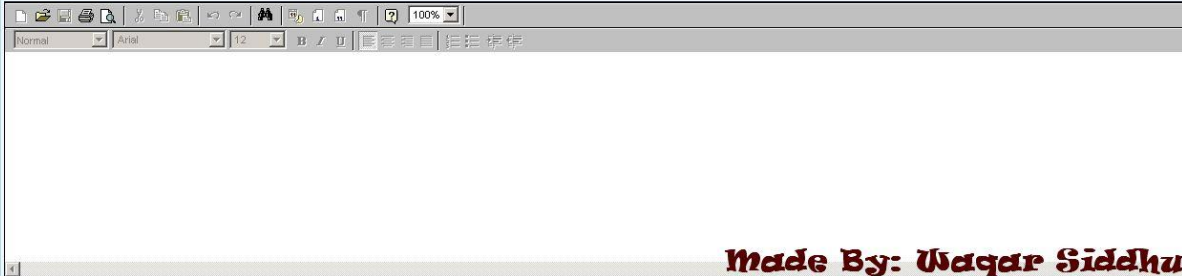
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Question No : 26 of 26

Marks: 5 (Budgeted Time 10 Min)

```
200: str r3, 32
204: add r2, r4, r5
208: sub r1, r2, r3
212: ld r7, 48
216: shl r6, r3, 5
```

Answer (Please [click here to Add Answer](#))



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