Question No : 1 of 26 Marks: 1 (Budgeted Time 1 Min)

What is the instruction length of the FALCON-A processor?

Answer (Please select your correct option)

- 8 bits
- 16 bits — correct
- 32 bits
- 64 bits

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Question No : 2 of 26 Marks: 1 (Budgeted Time 1 Min)

What is the instruction length of the SRC processor?

Answer (Please select your correct option)

- 8 bits
- 16 bits
- 32 bits — correct
- 64 bits

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Question No : 3 of 26 Marks: 1 (Budgeted Time 1 Min)

What does the word 'D' in the 'D-flip-Flop' stands for?

Answer (Please select your correct option)

- Double
- Data — correct
- Digital
- Dynamic

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Question No : 4 of 26 Marks: 1 (Budgeted Time 1 Min)

"If P = 1, then load the contents of register R1 into register R2".
This statement can be written in RTL as:

Answer (Please select your correct option)

- R1 ← R2
- P: R1 ← R2
- P: R2 ← R1

correct

- P: R2 ← R1, P: R1 ← R2

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Question No : 5 of 26 Marks: 1 (Budgeted Time 1 Min)

Almost every commercial computer has its own particular ---------- language

Answer (Please select your correct option)

- assembly language

correct

- English language
- Higher level language
- 3GL

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Question No : 6 of 26 Marks: 1 (Budgeted Time 1 Min)

A ---------- is a computer program that is used to test and debug other programs.

Answer (Please select your correct option)

- Linker
- Loader
- Debugger
- Compiler

correct

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Question No : 7 of 26 Marks: 1 (Budgeted Time 1 Min)

What is the working of **Processor Status Word** (PSW)?

Answer (Please select your correct option)

- To hold the current status of the processor. correct
- To hold the address of the current process
- To hold the instruction that the computer is currently processing
- To hold the address of the next instruction in memory that is to be executed

Question No : 8 of 26 Marks: 1 (Budgeted Time 1 Min)

The instruction ----------will **load** the register R3 with the contents of the memory location M [PC+56]

Answer (Please select your correct option)

- Add R3, 56
- lar R3, 56
- ldr R3, 56 correct
- str R3, 56

Question No : 9 of 26 Marks: 1 (Budgeted Time 1 Min)

Motorola MC68000 is an example of ---------microprocessor.

Answer (Please select your correct option)

- CISC correct
- RISC
- SRC
- FALCON

Question No : 10 of 26 Marks: 1 (Budgeted Time 1 Min)

_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

Answer (Please select your correct option)

- INC4
- LPC
- PCout

correct

- LC

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Question No : 11 of 26 Marks: 1 (Budgeted Time 1 Min)

op<4..0>:= IR<15..11>:
The above RTL instruction presents the _____ of the FALCON-A Instructions.

op<4..0>:= IR<15..11>: operation code field
ra<2..0> := IR<10..8>: target register field
rb<2..0> := IR<7..5>: operand or address index
rc<2..0> := IR<4..2>: second operand
c1<4..0> := IR<4..0>: short displacement field
c2<7..0> := IR<7..0>: long displacement or the immedia

Answer (Please select your correct option)

- operation code field

correct

- target register field
- operand or address index
- second operand

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Question No : 12 of 26 Marks: 1 (Budgeted Time 1 Min)

_____ operation is required to change the processor's state to a known, defined value.

reset(op-code=248)
This instruction is used to initialize the processor to a known state

Answer (Please select your correct option)

- Change
- Reset

correct

- Update
- Halt

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Question No : 13 of 26 Marks: 1 (Budgeted Time 1 Min)

_____ is/are defined as the number of instructions processed per second

Latency is defined as the time required to process a single instruction, while throughput is defined as the number of instructions processed per second.

Answer (Please select your correct option)

- Throughput — correct
- Latency
- Hazards
- Throughput and Latency

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Question No : 14 of 26 Marks: 1 (Budgeted Time 1 Min)

Which of the following register(s) is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

The registers A and C are required to hold an operand or result value while the bus is busy transmitting some other value. Both these registers are programmer invisible.

Answer (Please select your correct option)

- Instruction Register
- Memory address register
- Memory Buffer Register
- Registers A and C — correct

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Question No : 15 of 26 Marks: 1 (Budgeted Time 1 Min)

Anything that interrupts the normal flow of execution of instructions in the processor is called a/an ----------

Anything that interrupts the normal flow of execution of instructions in the processor is called an exception.

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Answer (Please select your correct option)

- Function
- Exception — correct
- Assembler
- Machine

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Question No : 16 of 26 Marks: 1 (Budgeted Time 1 Min)

In pipelining ---------- is increased by overlapping the instruction execution

Throughput increased by overlapping the instruction execution

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Answer (Please select your correct option)

- Latency
- Throughput

correct

- Execution time
- Clock speed

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Question No : 17 of 26 Marks: 1 (Budgeted Time 1 Min)

_____ control signal enable the input to the PC for receiving a value that is currently on the internal processor bus.

LPC: This will enable the input to the PC for receiving a value that is currently on the internal processor bus. Thus the PC will receive an incremented value.

Answer (Please select your correct option)

- LPC

correct

- INC4
- LC
- Cout

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Question No : 18 of 26 Marks: 1 (Budgeted Time 1 Min)

In which one of the following addressing modes, data is the part of the instruction itself, and so there is no need of address calculation?

Immediate addressing mode
In this addressing mode, data is the part of the instruction itself, and so there is no need of address calculation.

Answer (Please select your correct option)

- Direct Addressing Mode
- Immediate addressing mode

correct

- Indirect Addressing Mode
- Register (Direct) Addressing Mode

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Question No : 19 of 26 Marks: 1 (Budgeted Time 1 Min)

Which of the following hazard occurs when attempting to access the same resource in different ways at the same time?

Structural hazards
A structural hazard occurs when attempting to access the same resource in different ways at the same time. 231

Answer (Please select your correct option)

- RAW (read after write) data hazard
- Structural hazard — correct
- Branch hazard
- Complex hazard

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Question No : 20 of 26 Marks: 1 (Budgeted Time 1 Min)

---------- is the arithmetic portion of the Von Neumann architecture. It consists of registers, internal buses, arithmetic units and shifters.

The data path is the arithmetic portion of the Von Neumann architecture. It consists of registers, internal buses, arithmetic units and shifters. 154

Answer (Please select your correct option)

- Virtual Memory
- Data path — correct
- Structural RTL
- Timing

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Question No : 21 of 26 Marks: 2 (Budgeted Time 4 Min)

Compare the uni-bus implementation of FALCON-A with that of SRC with respect to size (Number of bits) of each register

Answer (Please click here to Add Answer)

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Question No : 22 of 26 Marks: 2 (Budgeted Time 4 Min)

Differentiate between hard reset and soft reset?

Answer (Please click here to Add Answer)

Soft reset implies initializing PC and interrupt flags. Hard reset initializes other processor state registers in addition to PC and interrupts enable flags. The software reset instruction asserts the external reset pin of the processor.

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Question No : 23 of 26 Marks: 3 (Budgeted Time 6 Min)

Write at least one advantage and one disadvantage of microprogramming.

Answer (Please click here to Add Answer)

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Question No : 24 of 26 Marks: 3 (Budgeted Time 6 Min)

Write the Structural RTL for the "out" instruction i.e. **out ra, c2.**

Answer (Please click here to Add Answer)

This Instruction is opposite to the „In" Instruction. First three instructions would fetch the instruction. In step T3 the contents of register ra are placed in to the buffer register C and then in Step T4 from C the data is placed at the output port indicated by the c2 constant. So this instruction is just opposite to the „In" instruction.

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Question No : 25 of 26 Marks: 5 (Budgeted Time 10 Min)

Write the related timing steps requirements and data path implementations of **Instruction Fetch** procedure using **structural RTL**

Answer (Please click here to Add Answer)

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Question No : 26 of 26 Marks: 5 (Budgeted Time 10 Min)

What are three main problems related to pipelining? Describe any two of them.

Answer (Please click here to Add Answer)

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