Quiz cs501 # 1 solved

Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register **B)** from the following example. ADD R1, R2, R3
Select correct option:

Opcode= R1, DR=ADD, SA=R2, SB=R3
Opcode= ADD, DR=R1, SA=R2, SB=R3
Opcode= R2, DR=ADD, SA=R1, SB=R3
Opcode= ADD, DR=R3, SA=R2, SB=R1
Which type of instructions help in changing the flow of the program as and when required?
Select correct option:

Arithmetic
Control
Data transfer
Floating point

Almost every commercial computer has its own particular ---------- language
Select correct option:

3GL
English language
Higher level language
assembly language
Which one of the following is a binary cell capable of storing one bit of information?
Select correct option:

Decoder
Flip-flop
Multiplexer
Diplexer
Which statement(s)from the following is/are correct about Reduced Instruction Set Computer (RISC) architectures.
(i) The typical RISC machine instruction set is small, and is usually a subject of a CISC instruction set.
(ii) (ii) No arithmetic or logical instruction can refer to the memory directly.
(iii) (iii) A comparatively large number of user registers are available.
(iv) (iv) Instructions can be easily decoded through hard-wired control units.
Select correct option:

(i) and (iii) only
(i), (iii) and (iv)
(i), (ii) and (iii) only
(i),(ii),(iii) and (iv)

What is the instruction length of the FALCON-E processor?
Select correct option:

8 bits

16 bits
32 bits
64 bits

Which one of the following are the code size and the Number of memory bytes respectively for a 3-address instruction?
Select correct option:

0 bytes, 10 bytes
4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?

Select correct option:

Jump and branch format instructions
Immediate format instructions
Register format instructions
All of the above

Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
Select correct option:

4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes
13 bytes, 22 bytes

Nadia: P: R3 <- R5 MAR <- IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
Select correct option:

Parentheses ()
Arrow <-
Colon :
Comma ,

In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:

Arithmetic/logic
Load/store
Test/branch
None of the given

In which one of the following addressing modes, the operand does not specify an address but it is the actual

data to be used.
Select correct option:

Direct
Indirect
Immediate
Relative

Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:

Address
Instruction code
Opcode
Operand

MC090405648 : Shabana Iqbal

Time Left 76 sec(s)

Quiz Start Time: 07:19 PM

Question # 2 of 10 (Start time: 07:19:55 PM) **Total Marks:** 1

Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?

Select correct option:

:=

&

%

©

Click here to Save Answer & Move to Next Question

MC090405648 : Shabana Iqbal

Time Left 87 sec(s)

Quiz Start Time: 07:19 PM

Question # 3 of 10 (Start time: 07:21:14 PM) **Total Marks:** 1

The data movement instructions ___________ data within the machine and to or from input/output devices.

Select correct option:

- Store
- Load
- Move
- None of given

Click here to Save Answer & Move to Next Question

MC090405648 : Shabana Iqbal

Time Left 86 sec(s)

Quiz Start Time: 07:19 PM

Question # 4 of 10 (Start time: 07:22:15 PM) **Total Marks:** 1

Which one of the following is the memory organization of EAGLE processor?

Select correct option:

- 2^8 * 8 bits
- 2^16 * 8 bits

- 2^32 * 8 bits
- 2^64 * 8 bits

Click here to Save Answer & Move to Next Question

MC090405648 : Shabana Iqbal

Time Left 87 sec(s)

Quiz Start Time: 07:19 PM

Question # 5 of 10 (Start time: 07:23:33 PM) **Total Marks:** 1

Which field of the machine language instruction is the "type of operation" that is to be performed?

Select correct option:

- Op-code (or the operation code)
- CPU registers
- Memory cells
- I/O locations

Click here to Save Answer & Move to Next Question

MC090405648 : Shabana Iqbal

Time Left 87 sec(s)

Quiz Start Time: 07:19 PM

Question # 6 of 10 (Start time: 07:24:42 PM) **Total Marks:** 1

Which one of the following circuit design levels is called the gate level?

Select correct option:

- Logic Design Level
- Circuit Level
- Mask Level
- None of the given

Click here to Save Answer & Move to Next Question

MC090405648 : Shabana Iqbal

Time Left 85 sec(s)

Quiz Start Time: 07:19 PM

Question # 7 of 10 (Start time: 07:26:07 PM) **Total Marks:** 1

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

Select correct option:

- Processor-Memory-Switch level (PMS level)
- Instruction Set Level
- Register Transfer Level
- None of the given

Click here to Save Answer & Move to Next Question

MC090405648 : Shabana Iqbal

Time Left 79 sec(s)

Quiz Start Time: 07:19 PM

Question # 8 of 10 (Start time: 07:27:23 PM) **Total Marks:** 1

What functionality is performed by the instruction "lar R3, 36" of SRC?

Select correct option:

- It will load the register R3 with the contents of the m
- It will load the register R3 with the relative address i
- It will store the register R3 contents to the memory l
- No operation

Click here to Save Answer & Move to Next Question

MC090405648 : Shabana Iqbal

Time Left 87 sec(s)

Quiz Start Time: 07:19 PM

Question # 9 of 10 (Start time: 07:28:47 PM) **Total Marks:** 1

What is the working of Processor Status Word (PSW)?

Select correct option:

- To hold the current status of the processor.

- To hold the address of the current process
- To hold the instruction that the computer is currently
- To hold the address of the next instruction in memor

Click here to Save Answer & Move to Next Question

MC090405648 : Shabana Iqbal

Time Left 88 sec(s)

Quiz Start Time: 07:19 PM

Question # 10 of 10 (Start time: 07:30:15 PM) **Total Marks:** 1

Which one of the following portions of an instruction represents the operation to be performed?

Select correct option:

- Address
- Instruction code
- Opcode
- Operand

Click here to Save Answer & Move to Next Question

Question # 1 of 10 (Start time: 03:54:37 PM) **Total Marks:** 1

In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?

Select correct option:

Direct Addressing Mode

Immediate addressing mode

OK Indirect Addressing Mode

Register (Direct) Addressing Mode

Question # 2 of 10 (Start time: 03:55:27 PM) **Total Marks:** 1

Almost every commercial computer has its own particular ---------- language

Select correct option:

3GL

English language

Higher level language

assembly language

Question # 3 of 10 (Start time: 03:55:56 PM) **Total Marks:** 1

Which one of the following is/are the features of Register Transfer Language?
a) It is a symbolic language
b) It is describing the internal organization of digital computers
c) It is an elementary operation performed (during one clock pulse), on the information stored in one or more registers

d) It is high level language

Select correct option:

(b) only

OK (a) & (b) only

(a) ,(b) & (d)

(b),(c) & (d)

Question # 4 of 10 (Start time: 03:56:54 PM) **Total Marks:** 1

Which of the instruction is used to load register from memory using a relative address?

Select correct option:

ld instruction

ldr instruction

lar instruction

str instruction

Question # 5 of 10 (Start time: 03:57:31 PM) **Total Marks:** 1

Which one of the following circuit design levels is called the gate level?

Select correct option:

- (selected) Logic Design Level
- Circuit Level
- Mask Level
- None of the given

Question # 6 of 10 (Start time: 03:57:53 PM) **Total Marks:** 1

What functionality is performed by the instruction "str R8, 34" of SRC?

Select correct option:

- It will load the register R8 with the contents of the memory location M [PC+34]
- It will load the register R8 with the relative address itself (PC+34).
- (selected) It will store the register R8 contents to the memory location M [PC+34]
- No operation

Question # 7 of 10 (Start time: 03:58:42 PM) **Total Marks:** 1

All processors need to support at least __________ categories (or functional groups) of instructions.

Select correct option:

- ○ Two
- ● Three
- ○ Four
- ○ Five

Question # 9 of 10 (Start time: 04:00:57 PM) **Total Marks:** 1

Which field of the machine language instruction is the "type of operation" that is to be performed?

Select correct option:

- ● Op-code (or the operation code)
- ○ CPU registers
- ○ Memory cells
- ○ I/O locations

Total Marks: 1

Question # 10 of 10 (Start time: 04:01:53 PM)

Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?

Select correct option:

OK

- (selected) Base address
- Binary address
- Effective address
- All of the given

Question # 1 of 10 (Start time: 07:17:21 PM) **Total Marks:** 1

The instruction --------------will load the register R3 with the contents of the memory location M [PC+56]

Select correct option:

- Add R3, 56
- lar R3, 56
- (selected) ldr R3, 56
- str R3, 56

Total Marks: 1

Question # 2 of 10 (Start time: 07:18:35 PM)

In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also

called data movement?

Select correct option:

- Arithmetic/logic
- Load/store
- Test/branch
- None of the given

Question # 3 of 10 (Start time: 07:20:04 PM) **Total Marks:** 1

Which type of instructions help in changing the flow of the program as and when required?

Select correct option:

- Arithmetic
- Control
- Data transfer
- Floating point

Total Marks: 1

Question # 4 of 10 (Start time: 07:21:00 PM)

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?

Select correct option:

- Jump and branch format instructions
- Immediate format instructions

Not sure

- Register format instructions
- All of the above

Question # 5 of 10 (**Start time: 07:22:23 PM** **)** **Total Marks:** 1

Which operator is used to ‘name’ registers, or part of registers, in the Register Transfer Language?

Select correct option:

OK

- :=
- &
- %
- ©

Total Marks: 1

Page 22 is important

Question # 6 of 10 (**Start time: 07:22:41 PM** **)**

Which one of the following is a bi-stable device, capable of storing one bit of Information?

Select correct option:

Decoder

OK Flip-flop

Multiplexer

Diplexer

Question # 7 of 10 (**Start time: 07:23:00 PM** **)** **Total Marks:** 1

Which type of instructions enables mathematical computations?

Select correct option:

OK Arithmetic

Control

Data transfer

Floating point

Total Marks: 1

Question # 8 of 10 (**Start time: 07:23:30 PM** **)**

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

Select correct option:

- (selected) Processor-Memory-Switch level (PMS level)
- Instruction Set Level
- Register Transfer Level
- None of the given

Question # 9 of 10 (Start time: 07:24:55 PM) **Total Marks:** 1

Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?

Select correct option:

- Arithmetic
- Control
- (selected) Data transfer
- Floating point

Total Marks: 1

Question # 10 of 10 (Start time: 07:25:56 PM)

Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3

Select correct option:

Opcode= R1, DR=ADD, SA=R2, SB=R3

OK Opcode= ADD, DR=R1, SA=R2, SB=R3

Opcode= R2, DR=ADD, SA=R1, SB=R3

Opcode= ADD, DR=R3, SA=R2, SB=R1

Question # 5 of 10 (Start time: 07:29:51 PM) **Total Marks:** 1

Which one of the following languages presents a simple, human-oriented language to specify the operations, register communication and timing of the steps that take place within a CPU to carry out higher level (user programmable) instructions?

Select correct option:

Assembly Language

OOP(Object Oriented Language)

RTL (Register Transfer Language)

UML(Unified Modeling language)

Total Marks: 1

Question # 6 of 10 (Start time: 07:30:41 PM)

An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------------

Select correct option:

- compiler
- cross assembler
- debugger
- linker

Question # 7 of 10 (Start time: 07:31:53 PM) **Total Marks:** 1

In-------------address mode, the actual data is stored in the instruction.

Select correct option:

- Direct
- Indirect
- Immediate
- Relative

Question # 8 of 10 (Start time: 07:33:12 PM) **Total Marks:** 1

What is the instruction length of the FALCON-A processor?

Select correct option:

- 8 bits
- 16 bits
- 32 bits
-

Question # 9 of 10 (Start time: 07:34:50 PM) **Total Marks:** 1

What does the instruction “ldr R3, 58” of SRC do?

Select correct option:

- It will load the register R3 with the contents of the m
- It will load the register R3 with the relative address i
- It will store the register R3 contents to the memory l
- No operation

Question # 1 of 10 (Start time: 07:37:42 PM) **Total Marks:** 1

Which one of the following is the memory organization of EAGLE processor?

Select correct option:

- 2^8 * 8 bits

- (selected) 2^16 * 8 bits
- 2^32 * 8 bits
- 2^64 * 8 bits

Question # 2 of 10 (Start time: 07:38:34 PM) **Total Marks:** 1

How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?

Select correct option:

- IR<16..0>
- (selected) IR<15..0>
- IR<16..1>
- IR<15..1>

Question # 3 of 10 (Start time: 07:39:50 PM) **Total Marks:** 1

Whic of the following statements is/are true about RISC processors' claimed advantages over CISC processors? (a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution. (b) RISC CPUs outperform CISC CPU's in procedural programming environments. (c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction. (d) It is easier to maintain the "family concept" in RISC CPUs.

Select correct option:

- (selected) (a), (b) &(c)

- (b), (c) & (e)
- (c), (d) & (e)
- (a), (c) & (d)

Question # 4 of 10 (Start time: 07:40:31 PM) **Total Marks:** 1

What functionality is performed by the instruction "lar R3, 36" of SRC?

Select correct option:

- It will load the register R3 with the contents of the m
- It will load the register R3 with the relative address i
- It will store the register R3 contents to the memory l
- No operation

Question # 6 of 10 (Start time: 07:42:00 PM) **Total Marks:** 1

Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction

Select correct option:

- (a)& (b)

(b)&(c)

(a)&(e)

(b)&(e)

Question # 8 of 10 (Start time: 07:44:17 PM) **Total Marks:** 1

Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?

Select correct option:

Base address

Binary address

Effective address

All of the given

Question # 9 of 10 (Start time: 07:45:39 PM) **Total Marks:** 1

Which notation do we use to name different fields of a register in RTL?

Select correct option:

()

<-

+

:=

Question # 1 of 10 (Start time: 04:33:46 PM) **Total Marks:** 1

Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

Select correct option:

Instruction Register

Memory address register

Memory Buffer Register

OK Registers A and C

FALCON-A consists of

Question # 3 of 10 (Start time: 04:36:52 PM) **Total Marks:** 1

The external interface of FALCON-A consists of a ___________ address bus.

Select correct option:

8-bit

- 16-bit
- 24-bit
- 32-bit

Question # 4 of 10 (**Start time: 04:38:35 PM** **)** **Total Marks:** 1

The external interface of FALCON-A consists of a ________ data bus.

Select correct option:

- 8-bit
- (selected) 16-bit
- 24-bit
- 32-bit

Question # 5 of 10 (**Start time: 04:40:08 PM** **)** **Total Marks:** 1

Which one of the following registers holds the instruction that is being executed?

Select correct option:

- Accumulator
- Address Mask

- [x] Instruction Register
- [ ] Program Counter

Question # 6 of 10 (Start time: 04:40:46 PM) **Total Marks:** 1

__________ enable the input to the PC for receiving a value that is currently on the internal processor bus.

Select correct option:

- [x] LPC
- [ ] INC4
- [ ] LC
- [ ] Cout

Question # 8 of 10 (Start time: 04:43:14 PM) **Total Marks:** 1

The processor must have a way of saving information about its state or context so that it can be restored upon return from the -------------

Select correct option:

- [ ] Exception
- [ ] Function

- Thread
- Stack

The processor must have a way of saving information about its state or context so that it can be restored upon return from the -------------

Select correct option:

- Exception
- Function
- Thread
- Stack

Saving... Click here to Save Answer & Move to Next Question

Question # 9 of 10 (Start time: 04:44:51 PM) **Total Marks:** 1

Which one of the following registers holds the address of the next instruction to be executed?

Select correct option:

- Accumulator
- Address Mask

Instruction Register

Program Counter

Question # 10 of 10 (Start time: 04:45:46 PM) **Total Marks:** 1

Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?

Select correct option:

Instruction Register

Memory address register

Memory Buffer Register

Registers A and C

Question # 1 of 10 (Start time: 04:53:38 PM) **Total Marks:** 1

Motorola MC68000 is an example of ---------microprocessor.

Select correct option:

CISC

RISC

- SRC
- FALCON

Question # 3 of 10 (Start time: 04:54:51 PM) **Total Marks:** 1

The external interface of FALCON-A consists of a __________address bus and a _________ data bus.

Select correct option:

- 8-bit , 8-bit
- 16-bit , 16-bit
- 16-bit , 24-bit
- 16-bit , 32-bit

Question # 5 of 10 (Start time: 04:56:45 PM) **Total Marks:** 1

_________ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

Select correct option:

- INC4
- LPC

- [x] PCout
- [ ] LC

Question # 6 of 10 (Start time: 04:57:24 PM) **Total Marks:** 1

Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

Select correct option:

- [ ] Instruction Register
- [ ] Memory address register
- [ ] Memory Buffer Register
- [x] Registers A and C

Question # 9 of 10 (Start time: 05:00:52 PM) **Total Marks:** 1

In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?

Select correct option:

- [ ] Perfecting
- [ ] Pipelining

Superscalar operation

Speedup

Question # 1 of 10 (Start time: 07:39:47 PM) **Total Marks:** 1

_________ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

Select correct option:

INC4

LPC

PCout

LC

Which one of the following registers stores a previously calculated value or a value loaded from the main memory?

Select correct option:

Accumulator

Address Mask

Instruction Register

Question # 9 of 10 (Start time: 07:45:04 PM) **Total Marks:** 1

Computer system performance is usually measured by the --------------

Select correct option:

- Time to execute a program or program mix
- The speed with which it executes programs
- Processor's utilization in solving the problems
- Instructions that can be carried out simultaneously

Question # 10 of 10 (Start time: 07:46:38 PM) **Total Marks:** 1

For any of the instructions that are a part of the instruction set of the SRC, there are certain ____________ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

Select correct option:

- Registers
- Control signals
- Memory
- None of the given

MIDTERM EXAMINATION
Spring 2010
CS501- Advance Computer Architecture (Session - 5)

Time: 60 min
Marks: 38

Question No: 1 (Marks: 1) - Please choose one

What is the instruction length of the SRC processor?

► 8 bits

► 16 bits

► **32 bits**

► 64 bits

Question No: 2 (Marks: 1) - Please choose one

Which one of the following is the memory organization of **FALCON-E processor?**

► 2^8 * 8 bits

► 2^{16} * 8 bits

► **2^{32} * 8 bits**

► 2^{64} * 8 bits

Question No: 3 (Marks: 1) - Please choose one

"If P = 1, then load the contents of register R1 into register R2".
This statement can be written in RTL as:

► R1 ¬ R2
► P: R1 ¬ R2
► P: R2 ¬ R1
► P: R2 ¬ R1, P: R1 ¬ R2

Question No: 4 (Marks: 1) - Please choose one

The instruction ---------------will **load** the register R3 with the contents of the memory location M [PC+56] http://vustudents.ning.com

- ▶ Add R3, 56
- ▶ lar R3, 56
- ▶ **ldr R3, 56**
- ▶ str R3, 56

Question No: 5 (Marks: 1) - Please choose one

----------are faster than cache memory

≡ **Accumulator register**

≡ CPU registers

≡ I/O devices

≡ ROM

Question No: 6 (Marks: 1) - Please choose one

P: R3 ¬ R5: MAR ¬ IR

These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

▶ Arrow ¬

▶ Colon :

▶ **Comma ,**

▶ Parentheses ()

Question No: 7 (Marks: 1) - Please choose one

Prefetching can be considered a primitive form of-------------

- ▶ **Pipelining**
- ▶ Multi-processing
- ▶ Self-execution
- ▶ Exception

Question No: 8 (Marks: 1) - Please choose one

The processor must have a way of saving information about its state or context so that it can be restored upon return from the -------------

- ▶ **Exception**
- ▶ Function
- ▶ Stack
- ▶ Thread

Question No: 9 (Marks: 1) - Please choose one

Which one of the following circuit design levels is called the gate level?

- **Logic Design Level**
- Circuit Level
- Mask Level
- None of the given

Question No: 10 (Marks: 1) - Please choose one

__________ enable the input to the PC for receiving a value that is currently on the internal processor bus.

- ▶ **LPC**
- ▶ INC4
- ▶ LC
- ▶ Cout

Question No: 11 (Marks: 1) - Please choose one

________ Operation is required to change the processor's state to a known, defined value.

- ▶ Change
- ▶ **Reset**
- ▶ Update
- ▶ None of the given

Question No: 12 (Marks: 1) - Please choose one

There are _________ types of reset operations in SRC

- ▶ **Two**
- ▶ Three
- ▶ Four
- ▶ Five

Question No: 13 (Marks: 1) - Please choose one

______________ Controller controls the sequence of the flow of microinstructions.

- ► Multiplexer
- ► **Microprogram**
- ► ALU
- ► None of the given

Question No: 14 (Marks: 1) - Please choose one

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is __________ wide.

- ► 8-bits
- ► 24-bits
- ► **32-bits**
- ► 64-bits

Question No: 15 (Marks: 1) - Please choose one

Which of the following statement(s) is/are correct about Reduced Instruction Set Computer (RISC) architectures.

(i) The typical RISC machine instruction set is small, and is usually a subject of a CISC instruction set.
(ii) No arithmetic or logical instruction can refer to the memory directly.
(iii) A comparatively large number of user registers are available.
(iv) Instructions can be easily decoded through hard-wired control units.

- ► (i) and (iii) only
- ► (i), (iii) and (iv)
- ► (i), (ii) and (iii) only
- ► (i),(ii),(iii) and (iv)

Question No: 16 (Marks: 1) - Please choose one

Which one of the following register holds the instruction that is being executed?

- ► Accumulator
- ► Address Mask
- ► **Instruction Register**
- ► Program Counter

Question No: 17 (Marks: 2)

Write the following statement of an Arithmetic Instruction using RTL.

If op-code is 0, the instruction is 'add'. The values in register rb and rc are added and the result is stored in register rc

(Page No. 109)

ANS: **(op<4..0>=0): R[ra] ← R[rb] + R[rc],**

Question No: 18 (Marks: 2)

Given below are the various fields of an SRC instruction register.

a) operation code field : **op<4..0>**
b) target register field : **ra<4..0>**
c) operand, address index, or branch target register : **rb<4..0>**
d) second operand, conditional test, or shift count register: **rc<4..0>**

Rewrite these various fields of an SRC instruction, using the **RTL.**

Question No: 19 (Marks: 2)

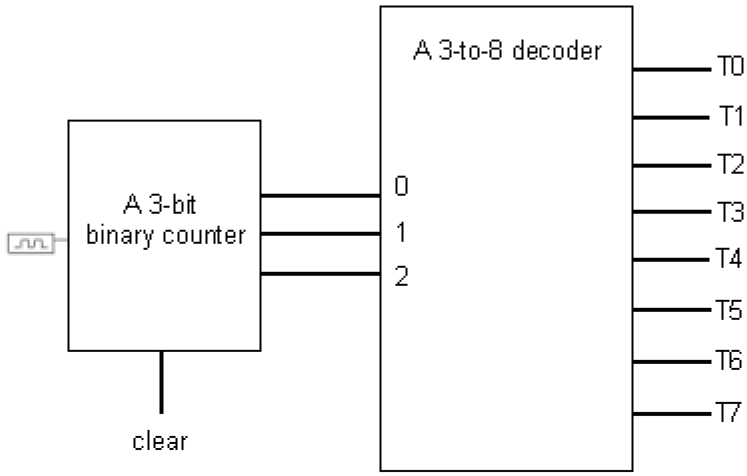
How can you define microprogram?

ANS: In a micro programmed control unit, control signals which need to be generated at a certain time are stored together in a control word. This control word is called a microinstruction. A collection of microinstructions is called a microprogram.

Question No: 20 (Marks: 3)

What is the role of timing step generator in a processor?

ANS: To ensure the correct and controlled execution of instructions in a program, and all the related operations, a timing device is required. This is to ensure that the operations of essentially different instructions do not mix up in time. There exists a 'timing step generator' that provides mutually exclusive and sequential timing intervals. This is analogous to the clock cycles in the actual processor. A possible implementation of the timing step generator is shown in the figure. Each mutually exclusive step is carried out in one timing interval. The timing intervals can be named T0, T1…T7. The given figure is helpful in understanding the 'mutual exclusiveness in time' of these timing intervals.



Question No: 21 (Marks: 3)

What is the utility of reset operation and when it is required?

ANS: Reset operation is required to change the processor' s state to a known, defined value. The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Question No: 22 (Marks: 5)

Write the **Structural RTL description for un-conditional jump instruction for uni-bus data path implementation.**

Jump [ra+c2]

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Question No: 23 (Marks: 5)

What function is performed by the reset operation of a processor? What are the two types of reset operations?

ANS: Reset operation is required to change the processor' s state to a known, defined value. The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Two Types of Reset Operations:

Hard Reset

The SRC should perform a hard reset upon receiving a start (Strt) signal. This initializes
the PC and the general registers.

Soft Reset

The SRC should perform a soft reset upon receiving a reset (rst) signal. The soft reset
results in initialization of PC only.

2^{nd} paper

There were 23 questions 1-14 are mcqs others are questions

Q : DEFINE HARD RESET AND SOFT RESET OPERATIONS IN SRC

ANS: **Hard Reset**

The SRC should perform a hard reset upon receiving a start (Strt) signal. This initializes
the PC and the general registers.

Soft Reset

The SRC should perform a soft reset upon receiving a reset (rst) signal. The soft reset
results in initialization of PC only.

Q : Write two pipelining problem and define them briefly.

Ans: 1. **Branch delay**

Branches can cause problems for pipelined processors. It is difficult to predict whether a branch will be taken or not before the branch condition is tested.

2. **Load delay**

Another problem surfaces when a value is loaded into a register and then immediately used in the next operation.

Q: What information is provided by the addressing modes of some processors?

Ans: 1. **Immediate (page 138)**

Q: eLEBORATE Pre-Fetching CONCEPT?

Ans: Pre-fetching technique is used with a pipelined architecture.

Q: Write RTL functions and there was a rb +rc instruction.

ANS: (op<4..0>=0): R[ra] ← R[rb] + R[rc],

Q: how we speed-up a computer?

Q: Write execution time of an instruction (there was a description too)

AnsL The execution time of a program with respect to the processor, is defined as **Execution Time = IC x CPI x T**

Where, IC = instruction count

CPI = average number of system clock periods to execute an instruction

T = clock period

Q : Types of instructions
Q : How you represent register data field?
ANS: `register data in` **`ra`** `is placed in the buffer register C through ALSU unit`

1)define virtual memory ?
2)differentiate between shared device and switched device?
3)write any three silent features of RAID level ....RAID levels se 3Q aya thy aik 5 marks ka aur aik 3 kamujy bas yahi 1 yad reh gia hain aur taqreeban 8,10 mcqs b aye thy is se
4) what is segmentation and write its addressing mechanism/ 5marks
5) write RTL for the following instructions 5marks
movi R3, 65
in R3, 57
out R3, 45
ret R3
addi R4, R3, 45
6) write one disaddvanteg and one addvantge of cache design
7) write the structure of the 64*1 SRAM chip

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Question # 1 of 10 (Start time: 10:02:48 PM) Total Marks: 1
What is the size of the memory space that is available to FALCON-A processor?
Select correct option:

2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes

Question # 2 of 10 (Start time: 10:03:58 PM) Total Marks: 1
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
Select correct option:

IR<16..0>
IR<15..0>
IR<16..1>
IR<15..1>

Question # 3 of 10 (Start time: 10:04:28 PM) Total Marks: 1
What is the working of Processor Status Word (PSW)?
Select correct option:

To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing
To hold the address of the next instruction in memory that is to be executed

Question # 4 of 10 (Start time: 10:05:10 PM) Total Marks: 1
What does the instruction "ldr R3, 58" of SRC do?
Select correct option:

It will load the register R3 with the contents of the memory location M [PC+58]
It will load the register R3 with the relative address itself (PC+58).
It will store the register R3 contents to the memory location M [PC+58]
No operation

Question # 5 of 10 (Start time: 10:06:34 PM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 6 of 10 (Start time: 10:06:57 PM) Total Marks: 1
Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:

Address
Instruction code
Opcode
Operand

Question # 8 of 10 (Start time: 10:07:36 PM) Total Marks: 1
For the __________ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory
Select correct option:

Jump
Control
load/store
None of the given

Question # 9 of 10 (Start time: 10:08:08 PM) Total Marks: 1
Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
Select correct option:

Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

Question # 10 of 10 (Start time: 10:08:50 PM) Total Marks: 1
Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3
Select correct option:

Opcode= R1, DR=ADD, SA=R2, SB=R3
Opcode= ADD, DR=R1, SA=R2, SB=R3
Opcode= R2, DR=ADD, SA=R1, SB=R3
Opcode= ADD, DR=R3, SA=R2, SB=R1

Question # 1 of 10 (Start time: 10:20:53 PM) Total Marks: 1
Which one of the following circuit design levels is called the gate level?
Select correct option:

Logic Design Level
Circuit Level
Mask Level
None of the given

Question # 2 of 10 (Start time: 10:21:17 PM) Total Marks: 1
The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
Select correct option:

Jump and branch format instructions
Immediate format instructions
Register format instructions
All of the above

Question # 5 of 10 (Start time: 10:24:08 PM) Total Marks: 1
P: R3 <- R5 MAR <- IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
Select correct option:

Parentheses ()
Arrow <-
Colon :
Comma ,

Question # 6 of 10 (Start time: 10:25:09 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:

Arithmetic/logic
Load/store
Test/branch
None of the given

What does the word 'D' in the 'D-flip-Flop' stands for?
Select correct option:

Data
Digital
Dynamic
Double

Question # 9 of 10 (Start time: 10:27:24 PM) Total Marks: 1
The instruction ---------------will load the register R3 with the contents of the memory location M [PC+56]

Select correct option:

Add R3, 56
lar R3, 56
ldr R3, 56
str R3, 56

Question # 10 of 10 (Start time: 10:28:07 PM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 2 of 10 (Start time: 10:41:07 PM) Total Marks: 1
Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
Select correct option:

4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes
13 bytes, 22 bytes

Question # 3 of 10 (Start time: 10:41:57 PM) Total Marks: 1
Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:

Address
Instruction code
Opcode
Operand

Question # 4 of 10 (Start time: 10:42:17 PM) Total Marks: 1
Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?
Select correct option:

:=
&
%
©

Question # 5 of 10 (Start time: 10:42:37 PM) Total Marks: 1
What is the size of the memory space that is available to FALCON-A processor?
Select correct option:

2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes

Question # 7 of 10 (Start time: 10:43:25 PM) Total Marks: 1
An “assembler” that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------------
Select correct option:

compiler
cross assembler
debugger
linker

Question # 8 of 10 (Start time: 10:43:59 PM) Total Marks: 1
Which instruction is used to store register to memory using relative address?
Select correct option:

ld instruction
ldr instruction
lar instruction
str instruction

Question # 9 of 10 (Start time: 10:44:37 PM) Total Marks: 1
What does the instruction “ldr R3, 58” of SRC do?
Select correct option:

It will load the register R3 with the contents of the memory location M [PC+58]
It will load the register R3 with the relative address itself (PC+58).
It will store the register R3 contents to the memory location M [PC+58]
No operation
Question # 1 of 10 (Start time: 11:06:09 PM) Total Marks: 1
Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?
Select correct option:
Base address
Binary address
Effective address
All of the given

Quiz Start Time: 11:06 PM
Time Left 88
sec(s)
Question # 2 of 10 (Start time: 11:06:53 PM) Total Marks: 1
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
Select correct option:
IR<16..0>
IR<15..0>
IR<16..1>
IR<15..1>

Question # 3 of 10 (Start time: 11:07:32 PM) Total Marks: 1
What functionality is performed by the instruction “str R8, 34” of SRC?
Select correct option:
It will load the register R8 with the contents of the memory location M [PC+34]
It will load the register R8 with the relative address itself (PC+34).

It will store the register R8 contents to the memory location M [PC+34]
No operation

Question # 4 of 10 (Start time: 11:08:39 PM) Total Marks: 1
Which type of instructions help in changing the flow of the program as and when required?
Select correct option:
Arithmetic
Control
Data transfer
Floating point

Question # 5 of 10 (Start time: 11:09:24 PM) Total Marks: 1
Whic of the following statements is/are true about RISC processors' claimed advantages over CISC processors? (a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution. (b) RISC CPUs outperform CISC CPU's in procedural programming environments. (c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction. (d) It is easier to maintain the "family concept" in RISC CPUs.
Select correct option:
(a), (b) &(c)
(b), (c) & (e)
(c), (d) & (e)
(a), (c) & (d)

Question # 8 of 10 (Start time: 11:11:44 PM) Total Marks: 1
Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

Question # 9 of 10 (Start time: 11:12:32 PM) Total Marks: 1
Which one of the following is/are the features of Register Transfer Language? a) It is a symbolic language b) It is describing the internal organization of digital computers c) It is an elementary operation performed (during one clock pulse), on the information stored in one or more registers d) It is high level language
Select correct option:
(b) only
(a) & (b) only
(a) ,(b) & (d)
(b),(c) & (d)

Question # 10 of 10 (Start time: 11:14:04 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

Question # 3 of 10 (Start time: 08:03:34 PM) Total Marks: 1
Motorola MC68000 is an example of ---------microprocessor.

Select correct option:

CISC
RISC
SRC
FALCON

Question # 5 of 10 (Start time: 08:05:09 PM) Total Marks: 1
Which one of the following registers holds the instruction that is being executed?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 9 of 10 (Start time: 08:08:13 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain ____________ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:

Registers
Control signals
Memory
None of the given

Question # 10 of 10 (Start time: 08:09:02 PM) Total Marks: 1
The external interface of FALCON-A consists of a ________ data bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 1 of 10 (Start time: 08:18:13 PM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 2 of 10 (Start time: 08:18:29 PM) Total Marks: 1
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?
Select correct option:

Perfecting
Pipelining

Superscalar operation
Speedup

Question # 3 of 10 (Start time: 08:18:52 PM) Total Marks: 1
__________ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC
INC4
LC
Cout

Question # 4 of 10 (Start time: 08:19:03 PM) Total Marks: 1
The processor must have a way of saving information about its state or context so that it can be restored upon return from the -------------
Select correct option:

Exception
Function
Thread
Stack

Question # 5 of 10 (Start time: 08:20:13 PM) Total Marks: 1
-----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 6 of 10 (Start time: 08:20:40 PM) Total Marks: 1
_________ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:

INC4
LPC
PCout
LC

Question # 7 of 10 (Start time: 08:21:15 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 8 of 10 (Start time: 08:21:49 PM) Total Marks: 1
Computer system performance is usually measured by the ---------------
Select correct option:

Time to execute a program or program mix
The speed with which it executes programs
Processor's utilization in solving the problems
Instructions that can be carried out simultaneously   I use here double dip :d

Question # 9 of 10 (Start time: 08:22:09 PM) Total Marks: 1
The external interface of FALCON-A consists of a ____________ address bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:22:19 PM) Total Marks: 1
Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?
Select correct option:

Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 1 of 10 (Start time: 08:24:34 PM) Total Marks: 1
-------------- performs the data operations as commanded by the program instructions.
Select correct option:

Control
Datapath
Structural RTL
Timing

Question # 2 of 10 (Start time: 08:25:17 PM) Total Marks: 1
_________ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:

INC4
LPC
PCout
LC

Question # 3 of 10 (Start time: 08:25:30 PM) Total Marks: 1
The external interface of FALCON-A consists of a __________address bus and a _________ data bus.
Select correct option:

8-bit , 8-bit
16-bit , 16-bit
16-bit , 24-bit
16-bit , 32-bit

Question # 4 of 10 (Start time: 08:25:50 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 5 of 10 (Start time: 08:26:02 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:

Accumulator
Address Mask
Instruction Register
Program Counter

Question # 6 of 10 (Start time: 08:26:41 PM) Total Marks: 1
Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?
Select correct option:

Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 7 of 10 (Start time: 08:27:38 PM) Total Marks: 1
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is __________ wide.
Select correct option:

8-bits
16-bits
32-bits
64-bits

Question # 8 of 10 (Start time: 08:27:54 PM) Total Marks: 1
__________ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC
INC4
LC

Cout

Question # 9 of 10 (Start time: 08:28:10 PM) Total Marks: 1
The external interface of FALCON-A consists of a ________ data bus.
Select correct option:

8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:28:29 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain ___________ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:

Registers
Control signals
Memory
None of the given

Which one of the following is the memory organization of EAGLE processor?

2^8 * 8 bits
2^16 * 8 bits
2^32 * 8 bits
2^64 * 8 bits

CS501 today paper

- Date 13-05-2012

What is the instruction length of the FALCON-E processor?
Select correct option:
8 bits
16 bits
32 bits
64 bits

Which one of the following circuit design levels is called the gate level?
Select correct option:
Logic Design Level
Circuit Level
Mask Level
None of the given

What does the word 'D' in the 'D-flip-Flop' stands for?
Select correct option:

Data
Digital
Dynamic
Double

The instruction ---------------will load the register R3 with the contents of the memory location M [PC+56]
Select correct option:
Add R3, 56
lar R3, 56
ldr R3, 56
str R3, 56

Which instruction is used to store register to memory using relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction

Which one of the following registers holds the instruction that is being executed?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter

For any of the instructions that are a part of the instruction set of the SRC, there are certain _____________ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:
Registers
Control signals
Memory
None of the given

The external interface of FALCON-A consists of a ________ data bus.
Select correct option:
8-bit
16-bit
24-bit
32-bit

___________ enable the input to the PC for receiving a value that is currently on the

internal processor bus.
Select correct option:
LPC
INC4
LC
Cout

Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?
Select correct option:
Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

-------------- performs the data operations as commanded by the program instructions.
Select correct option:
Control
Datapath
Structural RTL
Timing

Question No: 3 (Marks: 1) - Please choose one

"If P = 1, then load the contents of register R1 into register R2". This statement can be written in RTL as:

- ▶ R1 ¬ R2
- ▶ P: R1 ¬ R2
- ▶ P: R2 ¬ R1
- ▶ P: R2 ¬ R1, P: R1 ¬ R2

Question No: 12 (Marks: 1) - Please choose one

There are __________ types of reset operations in SRC

- ▶ Two
- ▶ Three
- ▶ Four
- ▶ Five

Question:-

Write down two processors name of superscalar architecture mark 2

Question:-

Structural RTL for subtract instruction

sub ra, rb, rc

In sub instruction three registers are involved. The first three steps will fetch the sub instruction and in T3, T4, T5 the steps for execution of the sub instruction will be performed.

Step	RTL
T0-T2	Instruction fetch
T3	A ← R[rb];
T4	C ← A - R[rc];
T5	R[ra] ← C;

Convert table into instruction form

Question:-

How exception may b generated write the difference between external and internal exceptions? 3 marks

Question:-

What are the pipeline problems. Describe each briefly.... 5marks

Question:-

Write the structure RTL description for the uni-bus data path implementation Jump[ra+2] (5 Marks)